PM5316

SPECTRA-4X155

SONET/SDH PAYLOAD EXTRACTOR/ALIGNER

DEVICE ERRATA

ISSUE 2: AUGUST 2001

PRODUCTION

REVISION HISTORY

Issue No.	Issue Date	Details of Change
2	August 2001	Document updated to detail known documentation errors in issue 4 datasheet
1	December 2000	Document created.

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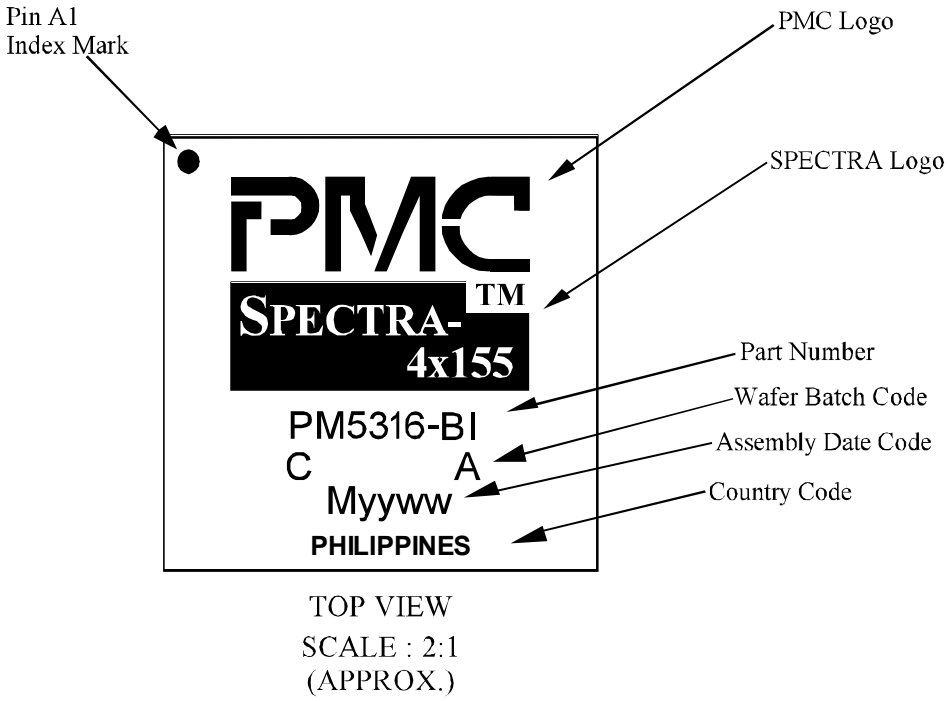
1 ISSUE 2 ERRATA

This document is the errata notice for Revision A, production release of the SPECTRA-4x155 (PM5316-BI) and issue 4 SPECTRA-4x155 datasheet. The issue 4 SPECTRA-4x155 datasheet (PMC-1990822) and issue 2 errata supersede all prior editions and versions of the datasheet.

1.1 Device Identification

The information in this document applies to the PM5316 SPECTRA-4x155 revision A device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM5316 SPECTRA-4x155 Revision A is packaged in a 520 pin Super BGA package.

Figure 1: PM5316 SPECTRA-4x155 Branding Format



2 SPECTRA-4X155 ISSUE 4 DATASHEET ERRATA

This section contains known errata in the issue 4 SPECTRA-4x155 datasheet.

1. *comments specific to this document are in italics*
2. new text is written in regular font

2.1 Patents

The following text indicates relevant patent information for SPECTRA-4x155:

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,959,490

Relevant patent applications and other patents may also exist.

2.2 Pin Diagram – pages 13-16

The following pins should be labeled as RESERVED on the pin diagram:

D25: Reserved1 (No Connect)
C25: Reserved2 (No Connect)
A25: Reserved3 (Ground)
E24: Reserved4 (Ground)
B25: Reserved5 (No Connect)

The following pins are labeled as NO CONNECT pins on the pin diagram. Note that this list does not indicate any changes from Issue 4 Datasheet pin diagram. Rather, this list is provided as a cross-reference to the pin diagram in Issue 4 Datasheet.

NO CONNECT PIN LIST							
A23	AF4	AG30	AH5	AK23	AL25	E4	P1
A5	AF5	AG4	AJ19	AK24	AL27	E8	P2
AA4	AG1	AG7	AJ20	AK25	AL5	F3	P3
AC1	AG17	AH10	AJ21	AK26	B23	F4	R27
AC2	AG18	AH12	AJ22	AK27	B5	F5	R29
AC27	AG19	AH19	AJ23	AK6	B7	G1	R30
AD1	AG2	AH2	AJ24	AK8	C23	G27	R31
AD29	AG20	AH20	AJ25	AL13	C5	H1	R5
AE2	AG22	AH21	AJ26	AL14	D22	H2	U5
AE3	AG23	AH22	AJ27	AL15	D30	J1	W30
AE4	AG24	AH23	AJ6	AL19	D5	J4	W4
AE5	AG25	AH24	AK19	AL20	E1	J5	W5
AF2	AG26	AH25	AK20	AL22	E2	K5	
AF27	AG28	AH26	AK21	AL23	E22	M27	
AF3	AG3	AH27	AK22	AL24	E3	N5	

2.3 Pin Descriptions – page 23, page 42

The following pin description omitted Pin Number from Issue 4 Datasheet:

Section 9.3 Receive Section/Line/Path Overhead Extraction Signals*:*

Pin Name	Pin Type	PIN No.	Function
RAD	Output	D23	The receive alarm port data signal (RAD) contains the path BIP error count and the path remote alarm indication status of the three STS-1 (STM-0/AU-3) streams or STS-3c (STM-1/AU-4) streams for all four channels. In Addition, the RAD contains the transmit K1 and K2 bytes of the four transmit streams when not generating AIS-L on the transmit stream. RPOHFP is used to determine the alignment of the RAD output. RAD is updated on the falling edge of RPOHCLK.

The following pin descriptions were omitted from Issue 4 Datasheet:

Section 9.13 Power and Ground:

Pin Name	Pin Type	PIN No.	Function
Reserved5	Output	B25	This output can be left floating
VBIAS[0] VBIAS[1]	Bias Voltage	AK28 E20	Digital input biases(VBIAS). When tied to +5V, the VBIAS input is used to bias the wells of the digital inputs so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When VBIAS is tied to +3.3V, the all digital inputs will only tolerate 3.3V level voltages.
QAVD1 QAVD2	Analog Power	G5 AD5	The quiet power (QAVD1-2) pins for the analog core. QAVD should be connected to well-decoupled analog +3.3V supply. Please see the Operation section for detailed information.
QAVS1 QAVS2	Analog Ground	F2 AE1	The quiet ground (QAVS1-2) pins for the analog core. QAVS should be connected to analog ground of the QAVD supply. Please see the Operation section for detailed information.

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