HYUNDAI

# HY29F040A Series

**512K x 8-bit CMOS 5.0 volt-only, Sector Erase Flash Memory**

## KEY FEATURES

- **5.0 V ± 10% Read, Program, and Erase**
  - Minimizes system-level power requirements
- **High performance**
  - 55 ns access time
- **Compatible with JEDEC-Standard Commands**
  - Uses software commands, pinouts, and packages following industry standards for single power supply Flash memory
- **Minimum 100,000 Program/Erase Cycles**
- **Sector Erase Architecture**
  - Eight equal size sectors of 64K bytes each
  - Any combination of sectors can be erased concurrently; also supports full chip erase
- **Erase Suspend/Resume**
  - Suspend a sector erase operation to allow a data read or programming in a sector not being erased within the same device
- **Internal Erase Algorithms**
  - Automatically erases a sector, any combination of sectors, or the entire chip
- **Internal Programming Algorithms**
  - Automatically programs and verifies data at a specified address.
- **Low Power Consumption**
  - 40 mA maximum active read current
  - 60 mA maximum program/erase current
  - 5 mA maximum standby current
- **Sector Protection**
  - Hardware method disables any combination of sectors from a program or erase operation

## DESCRIPTION

The HY29F040A is a 4 Megabit, 5.0 volt-only CMOS Flash memory device organized as a 512K bytes of 8 bits each. The device is offered in standard 32-pin PDIP, 32-pin PLCC and 32-pin TSOP packages. It is designed to be programmed and erased in-system with a 5.0 volt power-supply and can also be reprogrammed in standard PROM programmers.

The HY29F040A offers access times of 55 ns, 70 ns, 90 ns, 120 ns and 150 ns. The device has separate chip enable (/CE), write enable (/WE) and output enable (/OE) controls. Hyundai Flash memory devices reliably store memory data even after 100,000 program/erase cycles.

The HY29F040A is entirely pin and command set compatible with the JEDEC standard for 4 Megabit Flash memory devices. The commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The HY29F040A is programmed by executing the program command sequence. This will start the internal byte programming algorithm that automatically times the program pulse width and also verifies the proper cell margin. Erase is accomplished by executing either sector erase or chip erase command sequence. This will start the internal erasing algorithm that automatically times the erase pulse width and also verifies the proper cell margin. No preprogramming is required prior to execution of the internal erase algorithm. Sectors of the HY29F040A Flash memory array are electrically erased via Fowler-Nordheim tunneling. Bytes are programmed one byte at a time using a hot electron injection mechanism.

The HY29F040A features a sector erase architecture. The device memory array is divided into 8 sectors of 64K bytes each. The sectors can be erased individually or in groups without affecting the data in other sectors. The multiple sector erase and full chip erase capabilities add flexibility to altering the data in the device. To protect data in the device from accidental program and erase, the device also has a sector protect function. This function hardware write protects the selected sectors. The sector


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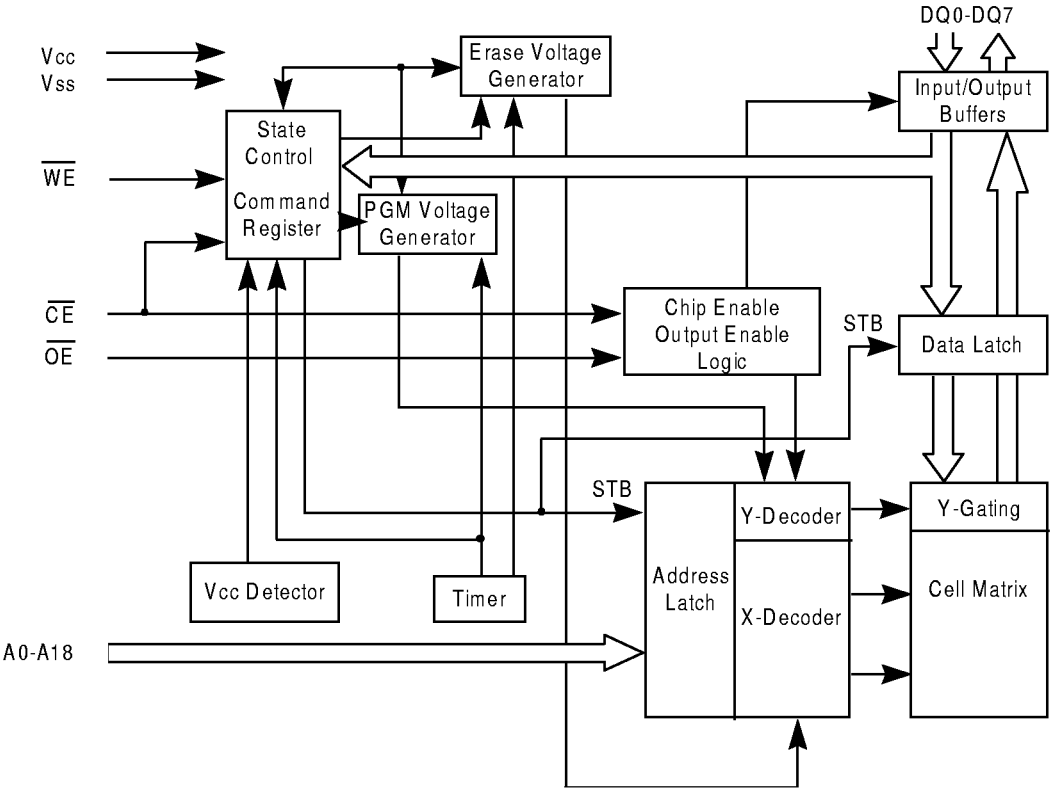
protect and sector unprotect features can be enabled in a PROM programmer.

The HY29F040A needs a single 5.0 volt power-supply for read, program and erase operation. Internally generated and well regulated voltages are provided for program and erase operation. A low Vcc detector inhibits write operations on loss of power. End of program or erase is detected by /Data Polling of DQ7 or by the Toggle Bit feature on DQ6. Once program or erase cycle is successfully completed, the device internally resets to the Read mode.

## BLOCK DIAGRAM



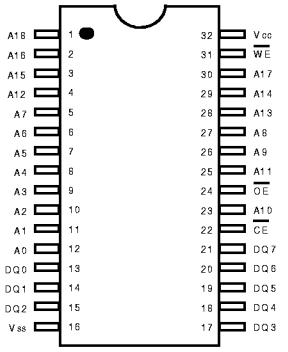
## PIN DESCRIPTION

| Pin Name | Pin Function |
|---|---|
| A0 - A18 | Address Inputs |
| DQ0 - DQ7 | Data Input/Output |
| /CE | Chip Enable |
| /OE | Output Enable |
| /WE | Write Enable |
| Vss | Device Ground |
| Vcc | Device Power Supply<br>(5.0V ± 10 % for -70, -90, -120 and -150)<br>(5.0V ± 5 % for -55) |

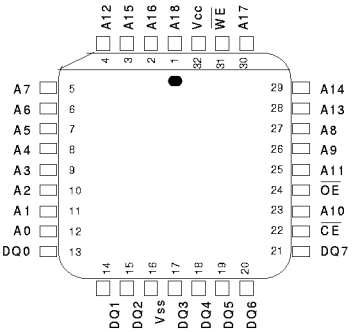
## PIN CONNECTION


**Standard TSOP**


**Reverse TSOP**




**PDIP**




**PLCC**

## BUS OPERATION

### Table 1. Bus Operations[1]

| OPERATION | /CE | /OE | /WE | A0 | A1 | A6 | A9 | I/O |
|---|---|---|---|---|---|---|---|---|
| Electronic ID Manufacturer Code[2] | L | L | H | L | L | L | $V_{ID}$ | Code |
| Electronic ID Device Code[2] | L | L | H | H | L | L | $V_{ID}$ | Code |
| Read[3] | L | L | H | A0 | A1 | A6 | A9 | $D_{OUT}$ |
| Standby | H | X | X | X | X | X | X | High Z |
| Output Disable | L | H | H | X | X | X | X | High Z |
| Write | L | H | L | A0 | A1 | A6 | A9 | $D_{IN}$[4] |
| Enable Sector Protect | L | $V_{ID}$ | L | X | X | X | $V_{ID}$ | X |
| Verify Sector Protect | L | L | H | L | H | L | $V_{ID}$ | Code |

**Notes:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care. See DC Characteristics for voltage levels.
2. Manufacturer and device codes may also be accessed via a command register sequence. Refer to Table 4.
3. /WE can be $V_{IL}$ if /CE is $V_{IL}$, /OE at $V_{IH}$ initiates the write operations.
4. Refer to Table 4 for valid $D_{IN}$ during a write operation.

### Table 2. Sector Protection Verify Electronic ID Codes

| Type | A18 | A17 | A16 | A6 | A1 | A0 | Code HEX | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacture Code | X | X | X | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | ADH | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| HY29F040A Device Code | X | X | X | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | A4H | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| Sector Protection | Sector Addresses | | | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | 01H[1] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Notes:**
1. Outputs 01H at protected sector addresses, and output 00H at unprotected sector addresses.

**Table 3. Sector Addresses**

| | A18 | A17 | A16 | Address Range |
|---|---|---|---|---|
| SA0 | 0 | 0 | 0 | 00000H - 0FFFFH |
| SA1 | 0 | 0 | 1 | 10000H - 1FFFFH |
| SA2 | 0 | 1 | 0 | 20000H - 2FFFFH |
| SA3 | 0 | 1 | 1 | 30000H - 3FFFFH |
| SA4 | 1 | 0 | 0 | 40000H - 4FFFFH |
| SA5 | 1 | 0 | 1 | 50000H - 5FFFFH |
| SA6 | 1 | 1 | 0 | 60000H - 6FFFFH |
| SA7 | 1 | 1 | 1 | 70000H - 7FFFFH |

## Electronic ID Mode

The Electronic ID mode allows the reading out of a binary code from the device and will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force $V_{ID}$ (11.5V to 12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from $V_{IL}$ to $V_{IH}$. All addresses are don't cares except A0, A1, A6, and A9.

The manufacturer and device codes may also be read via the command register, (i.e., when HY29F040A is erased or programmed in a system without access to high voltage on the A9 pin). The command sequence is illustrated in Table 4 (refer to Electronic ID Command section).

Byte 0 (A0=$V_{IL}$) represents the manufacturer's code (Hyundai Electronics=ADH) and byte 1 (A0=$V_{IH}$) the device identifier code (HY29F040A=A4H). These two bytes are given in Table 2. All identifiers for manufacturer and devices will exhibit odd parity with the MSB (DQ7) defined as the parity bit. To permit reading of the proper device codes when executing the Electronic ID, A1 must be $V_{IL}$ (see Table 2).

## Read Mode

The HY29F040A has three control functions which must be satisfied to obtain data at the outputs. /CE is the power control and should be used for device selection. /OE is the output control and should be used to gate data to the output pins if a device is selected. As shown in Table 1, /WE should be held at $V_{IH}$, except in Write mode and Enable Sector Protect mode.

Address access time ($t_{ACC}$) is equal to the delay from stable addresses to valid output data. The chip enable access time ($t_{CE}$) is the delay from stable addresses and stable /CE to valid data at the output pins. The output enable access time is the delay from the falling edge of /OE to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC}$-$t_{OE}$ time).

## Standby Mode

The HY29F040A has two standby modes: a CMOS standby mode (/CE input held at Vcc ± 0.5V), when current consumed is typically less than 1 mA; and a TTL standby mode (/CE is held at $V_{IH}$) when the typical current required is reduced to 1 mA. In standby mode, outputs are in a high impedance state, independent of /OE input.

If the device is deselected during programming or erase, the device will draw active current until the programming or erase operation is completed.

## Output Disable Mode

With the /OE input at a logic high level ($V_{IH}$), output from the device is disabled. This will cause the output pins to be in a high impedance state. It is shown in Table 1 that /CE = $V_{IL}$ and /WE = $V_{IH}$ for Output Disable. This is to differentiate Output Disable mode from Write mode and to prevent inadvertant writes during Output Disable.

## Write Mode

Device programming and erase are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. Outputs of the state machine dictate the function of the device.

The command register itself does not occupy any addressable memory locations. The register is a latch used to store the commands along with the addresses and data information needed to execute the command. The command register is written by bringing /WE to $V_{IL}$, while /CE is at $V_{IL}$ and /OE is at $V_{IH}$. Addresses are latched on the falling edge of /WE or /CE, whichever happens later, while data is latched on the rising edge of /WE or /CE, whichever happens first. Standard microprocessor write timings are used. Refer to AC Characteristics for Programming/Erase and their respective Timing Waveforms for specific timing parameters.

## Enable Sector Protect and Verify Sector Protect Modes

The HY29F040A has a hardware Sector Protect mode that disables both Programming and Erase operation to protected sectors. In this device there are 8 sectors of 64K bytes each. The sector protect feature is enabled using programming equipment at the user's site. The device is shipped from Hyundai's factory with all sectors unprotected.

To activate the Sector Protect mode, the user must force $V_{ID}$ on address pin A9 and control pin /OE. The sector addresses (A18, A17 and A16) should be set to the sector to be protected (see Table 3 for the sector address for each of the eight individual sectors). Programming of the protection circuitry starts on the falling edge of /WE pulse and is terminated with the rising edge of /WE. Sector addresses must be held fixed during the /WE pulse.

To verify programming of the protection circuitry, the programming equipment must force $V_{ID}$ on the address pin A9 with /CE and /OE at $V_{IL}$ and /WE at $V_{IH}$. As shown in Table 2, scanning the sector addresses (A18, A17 and A16) while (A6, A1 and A0) = (0, 1, 0) will produce a 01H code at the device output pins for a protected sector. In the Verify Sector Protect mode, the device will read 00H for an unprotected sector. In this mode, the lower order addresses, except for A0, A1 and A6, are don't care. Address locations with A1 = $V_{IL}$ are reserved for electronic ID manufacturer and device codes. It is also possible to determine if a sector is protected in-system by writing the Electronic ID command (described in the Electronic ID command section below).

## COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the Command register. Writing incorrect addresses and data values or writing them in the improper sequence will reset the device to Read mode. Table 4 defines the valid register command sequences. Either Read/Reset command will reset the device (when applicable).

### Table 4. Command Definitions(1,2,3,4)

| Command Sequence | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read/Reset | 1 | XXXH | F0H | RA | RD | | | | | | | | |
| Read/Reset | 4 | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | RA | RD | | | | |
| Electronic ID | 4 | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | XX00H<br>XX01H | ADH<br>A4H | | | | |
| Byte Program | 4 | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | PA | PD | | | | |
| Chip Erase | 6 | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Sector Erase | 6 | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | SA | 30H |
| Erase Suspend | 1 | XXXH | B0H | | | | | | | | | | |
| Erase Resume | 1 | XXXH | 30H | | | | | | | | | | |

**Notes:**
1. Bus Operations are defined in Table 1.
2. For a Command Sequence, address bits A15, A14, A13, A12, and A11 = X = Don't care. Address bits A18, A17, A16, and A15 = X = Don't care for all address commands except for Program Address(PA) and Sector Address(SA).
   In the case of Sector Address, address bit A15 = X = Don't care for all addresses except for Program Address (PA) and Sector Addresses (SA).
3. RA = Address of the memory location to be read.
   RD = Data read from location RA during read operation.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the /WE pulse.
   PD = Data to be programmed at location PA. Data is latched on the falling edge of /WE.
   SA = Address of the sector to be erased (see Table 3).
4. The Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

## Read/Reset Command

The read or reset operation is initiated by writing the Read/Reset command sequence in to the command register. Microprocessor read cycles retrieve the data from the memory. The device remains enabled for reads until the command register contents are changed.

The device will automatically power-up in the Read/Reset mode. In this case, a command sequence is not needed to read the memory data. This default power-up to Read mode ensures that no spurious changes of the data can take place during the power transitions. Refer to the AC Characteristics for Read-Only Operation and the respective Timing Waveforms for the specific timing parameters.

## Electronic ID Command

The HY29F040A contains an Electronic ID command to supplement the traditional PROM programming method described in the Electronic ID Mode section. The operation is initiated by writing the Electronic ID command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves manufacturer code of ADH. A read cycle from address XX01H returns the device code A4H (see Table 2). All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

The Electronic ID command can also be used to identify protected sectors. After writing the Electronic ID command sequence, the CPU can scan the sector addresses (A18, A17, A16) while (A6, A1, A0) = (0, 1, 0). Protected sectors will return 01H on the data outputs and unprotected sectors will return 00H. To terminate the operation, it is necessary to write the Read/Reset command sequence into the command register.

## Byte Programming Command

The HY29F040A is programmed one byte at a time. Programming is a four bus cycle operation (see Table 4). The program address (PA) is latched on the falling edge of /CE or /WE, whichever happens later, and program data (PD) is latched on the rising edge of /CE or /WE, whichever happens first. The rising edge of /CE or /WE, whichever happens first, begins byte programming.

Upon executing the Byte Programming command sequence, the device's internal state machine executes an internal byte programming algorithm. The system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin of the byte.

During byte programming operation, data bit DQ7 shows the complement of the program data. This operation is known as /Data Polling. The internal byte programming algorithm has completed it's operation when the data on DQ7 is equivalent to the last data written to this bit (see Write Operation Status section). At the completion of the byte programming algorithm, the device returns to the read mode. At this time, the address pins are no longer latched. Therefore, the system must supply the last program address at the completion of the byte programming operation to read the correct program data on DQ7.

Byte programming is allowed in any sequence, and across sector boundaries. However, remember that a data "0" cannot be programmed to a data "1". Only erase operations can convert a logical "0" to a logical "1". Attempting to program data from "0" to "1" may cause the device to exceed time limits, or even worse, result in an apparent success according to the /Data Polling algorithm. In the later case, however, a subsequent read of this bit will show that the data is still a logical "0".

Figure 1 illustrates the Byte Programming Algorithm using typical command strings and bus operations.

## Chip Erase Command

Chip erase is a six bus cycle operation (see Table 4). Chip erase begins on the rising edge of the last / WE pulse in the command sequence. There are two 'unlock' write cycles. These are followed by

writing the "set-up" command. Two more 'unlock' write cycles are then followed by the chip erase command.

Upon executing the Chip Erase command sequence, the device's internal state machine executes an internal erase algorithm. The system is not required to provide further controls or timings. The device will automatically provide adequate internally generated erase pulses and verify chip erase within the proper cell margins. During chip erase, all sectors of the device are erased except protected sectors.

During Chip Erase, data bit DQ7 shows a logical "0". This operation is known as /Data Polling. The erase operation is completed when the data on DQ7 is a logical "1" (see Write Operation Status section). Upon completion of the Chip Erase operation, the device returns to read mode. At this time, the address pins are no longer latched. Note that /Data Polling must be performed at a sector address within any of the sectors being erased and not a protected sector to ensure that DQ7 returns a logical "1" upon completion of the Chip Erase operation.

Figure 2 illustrates the Chip Erase Algorithm using typical command strings and bus operations. The device will ignore any commands written to the chip during execution of the internal Chip Erase algorithm.

## Sector Erase Command

Sector erase is a six bus cycle operation (see Table 5). There are two 'unlock' write cycles that are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of /WE, while the command data is latched on the rising edge of /WE. An internal device timer initiates Sector Erase operation after 100 ㎳ ± 20% (80 ㎳ to 120 ㎳) from the rising edge of the /WE pulse for the last Sector Erase command entered on the device.

Upon executing the Sector Erase command sequence, the device's internal state machine executes an internal erase algorithm. The system is not required to provide further controls or timings. The device will automatically provide adequate internally generated erase pulses and verify sector erase within the proper cell margins. Protected sectors of the device will not be erased, even if they are selected with the Sector Erase command.

Multiple sectors can be erased sequentially by writing the sixth bus cycle command of the Sector Erase command for each sector to be erased. The time between initiation of the next Sector Erase command must be less than 80 ㎳ to guarantee acceptance of the command by the internal state machine. The time-out window can be monitored via the write operation status pin DQ3 (refer to the Write Operation Status section for Sector Erase Timer operation). It is recommended that CPU interrupts be disabled during this time to ensure that the subsequent Sector Erase commands can be initiated within the 80 ㎳ window. The interrupts can be reenabled after the last Sector Erase command is written. As mentioned above, an internal device timer will initiate the Sector Erase operation 100 ㎳ ± 20% (80 ㎳ to 120 ㎳) from the rising edge of the last / WE pulse. The Sector Erase Timer Write Operation Status pin (DQ3) can be used to monitor the time out window. If another falling edge of the /WE occurs within the 100 ㎳ time-out window, the internal device timer is reset. Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Any command other than Sector Erase or Erase Suspend or Erase Resume during this period and afterwards will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution of a Sector Erase operation will result in the data in the operated sectors being undefined. In this case, restart the Sector Erase operation on those sectors and allow them to complete the Erase operation.

When erasing a sector or multiple sectors, the data in the unselected sectors remains unaffected. The system is not required to provide any controls or timings during these operations.

During Sector Erase operation, data bit DQ7 shows a logical "0". This operation is known as /Data Polling. Sector Erase operation is complete when data on DQ7 is a logical "1" (see Write Operation Status section) at which time the device returns to read mode. At this time, the address pins are no longer latched. Note that /Data Polling must be performed at a sector address within any of the sectors being erased and not a protected sector to ensure that DQ7 returns a logical "1" upon completion of the Sector Erase operation.

Figure 2 illustrates the Sector Erase Algorithm using typical command strings and bus operations.

During execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will reset the device to read mode. Note: *Do not attempt to write an invalid command sequence during the sector erase operation. Doing so will terminate the sector erase operation and the device will reset to the read mode.*

## Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the user to interrupt a Sector Erase operation and read data from or program to a sector that is not being erased. The Erase Suspend command onthe HY29F040 also allows for Byte Programming during the suspended erase from a sector not being erased. The Erase Suspend command is applicable only during Sector Erase operation and will be ignored if written during the Chip Erase operation or Byte Programming operation. The Erase Suspend command (B0H) will be allowed only during the Sector Erase operation, including, but not limited to, the sector erase time-out period after any Sector Erase commands (30H) have been initiated.

Writing the Erase Suspend command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase Resume command (30H). Note that any other commands during the time-out will reset the device to the read mode. The address pins are don't-cares when writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take a maximum of 15 ms to suspend the erase operation and go into erase suspended-read mode. During this time, the system can monitor the /Data Polling or Toggle Bit write operation status flags to determine when the device has entered erase suspend-read mode (see Write Operation Status section). The system must use an address of an erasing sector to monitor /Data Polling or Toggle Bit to determine if the Sector Erase operation has been suspended.

In the erase suspend-read mode, the system can read data from any sector that is not being erased. A read from a sector being erased may result in invalid data.

After the system writes the Erase Suspend command and waits until the Toggle Bit stops toggling, data reads from the device may then be performed. Any further writes of the Erase Suspend command at this time will be ignored.

To resume operation of Sector Erase, the Erase Resume command (30H) should be written. Any further writes of the Erase Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed the Sector Erase operation.

## WRITE OPERATION STATUS

### Table 5. Write Operation Status Flags[1]

| Status | | | DQ7 | DQ6 | DQ5 | DQ3 |
|---|---|---|---|---|---|---|
| In Progress | Byte Programming Operation | | /DQ7 | Toggle | 0 | 0 |
| | Chip or Sector Erase Operation | | 0 | Toggle | 0 | 1 |
| | Erase Suspend Mode | Erase Suspended Sector | 1 | No Toggle | 0 | N/A |
| | | Non-Erase Suspended Sector | Data | Data | Data | Data |
| Exceeded Time Limits | Byte Programming Operation | | /DQ7 | Toggle | 1 | 0 |
| | Chip or Sector Erase Operation | | 0 | Toggle | 1 | 1 |
| | Program in Erase Suspend Mode | | /DQ7 | Toggle | 1 | 1 |

**Notes**:
1. DQ0, DQ1, DQ2, DQ4 are reserve pins for future use.

### DQ7 /Data Polling

The HY29F040A device features /Data Polling as a method to indicate to the host the status of the Byte Programming, Chip Erase, and Sector Erase operations. When the Byte Programming operation is in progress, an attempt to read the device will produce the compliment of the data last written to DQ7. Upon completion of the Byte Programming operation, an attempt to read the device will produce the true data last written to DQ7. When the Chip Erase or Sector Erase operation is in progress, an attempt to read the device will produce a logical "0" at the DQ7 output. Upon completion of the Chip Erase or Sector Erase operation, an attempt to read the device will produce a logical "1" at the DQ7 output. The flowchart for /Data Polling (DQ7) is shown in Figure 3.

For Chip Erase, the /Data Polling is valid after the rising edge of the sixth /WE pulse in the six write pulse sequence. For Sector Erase, the /Data Polling is valid after the last rising edge of the sector erase /WE pulse. For both Chip Erase and Sector Erase, /Data Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the /Data Polling status may not be valid. Once the Internal Algorithm operation is close to being completed, the HY29F040A data pins (DQ7) may change asynchronously while the output enable (/OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Internal Algorithm operation and DQ7 has a valid data, data outputs on DQ0-DQ6 may be still invalid. Valid data on DQ0-DQ7 will be read on successive read attempts.

The Data Polling feature is only active during the Byte Programming operation, Chip Erase operation, Sector Erase Operation, or sector erase time-out window (see Table 5).

### DQ6 Toggle Bit

The HY29F040A also features the "Toggle Bit" as a method to indicate to the host system the status of the Internal Programming and Erase Algorithms. The flowchart for Toggle Bit (DQ6) is shown in Figure 4.

During an Internal Programming or Erase Algorithm cycle, successive attempts to read (/OE toggling) data from the device will result in DQ6 toggling between one and zero. Once the Internal Programming or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the

next successive attempts. During Byte Programming, the Toggle Bit is valid after the rising edge of the fourth /WE pulse in the four write pulse sequence. For Chip Erase, the Toggle Bit is valid after the rising edge of the sixth /WE pulse in the six write pulse sequence. For Sector Erase, the Toggle Bit is valid after the last rising edge of the sector erase /WE pulse. The Toggle Bit is also active during the sector erase time-out window.

In Byte Programming, if the sector being written to is protected, the Toggle Bit toggles for about 2 ㎲ and then stops toggling without the data having changed. In Chip Erase or Sector Erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the Toggle Bit for about 100 ㎲ and then drop back into read mode, having changed none of the data. Either /CE or /OE toggling will cause the DQ6 Toggle Bit to toggle.

### DQ5
### Exceeded Timing Limits

DQ5 will indicate if Byte Programming, Chip Erase, or Sector Erase time has exceeded the specified limits (internal pulse count) of the device. Under these conditions DQ5 will produce a logical "1". This is a failure condition that indicates the program or erase cycle was not successfully completed. /Data Polling is the only operating function of the device under this condition. The /OE and /WE pins will control output disable functions as described in Table 1.

If this failure condition occurs during Sector Erase operation, it indicates a particular sector is bad and it may not be reused. However, other sectors are still functional and may continue to be used for the program or erase operation. To use other sectors of the device, it must be reset to Read mode. Write the Read/Reset command sequence to the device, and then execute the Byte Programming or Sector Erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the Chip Erase operation, it indicates the entire chip is bad or combination of sectors are bad. In this situation, the chip should not be reused.

If this failure condition occurs during the Byte Programming operation, it indicates the entire sector containing that byte is bad and this sector may not be reused (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non-blank location without erasing. In this example, the device may exceed time limits and not complete the Internal Algorithm operation. Hence, the system never reads valid data on DQ7 bit, and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1".

### DQ3
### Sector Erase Timer

After the completion of the initial Sector Erase command sequence, the sector erase time-out window will begin. DQ3 will remain low until the time-out window is closed. /Data Polling and Toggle Bit are valid after the initial Sector Erase command sequence.

If /Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the Sector Erase time-out window is still open. If DQ3 is a logical "1", the internally controlled erase cycle has begun. Attempts to write subsequent command to the device will be ignored until the erase operation is completed as indicated by /Data Polling or Toggle Bit. If DQ3 is a logical "0", the device will accept additional Sector Erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent Sector Erase command. If DQ3 were high on the second status check, the command may not have been accepted. Refer to Table 5: Write Operation Status Flags.

## DATA PROTECTION

The HY29F040A is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power-up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power-up and power-down transitions or system noise.

### Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 3.2V (typically 3.7V). If Vcc < $V_{LKO}$, the command register is disabled and all internal programming/erase circuits are disabled. Under this condition the device will reset to the Read mode. Subsequent writes will be ignored until the Vcc level is greater than $V_{LKO}$. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 3.2V.

### Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on /OE, /CE or /WE will not initiate a write cycle.

### Logical Inhibit

Writing is inhibited by holding any one of /OE = $V_{IL}$, /CE = $V_{IH}$ , or /WE = $V_{IH}$. To initiate a write cycle /CE and /WE must be a logical "0" while /OE is a logical "1".

### Power-Up Write Inhibit

Power-up of the device with /WE = /CE = $V_{IL}$ and /OE = $V_{IH}$ will not accept commands on the rising edge of /WE. The internal state machine is automatically reset to Read mode on power-up.

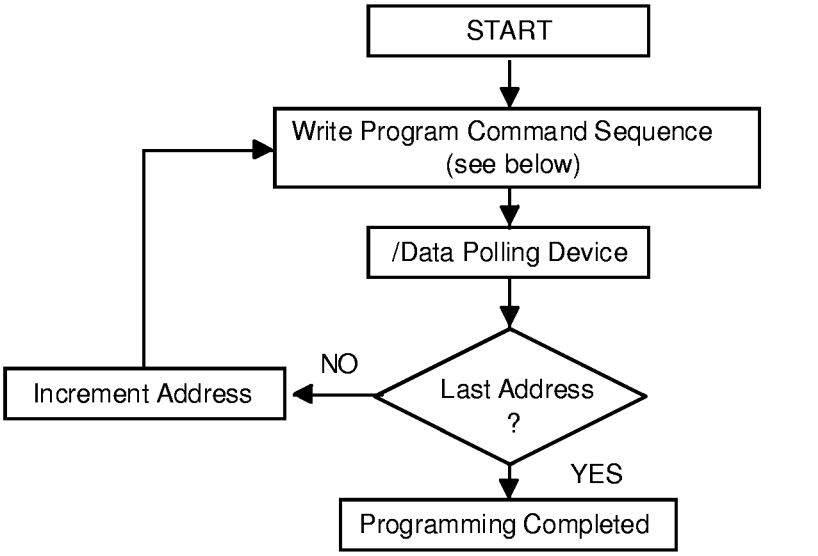
### Sector Protection

Sectors of the HY29F040A may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sectors. Requests to program or erase a protected sector will be ignored by the device. Sector protection is accomplished in a PROM programmer.

The HY29F040A features hardware sector protection that will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, programming equipment must force $V_{ID}$ on control pin /OE and address pin A9. Sector addresses should be set using higher address lines A18, A17 and A16. The protection mechanism begins on the falling edge of the /WE pulse and is terminated with the rising edge of /WE. See Figures 13 and 14 for details of implementing Sector Protect.

### Sector Unprotect

The HY29F040A also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. Protecting all sectors is necessary before unprotecting any sector(s). Sector unprotection is accomplished in a PROM programmer. See Figures 15 and 16 for details of implementing Sector Unprotect.




Program Command Sequence (Address/Command)

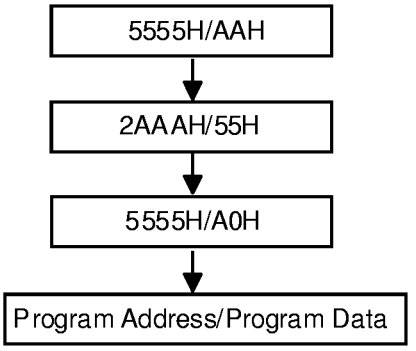



**Figure 1. Internal Programming Algorithm**

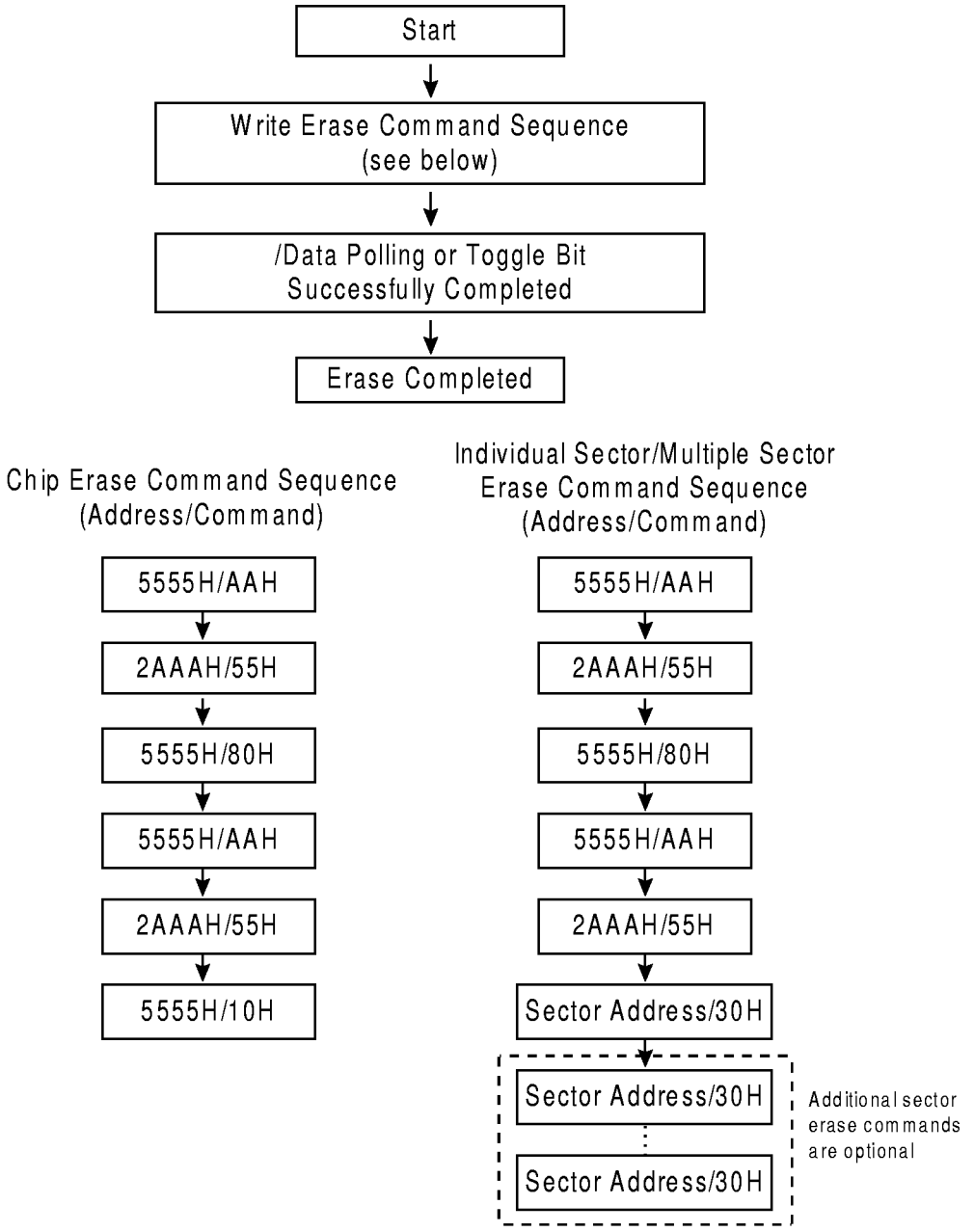
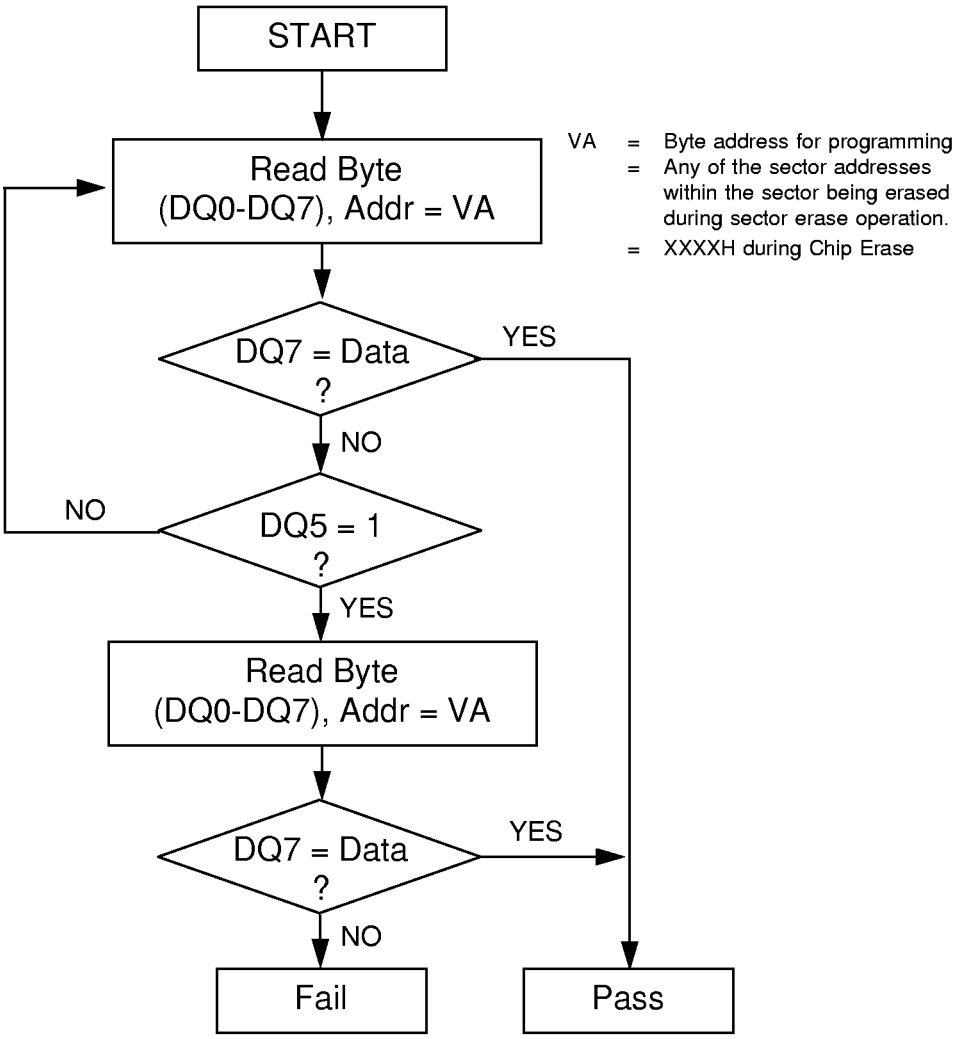


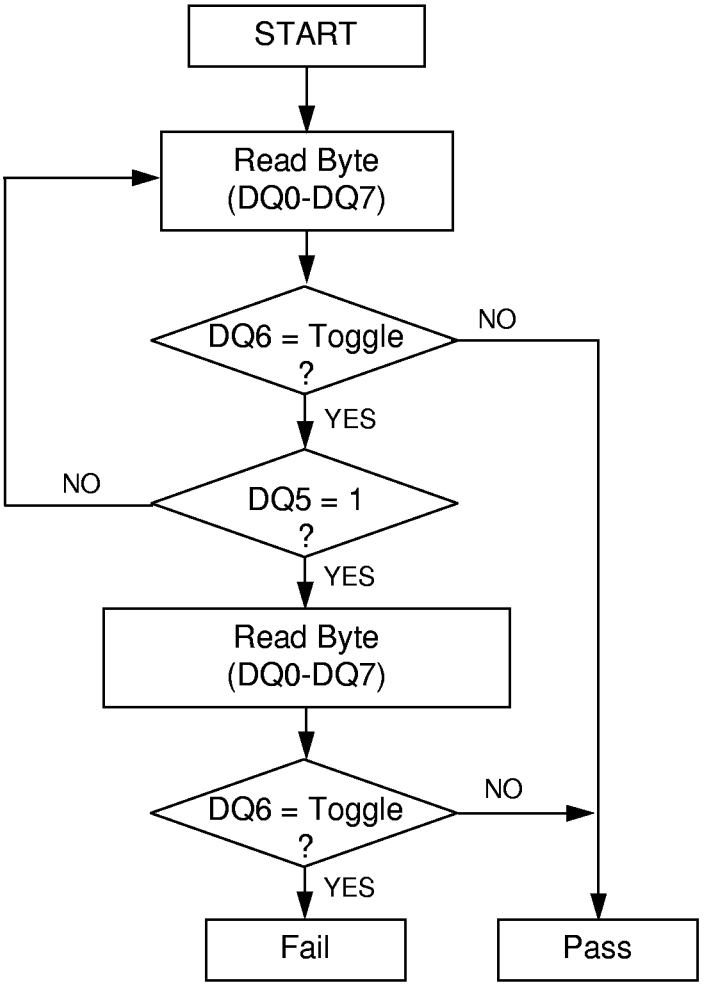

**Figure 2. Internal Erase Algorithm**




**Notes:**

1. DQ7 is rechecked even if DQ5 = logical "1" because DQ7 may change simultaneously with DQ5.

**Figure 3. /Data Polling Algorithm**




**Notes:**
1. DQ6 is rechecked even if DQ5 = logical "1" because DQ6 may stop toggling at the same time as DQ5 changing to a logical "1".

**Figure 4. Toggle Bit Algorithm**

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Package ..... -65°C to + 125°C
Ambient Temperature
With Power Applied ..... -55°C to + 125°C
Voltage with Respect to Ground
All pins except A9 (1) ..... -2.0V to + 7.0V
Vcc[1] ..... -2.0V to + 7.0V
A9[2] ..... -2.0V to + 14.0V
Output Short Circuit Current[3] ..... 200 mA

**Notes:**
1. Minimum DC voltage on input or I/O pins is - 0.5V. During voltage transitions, inputs may overshoot Vss to -2.0V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is Vcc + 0.5V. During Voltage transitions, outputs may overshoot to Vcc + 2.0V for periods up to 20 ns.

2. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2.0V for periods of up to 20 ns. Maximum DC input voltage on A9 is + 13.5V which may overshoot to 14.0V for periods of up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

## OPERATING RANGES

**Commercial( C) Devices** ..... 0°C to + 70°C

**Industrial (I) Devices** ..... -40°C to + 85°C

**Extended (E) Devices** ..... -55°C to + 125°C

**Vcc Supply Voltages** .....
Vcc for HY29F040A-55 ..... + 4.75V to + 5.25V
Vcc for HY29F040A-70, -90, -120, -150
..... + 4.5V to + 5.5V

**Notes:**
1. Operating ranges define those limits between which the functionality of the device is guaranteed.

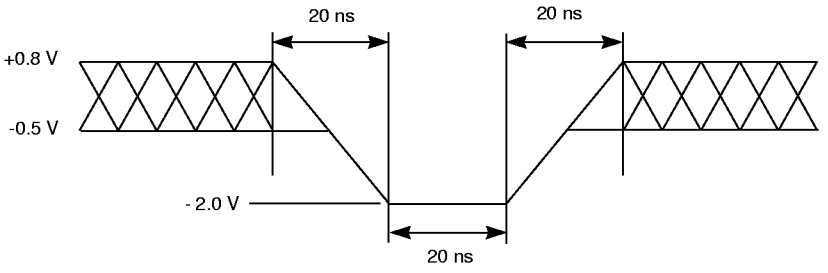



**Figure 5. Maximum Negative Overshoot Waveform**

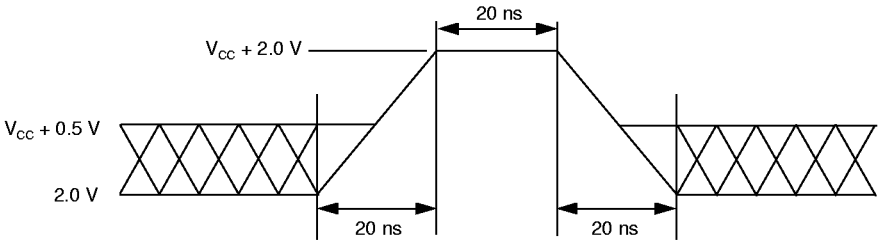



**Figure 6. Maximum Positive Overshoot Waveform**

## DC CHARACTERISTICS

### TTL/NMOS Compatible

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = Vss to Vcc, Vcc = Vcc Max. | | ±1.0 | μA |
| $I_{LIT}$ | A9 Input Load Current | Vcc = Vcc Max., A9 = $V_{ID}$ | | 50 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = Vss to Vcc, Vcc = Vcc Max. | | ±1.0 | μA |
| $I_{CC1}$ | Vcc Active Current[1] | /CE = $V_{IL}$, /OE = $V_{IH}$ | | 40 | mA |
| $I_{CC2}$ | Vcc Active Current[2,3] | /CE = $V_{IL}$, /OE = $V_{IH}$ | | 60 | mA |
| $I_{CC3}$ | Vcc Standby Current | Vcc = Vcc Max., /CE = $V_{IH}$ | | 1.0 | mA |
| $V_{IL}$ | Input Low Level | | -0.5 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.0 | Vcc + 0.5 | V |
| $V_{ID}$ | Voltage for Electronic ID and Sector Protect | Vcc = 5.0 V | 11.5 | 12.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 12 mA, Vcc = Vcc Min. | | 0.45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -2.5 mA, Vcc = Vcc Min. | 2.4 | | V |
| $V_{LKO}$ | Low Vcc Lock-Out Voltage | | 3.2 | 4.2 | V |

**Notes:**

1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 1 mA/MHz, with /OE at $V_{IH}$.
2. Icc active while Internal Algorithm (program or erase) is in progress.
3. Not 100% tested.

## DC CHARACTERISTICS (continued)

### CMOS Compatible

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = Vss to Vcc, Vcc = Vcc Max. | | ±1.0 | μA |
| $I_{LIT}$ | A9 Input Load Current | Vcc = Vcc Max., A9 = $V_{ID}$ | | 50 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = Vss to Vcc, Vcc = Vcc Max. | | ±1.0 | μA |
| $I_{CC1}$ | Vcc Active Current[1] | /CE = $V_{IL}$, /OE = $V_{IH}$ | | 40 | mA |
| $I_{CC2}$ | Vcc Active Current[2,3] | /CE = $V_{IL}$, /OE = $V_{IH}$ | | 60 | mA |
| $I_{CC3}$ | Vcc Standby Current | Vcc = Vcc Max., /CE = Vcc ± 0.5V | | 5.0 | μA |
| $V_{IL}$ | Input Low Level | | -0.5 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 0.7x Vcc | Vcc + 0.3 | V |
| $V_{ID}$ | Voltage for Electronic ID and Sector Protect | Vcc = 5.0 V | 11.5 | 12.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 12 mA, Vcc = Vcc Min. | | 0.45 | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = -2.5 mA, Vcc = Vcc Min. | 0.85x Vcc | | V |
| $V_{OH2}$ | | $I_{OH}$ = -100 μA, Vcc = Vcc Min. | Vcc -0.4 | | V |
| $V_{LKO}$ | Low Vcc Lock-out Voltage | | 3.2 | 4.2 | V |

**Notes:**
1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 1 mA/MHz, with /OE at $V_{IH}$.
2. Icc active while Internal Algorithm (program or erase) is in progress.
3. Not 100% tested.

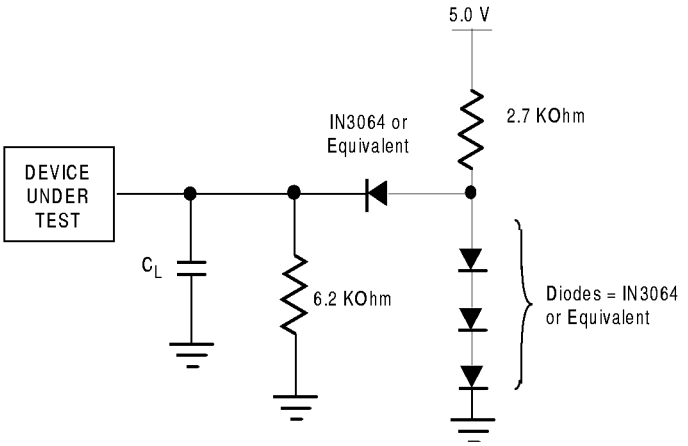
## AC CHARACTERISTICS

### Read Only Operations

| Parameter Symbol | | Description | Test Setup | | -55[1] | -70[2] | -90[2] | -120[2] | - 150[2] | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | | | | | | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time[3] | | Min. | 55 | 70 | 90 | 120 | 150 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | /CE = $V_{IL}$ /OE = $V_{IL}$ | Max. | 55 | 70 | 90 | 120 | 150 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | /OE = $V_{IL}$ | Max. | 55 | 70 | 90 | 120 | 150 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | Max. | 25 | 30 | 35 | 50 | 55 | ns |
| $t_{EHQZ}$ | $t_{HZ}$ | Chip Enable to Output High Z[3,4] | | Max. | 18 | 20 | 20 | 30 | 35 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z[3,4] | | | 18 | 20 | 20 | 30 | 35 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time from Addresses, /CE or /OE, Whichever Occurs First | | Min. | 0 | 0 | 0 | 0 | 0 | ns |

**Notes:**

1. Test Conditions:
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. Test Conditions:
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. Output driver disable time.
4. Not 100% tested.




**Notes:**
1. For -55: CL = 30pF including jig capacitance.
2. For all others: CL = 100pF including jig capacitance.

**Figure 7. Test Condition**

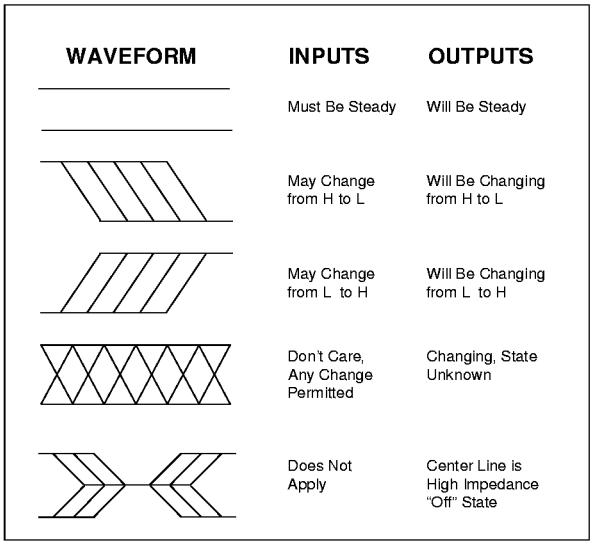
## AC CHARACTERISTICS

### Programming/Erase Operations

| Parameter Symbols | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | Description | | | -55 | -70 | -90 | -120 | -150 | Unit |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time[1] | | Min. | 55 | 70 | 90 | 120 | 150 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | | Min. | 40 | 45 | 45 | 50 | 50 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | Min. | 25 | 30 | 45 | 50 | 50 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| | $t_{OEH}$ | Output Enable Hold Time | Read[1] | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| | | | Toggle Bit & /Data Polling[1] | Min. | 10 | 10 | 10 | 10 | 10 | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recover Time Before Write | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{ELWL}$ | $t_{CS}$ | /CE Setup Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{WHEH}$ | $t_{CH}$ | /CE Hold Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | Min. | 30 | 35 | 45 | 50 | 50 | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Pulse Width High | | Min. | 20 | 20 | 20 | 20 | 20 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Byte Programming Operation | | Typ. | 7 | 7 | 7 | 7 | 7 | ms |
| | | | | Max. | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | ms |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation | | Typ. | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | sec |
| | | | | Max. | 15 | 15 | 15 | 15 | 15 | sec |
| $t_{WHWH3}$ | $t_{WHWH3}$ | Chip Erase Operation | | Typ. | 8 | 8 | 8 | 8 | 8 | sec |
| | | | | Max. | 120 | 120 | 120 | 120 | 120 | sec |
| | $t_{VCS}$ | Vcc Setup Time[1] | | Min. | 50 | 50 | 50 | 50 | 50 | ms |
| | $t_{VIDR}$ | Rise Time to $V_{ID}$[1,2] | | Min. | 500 | 500 | 500 | 500 | 500 | ns |
| | $t_{OESP}$ | /OE Setup Time to /WE Active[1,2] | | Min. | 4 | 4 | 4 | 4 | 4 | ms |
| | $t_{VLHT}$ | Voltage Transition Time[1,2] | | Min. | 4 | 4 | 4 | 4 | 4 | ms |
| | $t_{WPP1}$ | Sector Protect Write Pulse Width[2] | | Min. | 100 | 100 | 100 | 100 | 100 | ms |
| | $t_{WPP2}$ | Sector Unprotect Write Pulse Width[2] | | Min. | 10 | 10 | 10 | 10 | 10 | ms |
| | $t_{CSP}$ | /CE Setup Time to /WE Active[1, 2] | | Min. | 4 | 4 | 4 | 4 | 4 | ns |

**Notes:**
1. Not 100% tested.
2. These timings are for Sector Protect and/or Sector Unprotect operations.

## SWITCHING WAVEFORMS



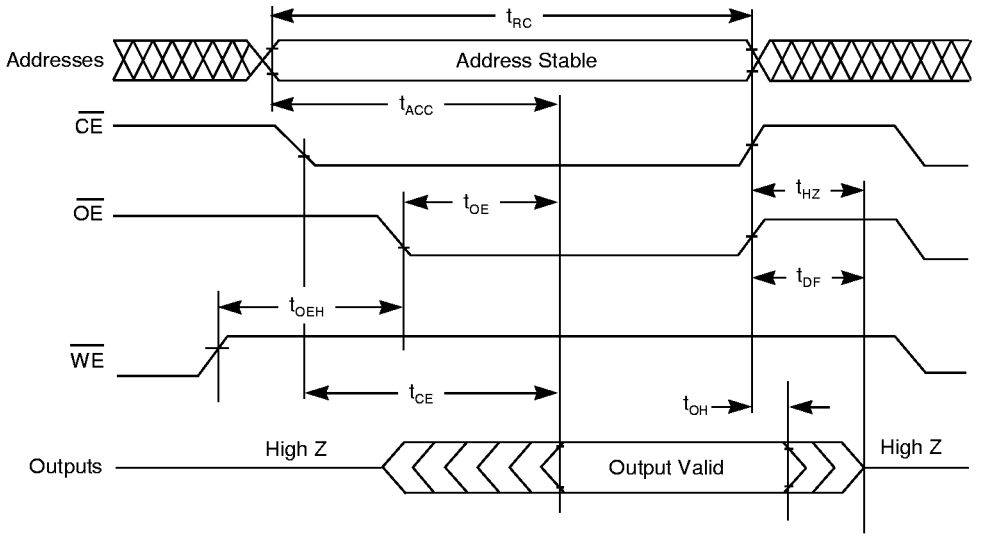
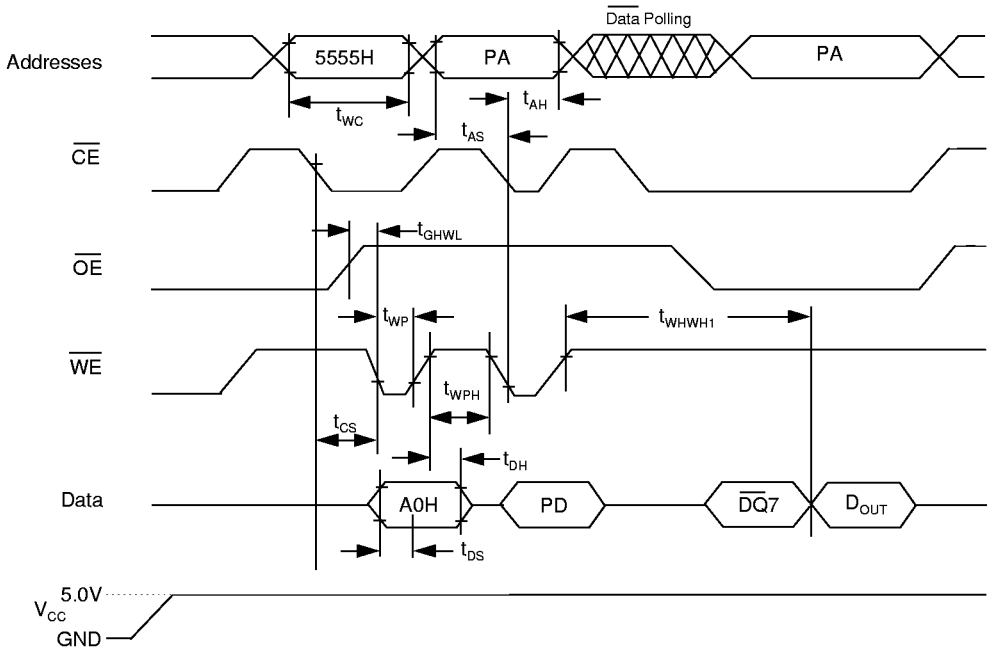




**Figure 8. AC Waveforms for Read Operations**

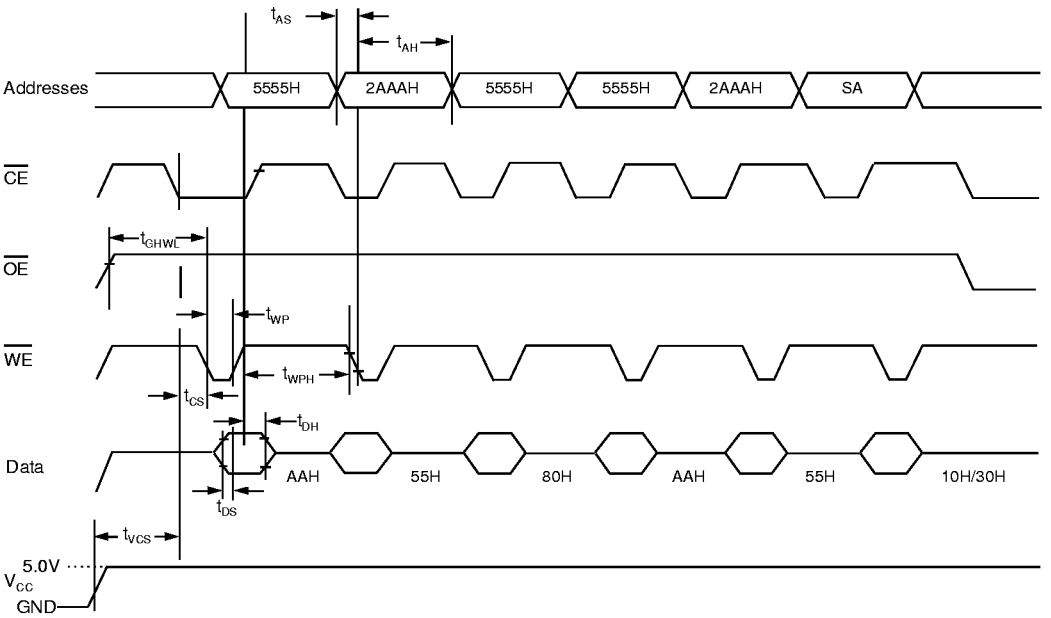
## SWITCHING WAVEFORMS




**Notes:**
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. /DQ7 is the output of the complement of the data written to the device.
4. $D_{OUT}$ is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

**Figure 9. AC Waveforms Program Operations**

## SWITCHING WAVEFORMS

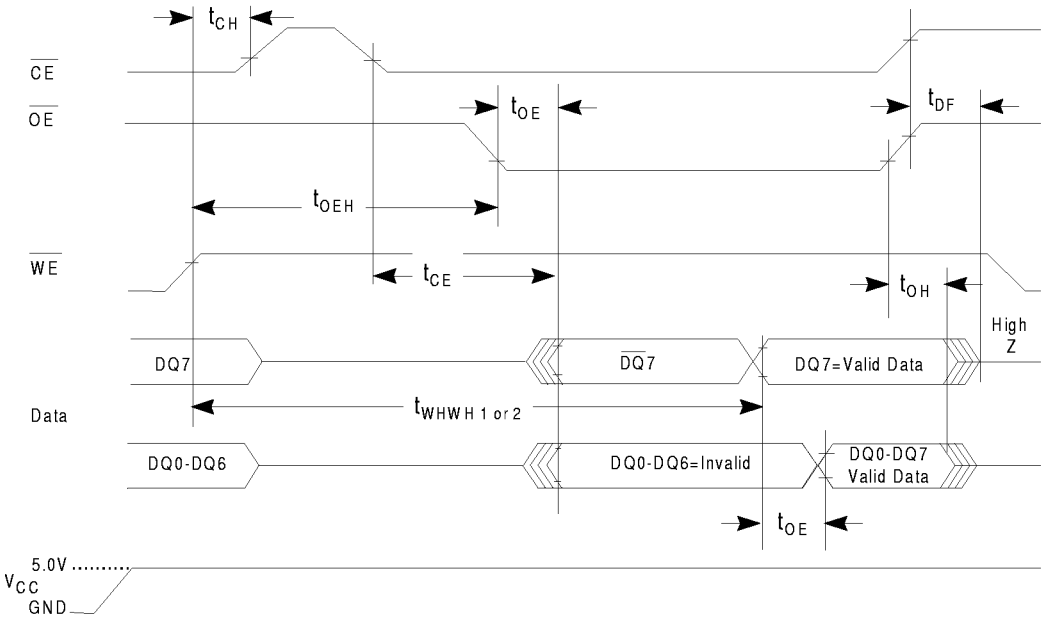



**Notes:**

1. SA is the sector address for Sector Erase. Address = X = Don't Care for Chip Erase.

**Figure 10. AC Waveforms Chip/Sector Erase Operations**

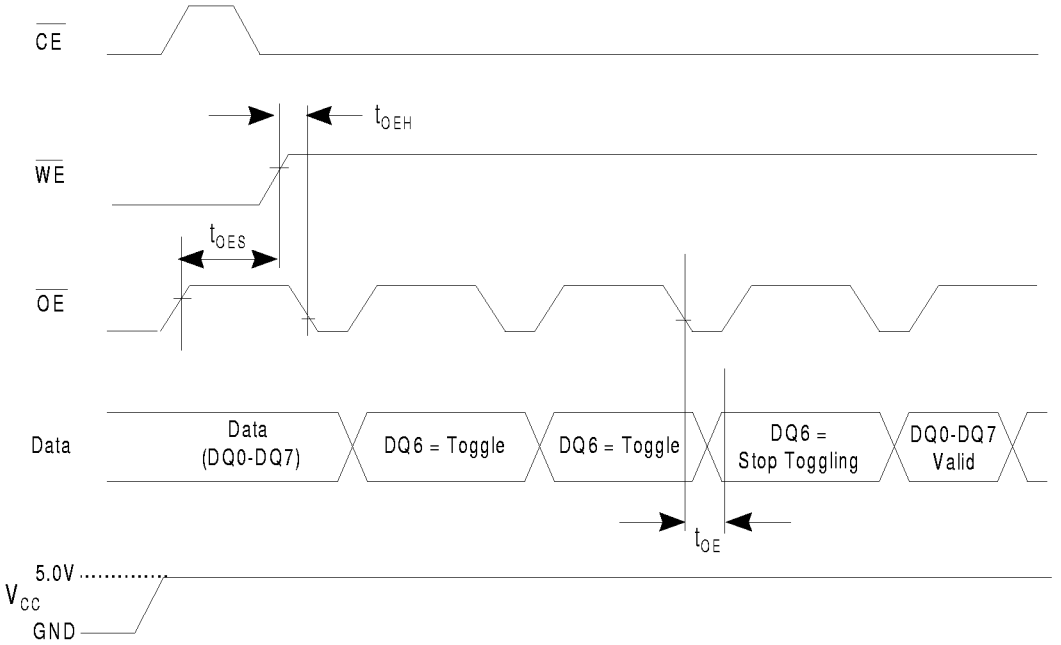
## SWITCHING WAVEFORMS




**Notes:**
1. DQ7 = Valid Data (The device has completed the internal program or erase operation.)

**Figure 11. AC Waveforms for /Data Polling during Internal Algorithm Operations**

## SWITCHING WAVEFORMS




**Notes:**

1. DQ6 stops toggling (The device has completed the internal program or erase operation)

**Figure 12. AC Waveforms for Toggle Bit during Internal Algorithm Operations**

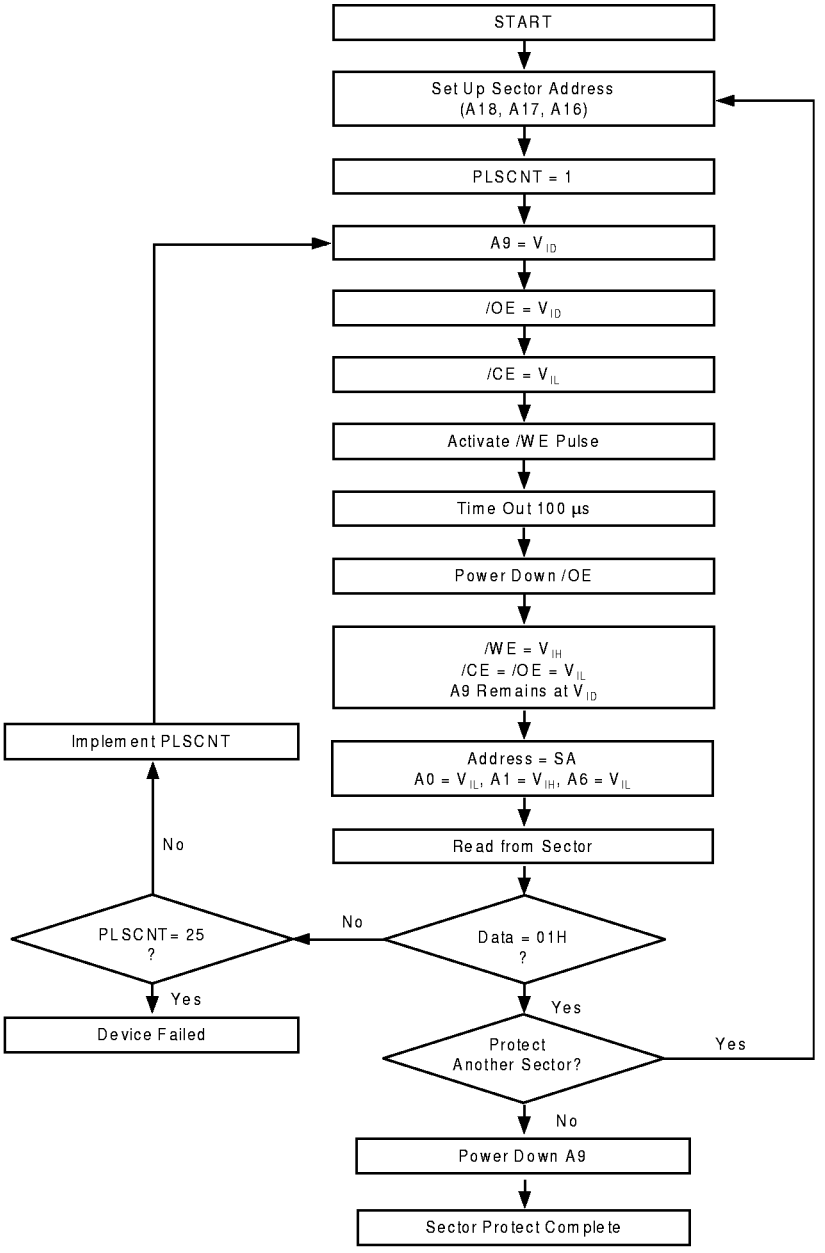
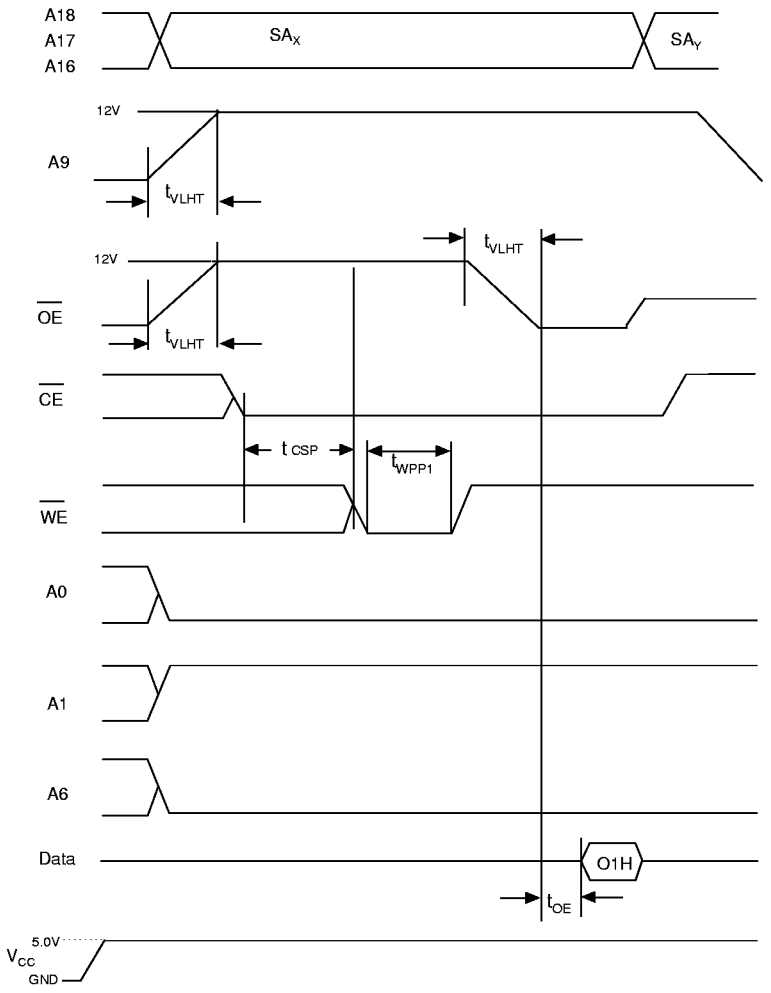


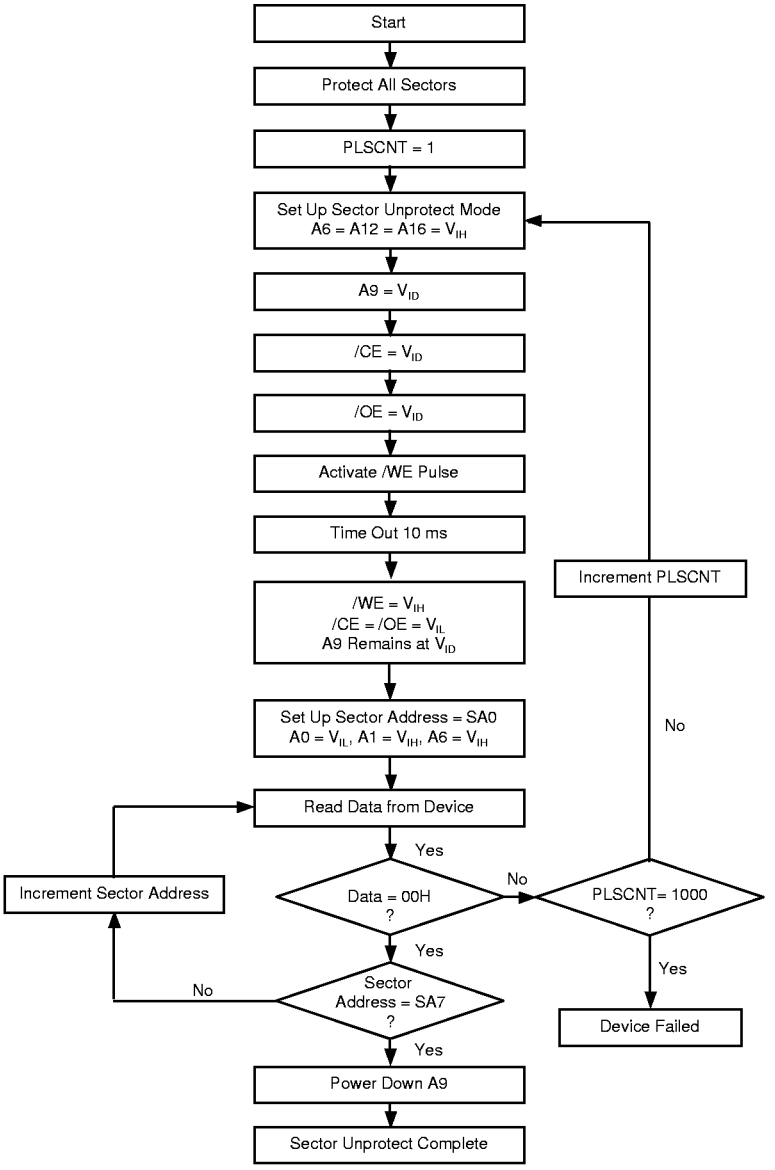

**Figure 13. Sector Protection Algorithm**

## SWITCHING WAVEFORMS




**Notes:**
1. $SA_X$ = Sector Address for initial sector
2. $SA_Y$ = Sector Address for next sector

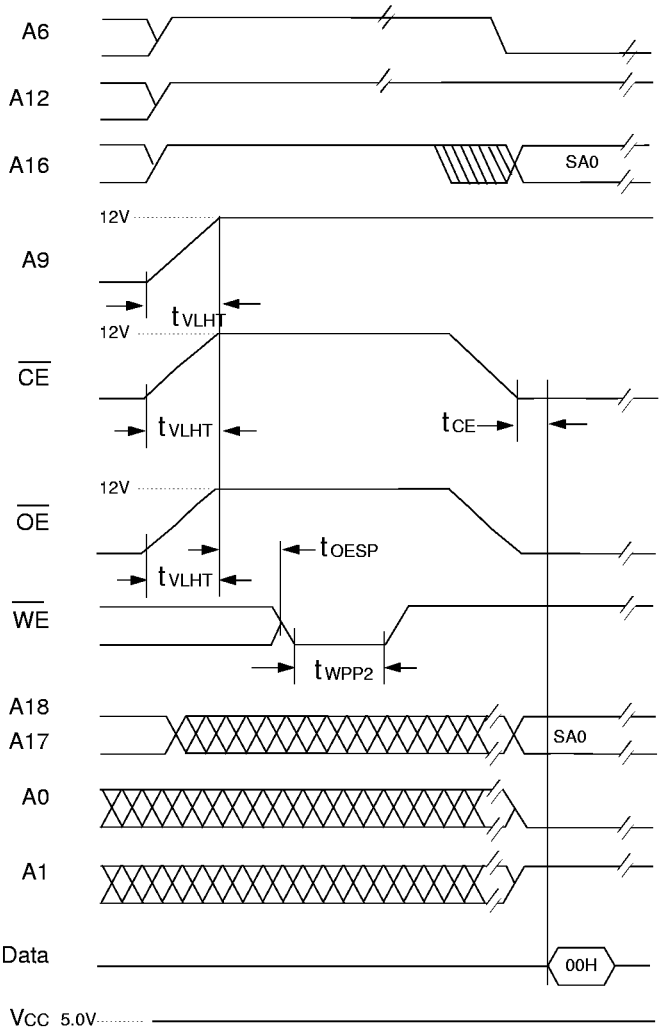
**Figure 14. AC Waveforms for Sector Protection**




**Notes:**
1. SA0 = Sector Address for initial sector
2. SA7 = Sector Address for the last sector

**Figure 15. Sector Unprotect Algorithm**

## SWITCHING WAVEFORMS




**Notes:**
1. Starts with SA0 and sequences to SA7.
2. See Figure 15 for details.

**Figure 16. AC Waveforms for Sector Unprotect**

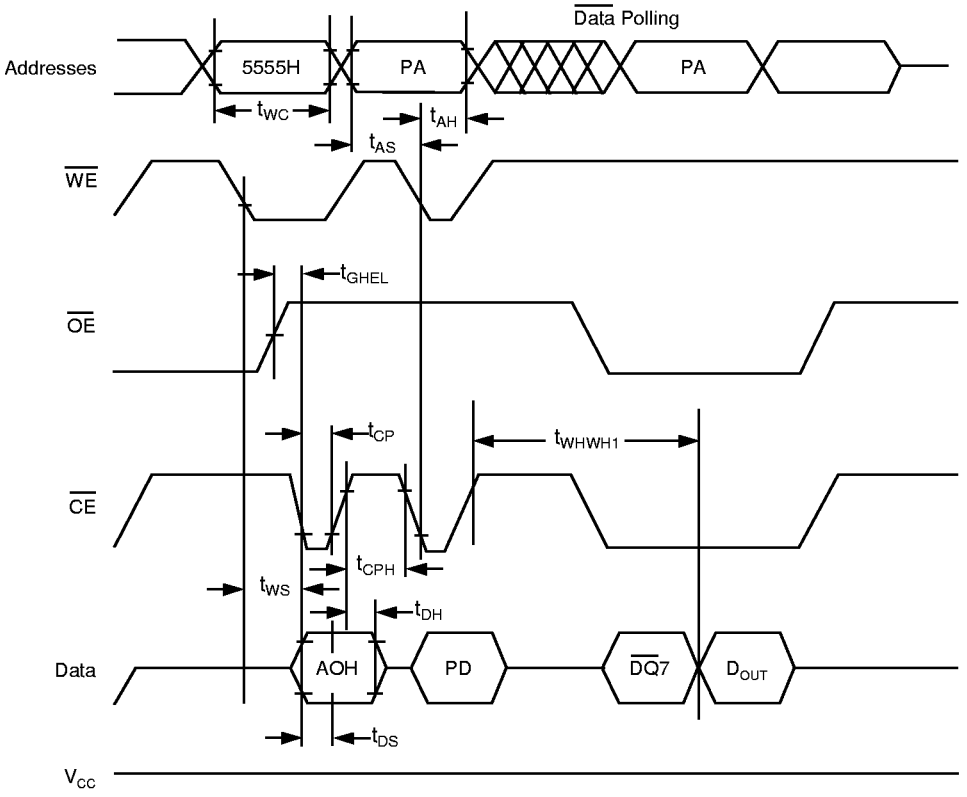
## AC CHARACTERISTICS

### Write / Erase / Program Operations
### Alternate /CE Controlled Writes

| Parameter Symbols | | Description | | | -55 | -70 | -90 | -120 | -150 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | | | | | | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time[1] | | Min. | 55 | 70 | 90 | 120 | 150 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | | Min. | 40 | 45 | 45 | 50 | 50 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time Min. | | 25 | 30 | 45 | 50 | 50 | ns | |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| | $t_{OEH}$ | Output Enable Hold Time | Read[1] | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| | | | Toggle Bit and /Data Polling[1] | Min. | 10 | 10 | 10 | 10 | 10 | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recover Time Before Write | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{WLEL}$ | $t_{WS}$ | /WE Setup Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{EHWH}$ | $t_{WH}$ | /WE Hold Time | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| $t_{ELEH}$ | $t_{CP}$ | /CE Pulse Width | | Min. | 30 | 35 | 45 | 50 | 50 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | /CE Pulse Width High | | Min. | 20 | 20 | 20 | 20 | 20 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Byte Programming Operation | | Typ. | 7 | 7 | 7 | 7 | 7 | μs |
| | | | | Max. | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | ms |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation[2] | | Typ. | 1 | 1 | 1 | 1 | 1 | sec |
| | | | | Max. | 15 | 15 | 15 | 15 | 15 | sec |
| $t_{WHWH3}$ | $t_{WHWH3}$ | Chip Erase Operation[2] | | Typ. | 8 | 8 | 8 | 8 | 8 | sec |
| | | | | Max. | 120 | 120 | 120 | 120 | 120 | sec |
| | $t_{VCS}$ | $V_{CC}$ Set Up Time[1] | | Min. | 50 | 50 | 50 | 50 | 50 | μs |
| | $t_{VIDR}$ | Rise Time to $V_{ID}$[1,2] | | Min. | 500 | 500 | 500 | 500 | 500 | ns |
| | $t_{CESP}$ | /OE Setup Time to /WE Active[1,2] | | Min. | 4 | 4 | 4 | 4 | 4 | μs |
| | $t_{VLHT}$ | Voltage Transition Time[1,2] | | Min. | 4 | 4 | 4 | 4 | 4 | μs |
| | $t_{WPP1}$ | Sector Protect Write Pulse Width[2] | | Min. | 100 | 100 | 100 | 100 | 100 | μs |
| | $t_{WPP2}$ | Sector Unprotect Write Pulse Width[2] | | Min. | 10 | 10 | 10 | 10 | 10 | ms |
| | $t_{CSP}$ | /CE Setup Time to /WE Active[1,2] | | Min. | 4 | 4 | 4 | 4 | 4 | ns |

**Notes:**
1. Not 100% tested.
2. These timings are for Sector Protect and/or Sector Unprotect operations.

## SWITCHING WAVEFORMS




**Notes:**
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. $D_{OUT}$ is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

**Figure 17. Alternate /CE Controlled Program Operation Timings**

## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Limits | | | Unit |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| Sector Erase Time | | 1.0 | 15 | sec |
| Chip Erase Time | | 8 | 120 | sec |
| Byte Programming Time | | 7 | 1000 | ms |
| Chip Programming Time | | 7 | 25 | sec |
| Erase/Program Cycles | 100,000 | 1,000,000 | | cycles |

## LATCH UP CHARACTERISTICS

| Parameter | Min. | Max. |
|---|---|---|
| Input Voltage with respect to Vss on all I/O pins | -1.0V | Vcc + 1.0V |
| Vcc Current | -100 mA | + 100 mA |

Notes:
1. Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.

## PDIP PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 8 | 12 | pF |

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 Mhz

## PLCC PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 8 | 12 | pF |

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 Mhz

## TSOP PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 7.5 | 9 | pF |

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 MHz.

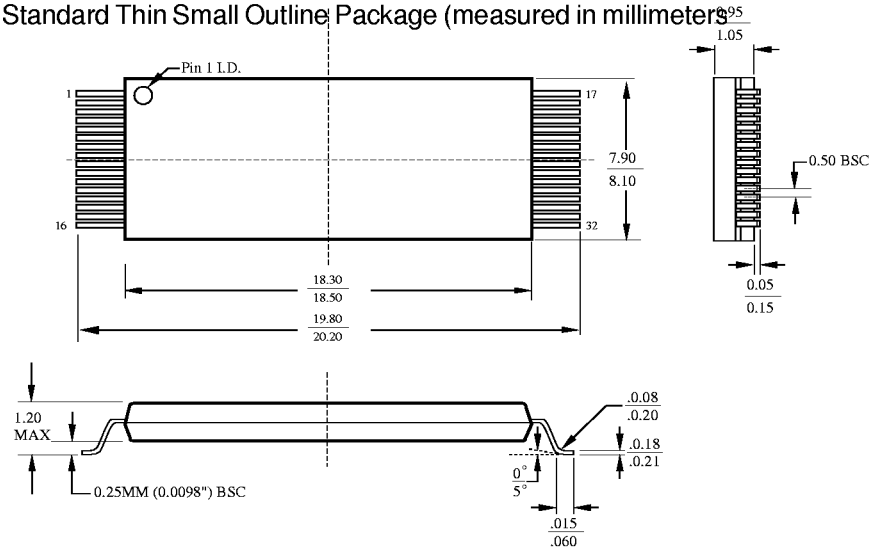
## DATA RETENTION

| Parameter | Test Conditions | Minimum | Unit |
|---|---|---|---|
| Minimum Pattern Data Retention Time | 150°C | 10 | Years |
| | 125°C | 20 | Years |

## PACKAGE DRAWINGS - Physical Dimensions

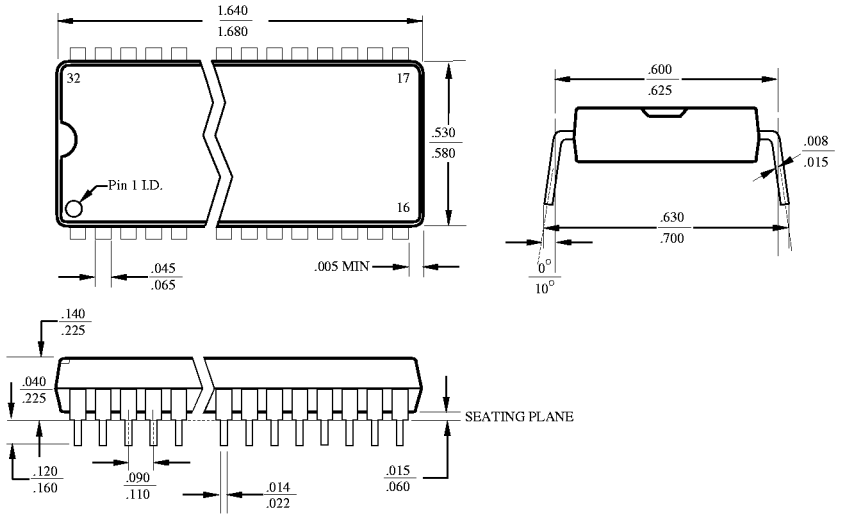
### TSOP32

32-Pin Standard Thin Small Outline Package (measured in millimeters)




### PDIP32

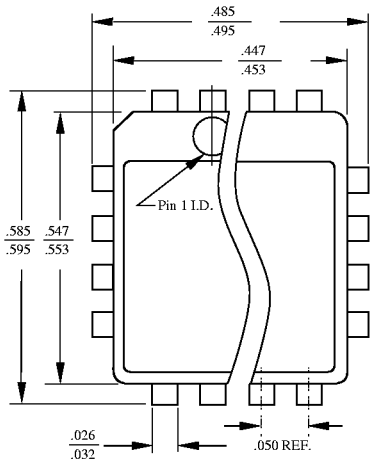
32-Pin Plastic DIP (measured in inches)



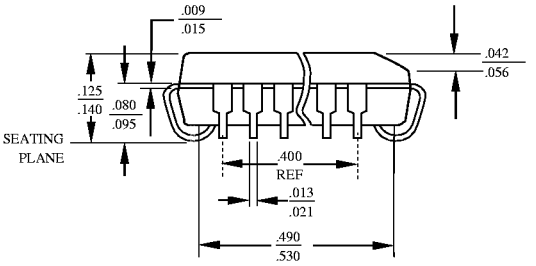
## PACKAGE DRAWINGS - Physical Dimensions

### PLCC32

32-Pin Plastic Leaded Chip Carrier (measured in inches)



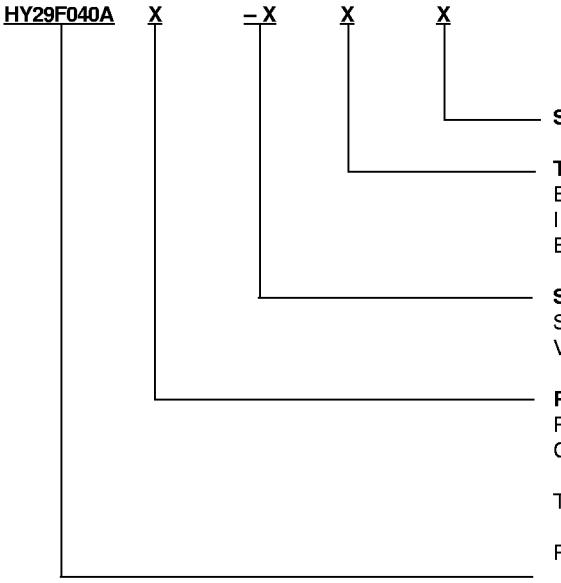

TOP VIEW




SIDE VIEW

## ORDERING INFORMATION

Hyundai products are available in several packages and operating ranges.
The order number (Valid Combination) is formed by a combination of the following:




**SPECIAL INSTRUCTIONS**

**TEMPERATURE RANGE**
Blank = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

**SPEED OPTION**
See Product Selector Guide and Valid Combinations

**PACKAGE TYPE**
P = 32-Pin Plastic DIP (PDIP)
C = 32-Pin Rectangular Plasteic Leaded Chip Carrier (PLCC)
T = 32-Pin Thin Small Outline Package (TSOP) Standard Pinout
R = 32-Pin Thin Small Outline Package (TSOP) Reverse Pinout

**DEVICE NUMBER/DESCRIPTION**
HY29F040A
4 Megabit (512K x 8-Bit) CMOS 5.0 volt-only. Sector Erase Flash Memory.

| VALID COMBINATIONS | |
|---|---|
| 55ns | P-55, C-55, T-55, R-55<br>P-55I, C-55I, T-55I, R-55I<br>P-55E, C-55E, T-55E, R-55E |
| 70ns | P-70, C-70, T-70, R-70<br>P-70I, C-70I, T-70I, R-70I<br>P-70E, C-70E, T-70E, R-70E |
| 90ns | P-90, C-90, T-90, R-90<br>P-90I, C-90I, T-90I, R-90I<br>P-90E, C-90E, T-90E, R-90E |
| 120ns | P-12, C-12, T-12, R-12<br>P-12I, C-12I, T-12I, R-12I<br>P-12E, C-12E, T-12E, R-12E |
| 150ns | P-15, C-15, T-15, R-15<br>P-15I, C-15I, T-15I, R-15I<br>P-15E, C-15E, T-15E, R-15E |

**VALID COMBINATIONS**
Valid Combinations List configurations planned to be supported in volume for this device. Consult the local Hyundai sales office to confirm availability of specific valid combinations and to check on newly released combinations.