4Mb Late Write HSTL High Speed Synchronous SRAMs (128K x 36 or 256K x 18 Organization) **Preliminary**

Description

The CXK77B3640A (organized as 131,072 words by 36 bits) and the CXK77B1840A (organized as 262,144 words by 18 bits) are high speed BiCMOS synchronous static RAMs with common I/O pins. These synchronous SRAMs integrate input registers, high speed RAM, output registers/latches, and a one-deep write buffer onto a single monolithic IC. Four distinct read operation protocols, Register - Register (R-R), Register - Latch (R-L), Register - Flow Thru (R-FT), and Dual Clock (DC), and one write operation protocol, Late Write (LW), are supported, providing a flexible, high-performance user interface.

All address, data, and control input signals except $\overline{G}$ (Output Enable) and ZZ (Sleep Mode) are registered on the positive edge of K clock. Read operation protocol is selectable through external mode pins M1 and M2.

Write operations are internally self-timed, eliminating the need for complex off-chip write pulse generation. In Register - Latch and Register - Flow Thru modes, when $\overline{SW}$ (Global Write Enable) is driven active, the subsequent positive edge of K clock tri-states the SRAM's output drivers immediately, allowing Read-Write-Read operations to be initiated consecutively, with no dead cycles between them.

The output drivers are series terminated, and the output impedance is programmable through an external impedance matching resistor RQ. By connecting RQ between ZQ and V_{SS}, the output impedance of all DQ pins can be precisely controlled.

Sleep (power down) mode control is provided through the asynchronous ZZ input. 270 MHz operation is obtained from a single 3.3V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

Features

• Fast Cycle / Access Time	R-R Mode t_{KHKH} / t_{KHQV}	R-L, R-FT Modes t_{KHKH} / t_{KHQV}	**DC Mode** t_{KHKH} / t_{KHQV}
-37	3.45ns / 2.25ns	4.8ns / 4.6ns	3.7ns / 4.9ns
-38	3.8ns / 2.25ns	4.8ns / 4.8ns	3.8ns / 4.9ns
-4	3.8ns / 2.25ns	5.2ns / 5.2ns	4.0ns / 5.2ns
-45	5.0ns / 2.50ns	6.0ns / 6.0ns	4.5ns / 6.0ns

Note: Contact Sony Memory Marketing for availability of DC mode functionality in CXK77B1840A.

- Single 3.3V power supply (V_{DD}): 3.3V ± 5%
- Register - Register (R-R), Register - Latch (R-L), Register - Flow Thru (R-FT), or Dual Clock (DC) read operations
- Read operation protocol selectable via dedicated mode pins (M1, M2)
- Fully coherent, late write, self-timed write operations
- Byte Write capability
- Differential input clocks (K/$\overline{K}$, C/$\overline{C}$)
- Asynchronous output enable ($\overline{G}$)
- Dedicated output supply voltage (V_{DDQ}): 1.5V typical, 2.0V maximum
- HSTL-compatible I/O interface with dedicated input reference voltage (V_{REF}): 0.75V typical
- Programmable impedance output drivers
- Sleep (power down) mode via dedicated mode pin (ZZ)
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 119 pin (7x17), 1.27mm pitch, 14mm x 22mm Plastic Ball Grid Array (PBGA) package

128K x 36 Pin Assignment (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA6	SA7	NC	SA3	SA2	V_{DDQ}
B	NC	NC (3)	SA8	NC	SA4	NC (2)	NC
C	NC	SA12	SA5	V_{DD}	SA0	SA13	NC
D	DQ7c	DQ8c	V_{SS}	ZQ	V_{SS}	DQ8b	DQ7b
E	DQ5c	DQ6c	V_{SS}	$\overline{SS}$	V_{SS}	DQ6b	DQ5b
F	V_{DDQ}	DQ4c	V_{SS}	$\overline{G}$	V_{SS}	DQ4b	V_{DDQ}
G	DQ2c	DQ3c	$\overline{SBW}$c	$\overline{C}$	$\overline{SBW}$b	DQ3b	DQ2b
H	DQ0c	DQ1c	V_{SS}	C	V_{SS}	DQ1b	DQ0b
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ0d	DQ1d	V_{SS}	K	V_{SS}	DQ1a	DQ0a
L	DQ2d	DQ3d	$\overline{SBW}$d	$\overline{K}$	$\overline{SBW}$a	DQ3a	DQ2a
M	V_{DDQ}	DQ4d	V_{SS}	$\overline{SW}$	V_{SS}	DQ4a	V_{DDQ}
N	DQ5d	DQ6d	V_{SS}	SA14	V_{SS}	DQ6a	DQ5a
P	DQ7d	DQ8d	V_{SS}	SA11	V_{SS}	DQ8a	DQ7a
R	NC	SA10	M1	V_{DD}	M2	SA15	NC
T	NC	NC (1)	SA9	SA16	SA1	NC (1)	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Notes:

1. Pad Locations 2T and 6T are true no-connects. However, they are defined as SA address inputs in x18 LW SRAMs.
2. Pad Location 6B is a true no-connect. However, it is defined as an SA address input in 8Mb and 16Mb LW SRAMs.
3. Pad Location 2B is a true no-connect. However, it is defined as an SA address input in 16Mb LW SRAMs.

256K x 18 Pin Assignment (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA6	SA7	NC	SA3	SA2	V_{DDQ}
B	NC	NC (3)	SA8	NC	SA4	NC (2)	NC
C	NC	SA12	SA5	V_{DD}	SA0	SA13	NC
D	DQ0b	NC (1b)	V_{SS}	ZQ	V_{SS}	DQ8a	NC (1b)
E	NC (1b)	DQ1b	V_{SS}	$\overline{SS}$	V_{SS}	NC (1b)	DQ7a
F	V_{DDQ}	NC (1b)	V_{SS}	$\overline{G}$	V_{SS}	DQ6a	V_{DDQ}
G	NC (1b)	DQ2b	$\overline{SBW}$b	$\overline{C}$	V_{SS}	NC (1b)	DQ5a
H	DQ3b	NC (1b)	V_{SS}	C	V_{SS}	DQ4a	NC (1b)
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC (1b)	DQ4b	V_{SS}	K	V_{SS}	NC (1b)	DQ3a
L	DQ5b	NC (1b)	V_{SS}	$\overline{K}$	$\overline{SBW}$a	DQ2a	NC (1b)
M	V_{DDQ}	DQ6b	V_{SS}	$\overline{SW}$	V_{SS}	NC (1b)	V_{DDQ}
N	DQ7b	NC (1b)	V_{SS}	SA14	V_{SS}	DQ1a	NC (1b)
P	NC (1b)	DQ8b	V_{SS}	SA11	V_{SS}	NC (1b)	DQ0a
R	NC	SA10	M1	V_{DD}	M2	SA15	NC
T	NC	SA17	SA9	NC (1a)	SA1	SA16	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Notes:

1a. Pad Location 4T is a true no-connect. However, it is defined as an SA address input in x36 LW SRAMs.

1b. Pad Locations 2D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, and 6P are true no-connects. However, they are defined as DQ data inputs / outputs in x36 LW SRAMs.

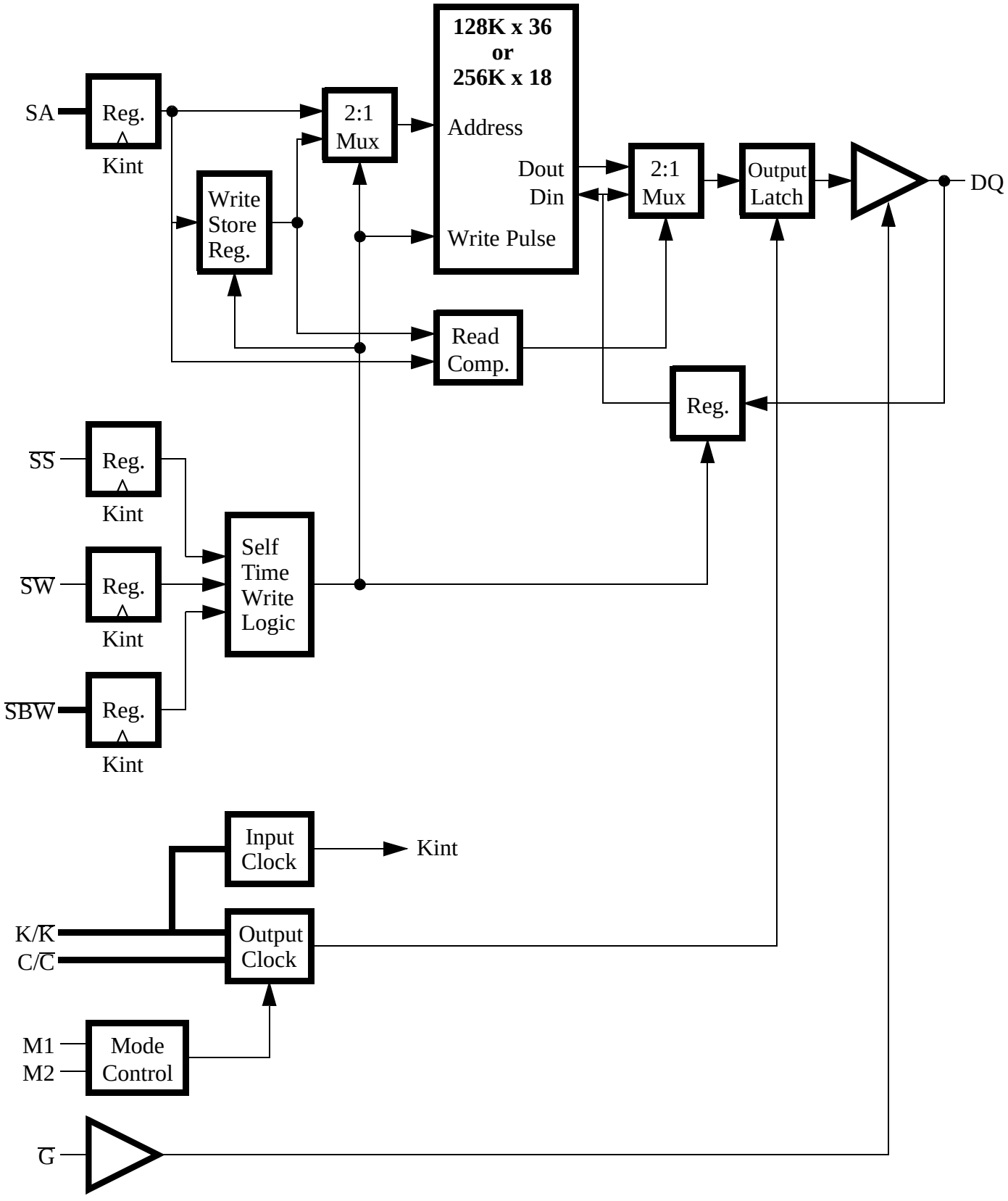
2. Pad Location 6B is a true no-connect. However, it is defined as an SA address input in 8Mb and 16Mb LW SRAMs.

3. Pad Location 2B is a true no-connect. However, it is defined as an SA address input in 16Mb LW SRAMs.

Pin Description

Symbol	Type	Description
SA	Input	Synchronous Address Inputs - Registered on the rising edge of K.
DQa, DQb DQc, DQd	I/O	Synchronous Data Inputs / Outputs - Registered on the rising edge of K during write operations. DQa - indicates Data Byte a DQb - indicates Data Byte b DQc - indicates Data Byte c DQd - indicates Data Byte d
K, $\overline{K}$	Input	Differential Input Clocks
C, $\overline{C}$	Input	Differential Output Control Clocks - For Dual-Clock read operations only.
$\overline{SS}$	Input	Synchronous Select Input - Registered on the rising edge of K. $\overline{SS}$ = 0 specifies a Write Operation when $\overline{SW}$ = 0 specifies a Read Operation when $\overline{SW}$ = 1 $\overline{SS}$ = 1 specifies a Deselect Operation
$\overline{SW}$	Input	Synchronous Global Write Enable Input - Registered on the rising edge of K. $\overline{SW}$ = 0 specifies a Write Operation when $\overline{SS}$ = 0 $\overline{SW}$ = 1 specifies a Read Operation when $\overline{SS}$ = 0
$\overline{SBW}$a, $\overline{SBW}$b, $\overline{SBW}$c, $\overline{SBW}$d	Input	Synchronous Byte Write Enable Inputs - Registered on the rising edge of K. $\overline{SBW}$a = 0 specifies write Data Byte a when $\overline{SS}$ = 0 and $\overline{SW}$ = 0 $\overline{SBW}$b = 0 specifies write Data Byte b when $\overline{SS}$ = 0 and $\overline{SW}$ = 0 $\overline{SBW}$c = 0 specifies write Data Byte c when $\overline{SS}$ = 0 and $\overline{SW}$ = 0 $\overline{SBW}$d = 0 specifies write Data Byte d when $\overline{SS}$ = 0 and $\overline{SW}$ = 0
$\overline{G}$	Input	Asynchronous Output Enable Input - De-asserted (high) forces the data output drivers to Hi-Z.
ZZ	Input	Asynchronous Sleep Mode Input - Asserted (high) forces the SRAM into low-power mode.
M1, M2	Input	Read Operation Protocol Select - These mode pins must be tied to V_{DD} or V_{SS} before power-up. M1:M2 = 00 specifies Register - Flow Thru Read Operations M1:M2 = 01 specifies Register - Register Read Operations M1:M2 = 10 specifies Register - Latch Read Operations M1:M2 = 11 specifies Dual Clock Read Operations
ZQ	Input	Output Impedance Control Resistor Input
V_{DD}		3.3V Core Power Supply - Core supply voltage.
V_{DDQ}		Output Power Supply - Output buffer supply voltage.
V_{REF}		Input Reference Voltage - Input buffer threshold voltage.
V_{SS}		Ground
TCK	Input	JTAG Clock
TMS	Input	JTAG Mode Select
TDI	Input	JTAG Data In
TDO	Output	JTAG Data Out
NC		No Connect - These pins are true no-connects, i.e. there is no internal chip connection to these pins. They can be left unconnected or tied directly to V_{DD} or V_{SS}.

BLOCK DIAGRAM



•Truth Tables

Register - Register Mode

ZZ	$\overline{SS}$ (t_n)	$\overline{SW}$ (t_n)	$\overline{SBW}$x (t_n)	$\overline{G}$	Mode	DQ (t_n)	DQ (t_{n+1})	V_{DD} Current
H	X	X	X	X	Sleep (Power Down) Mode	Hi - Z	Hi - Z	I_{SB}
L	H	X	X	X	Deselect	X	Hi - Z	I_{DD}
L	L	H	X	H	Read	Hi - Z	Hi - Z	I_{DD}
L	L	H	X	L	Read	X	$Q(t_n)$	I_{DD}
L	L	L	L	X	Write All Bytes	X	$D(t_n)$	I_{DD}
L	L	L	X	X	Write Bytes With $\overline{SBW}$x = L	X	$D(t_n)$	I_{DD}
L	L	L	H	X	Abort Write	X	Hi - Z	I_{DD}

Register - Latch and Register - Flow Thru Mode

ZZ	$\overline{SS}$ (t_n)	$\overline{SW}$ (t_n)	$\overline{SBW}$x (t_n)	$\overline{G}$	Mode	DQ (t_n)	DQ (t_{n+1})	V_{DD} Current
H	X	X	X	X	Sleep (Power Down) Mode	Hi - Z	Hi - Z	I_{SB}
L	H	X	X	X	Deselect	Hi - Z	X	I_{DD}
L	L	H	X	H	Read	Hi - Z	Hi - Z	I_{DD}
L	L	H	X	L	Read	$Q(t_n)$	X	I_{DD}
L	L	L	L	X	Write All Bytes	Hi - Z	$D(t_n)$	I_{DD}
L	L	L	X	X	Write Bytes With $\overline{SBW}$x = L	Hi - Z	$D(t_n)$	I_{DD}
L	L	L	H	X	Abort Write	Hi - Z	X	I_{DD}

Dual Clock Mode

ZZ	$\overline{SS}$ (t_n)	$\overline{SW}$ (t_n)	$\overline{SBW}$x (t_n)	$\overline{G}$	Mode	DQ (t_n)	DQ (t_{n+1})	V_{DD} Current
H	X	X	X	X	Sleep (Power Down) Mode	Hi - Z	Hi - Z	I_{SB}
L	H	X	X	X	Deselect	Hi - Z	X	I_{DD}
L	L	H	X	H	Read	Hi - Z	Hi - Z	I_{DD}
L	L	H	X	L	Read	$Q(t_n)$	X	I_{DD}
L	L	L	L	X	Write All Bytes	Hi - Z	$D(t_n)$	I_{DD}
L	L	L	X	X	Write Bytes With $\overline{SBW}$x = L	Hi - Z	$D(t_n)$	I_{DD}
L	L	L	H	X	Abort Write	Hi - Z	Hi - Z	I_{DD}

•Read Operations

These devices support four distinct JEDEC standard read protocols via mode pins M1 and M2. The mode pins must be set during power-up, and cannot change during SRAM operation.

Mode Select Truth Table.

	M1	M2
Register - Register	L	H
Register - Flow Thru	L	L
Register - Latch	H	L
Dual Clock	H	H

When a read operation is initiated, all address and control signals (except $\overline{G}$ and ZZ) are latched into input registers on the rising edge of K clock. The latched address is decoded and then used to access a particular location in the internal memory array. These two events occur regardless which read protocol is selected. After the memory location is accessed, the read protocol determines when data from that memory location is driven valid externally.

Register - Register Mode

In Register - Register mode, data is driven valid externally from the subsequent rising edge of K clock, one full K clock cycle after the address is latched. Data remains valid until at least the next rising edge of K clock, one full K clock cycle thereafter.

Register - Latch Mode

In Register - Latch mode, data is driven valid externally from the subsequent falling edge of K clock, or, some minimum amount of time after the address is latched (determined by the access time of the memory array), whichever is greater. Data remains valid until at least the next falling edge of K clock, approximately one full K clock cycle thereafter.

Register - Flow Thru Mode

In Register - Flow Thru mode, data is driven valid immediately, some minimum amount of time after the address is latched (determined by the access time of the memory array). Data remains valid until at least the next rising edge of K clock, approximately one full K clock cycle thereafter.

Dual Clock Mode

In Dual Clock mode, data is driven valid from the subsequent rising edge of C clock, or, some minimum amount of time after the address is latched (determined by the access time of the memory array), whichever is greater. Data remains valid until at least the next rising edge of C clock, approximately one full C clock cycle thereafter.

Regardless which read protocol is selected, read operations may be initiated consecutively, with no dead cycles between them.

•Write Operations

These devices follow a Late Write protocol, where, during a write operation, data is provided to the SRAM one clock cycle after the address and control signals, eliminating the need for one of the bus-turnaround cycles required when changing from a read to a write operation. The Late Write function is controlled internally by using a dedicated one-deep write buffer to store the address and data signals associated with the current write operation. The buffered data is not actually written to the memory array until the next write operation is initiated.

When a write operation is initiated, all address and control signals (except $\overline{G}$ and ZZ) are latched into input registers on the rising edge of K clock. Also at this time, any valid data currently stored in the one-deep write buffer (associated with the previous write operation) is written to the memory array. On the subsequent rising edge of K clock, the data and address signals for the current write operation are stored in the write buffer. This write pipeline mechanism allows write operations to be initiated consecutively, with no dead cycles between them.

Note: In order to maintain coherency, if a read operation is initiated to the same address as that of the last write operation (i.e. to the address of the write operation currently stored in the write buffer), read data is provided from the write buffer instead of the memory array. If only some of the bytes of data in the write buffer are valid, those bytes of data that are valid are provided from the write buffer, and those bytes of data that are invalid are provided from the memory array.

•Sleep (Power Down) Mode

Sleep (power down) mode is provided through the asynchronous input signal ZZ. When ZZ is asserted (high), the output drivers will go to a Hi-Z state, and the SRAM will begin to draw standby current. Contents of the memory array will be preserved. An enable time (t_{ZZE}) must be met before the SRAM is guaranteed to be in sleep mode, and a recovery time (t_{ZZR}) must be met before the SRAM can resume normal operation.

•Power-Up Sequence

Power supplies must power up in the following sequence: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, and Inputs. V_{DDQ} must never exceed V_{DD}.

•Programmable Impedance Output Drivers

These devices have programmable impedance output drivers. The output impedance is controlled by an external resistor, RQ, connected between the SRAM's ZQ pin and V_{SS}, and is equal to one-fifth the value of this resistor. For output impedance matching within a ±7.5% tolerance, RQ must be in the range of 100Ω to 200Ω. For maximum output drive, the ZQ pin can be connected directly to V_{SS}. For minimum output drive, the ZQ pin can be left open or connected to V_{DDQ}. The output impedance is updated whenever the output drivers are in a Hi-Z state. At power up, 8192 clock cycles followed by a write or deselect operation are required to ensure that the output impedance has reached its desired value. After power up, periodic updates of the output impedance, via a write or deselect operation, are also required to ensure that the output impedance remains within a ±7.5% tolerance.

•Absolute Maximum Ratings(1)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5 to +4.6	V
Output Supply Voltage	V_{DDQ}	-0.5 to +4.6	V
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5 (4.6V max.)	V
Output Voltage	V_{OUT}	-0.5 to V_{DDQ}+0.5 (4.6V max.)	V
Operating Temperature	T_A	0 to 85	°C
Junction Temperature	T_J	0 to 110	°C
Storage Temperature	T_{STG}	-55 to 150	°C

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

•PBGA Package Thermal Characteristics

		Sample Form	Ambient	Air Flow (m/s)	Thermal Resistance (°C/W)	Reference
1	θ_{JA}	PKG only	Room Temp	0 1 2 3	81.0 36.9 29.5 26.1	Max Thermal Resistance
2	θ_{JA}	PKG on Board A*	Room Temp	0 1 2 3	32.4 23.8 20.7 18.6	*Board A is a two layer printed circuit board with very low density trace in both layers.
3	θ_{JA}	PKG on Board B**	Room Temp	0 1 2 3	16.0 12.9 12.0 11.3	**Board B is a four layer printed circuit board, same as Board A except with two GND planes in the middle layers.
4	θ_{JC}	PKG only	DI Water	-	3.6	Min Thermal Resistance

Board size & thickness (Board A, B): 7.62W x 11.43L x 1.57T (mm)

•DC Recommended Operating Conditions

(V_{SS} = 0V, T_A = 0 to 85°C)

Item		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{DD}	3.13	3.3	3.47	V
Output Supply Voltage(1)		V_{DDQ}	1.4	---	1.6	V
Input	Reference Voltage	V_{REF}	0.5	---	1.0	V
	High Voltage(2)	V_{IH}	V_{REF} + 0.2	---	V_{DD} + 0.3	V
	Low Voltage(3)	V_{IL}	-0.3	---	V_{REF} - 0.2	V
Clock(4) Input	Signal Voltage	V_{KIN}	-0.3	---	V_{DD} + 0.3	V
	Differential Voltage	V_{DIF}	0.4	---	V_{DD} + 0.6	V
	Common Mode Voltage	V_{CM}	0.5	0.75	1.1	V
	Cross Point Voltage	V_X	0.6	0.75	1.0	V
B-Scan Input	Input High Voltage(5)	V_{TIHSC}	2.0	---	V_{DD} + 0.3	V
	Input Low Voltage(5)	V_{TILSC}	-0.3	---	0.8	V
	Input High Voltage(6)	V_{TIHBS}	V_{REF} + 0.5	---	V_{DD} + 0.3	V
	Input Low Voltage(6)	V_{TILBS}	-0.3	---	V_{REF} - 0.5	V
Output Impedance Control Resistor		RQ	100	150	200	Ω

(1) Extended V_{DDQ} support up to 2.0V is available - please contact marketing.

(2) V_{IH} (Max) AC = V_{DD} + 1.5V for pulse width less than 2.0 ns.

(3) V_{IL} (Min) AC = -1.5V for pulse width less than 2.0 ns.

(4) These devices support two different input clocking schemes:

a. Differential - In this scheme, both clock inputs (K and $\overline{K}$) are driven differentially. V_{KIN}, V_{DIF}, and V_{CM} must all be considered when using this scheme.

b. Single Ended - In this scheme, one of the two clock inputs (either K or $\overline{K}$) is driven to the same voltage levels as the other inputs, i.e. from V_{SS} to V_{DDQ} nominally, while the other clock input (either $\overline{K}$ or K) is tied to an external reference voltage (V_X). V_{KIN}, V_{DIF}, and V_X must all be considered when using this scheme.

(5) Scan control (SC) signals are: TDO, TDI, TMS & TCK.

(6) BS signals are all signals in the Boundary Scan chain except the scan control (SC) signals: TDO, TDI, TMS & TCK.

•I/O Capacitance

(T_A = 25°C, f = 1 MHz)

Item	Symbol	Test conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	---	6	pF
Clock Input Capacitance	C_{CLK}	V_{IN} = 0V	---	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	---	7	pF

Note: These parameters are sampled and are not 100% tested.

•DC Electrical Characteristics

(V_{DD} = 3.3V ± 5%, V_{SS} = 0V, T_A = 0 to 85°C)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{DD}	-1	---	1	uA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{DD} $\overline{G} = V_{IH}$	-10	---	10	uA
Power Supply Operating Current - x36	$I_{DD-5.0}$ $I_{DD-4.5}$ $I_{DD-4.0}$ $I_{DD-3.7}$	I_{OUT} = 0 mA $\overline{SS} = V_{IL}$, ZZ = V_{IL}	---	655 675 700 725	---	mA
Power Supply Operating Current - x18	$I_{DD-5.0}$ $I_{DD-4.5}$ $I_{DD-4.0}$ $I_{DD-3.7}$	I_{OUT} = 0 mA $\overline{SS} = V_{IL}$, ZZ = V_{IL}	---	590 610 635 660	---	mA
Power Supply Standby Current	I_{SB}	I_{OUT} = 0 mA ZZ = V_{IH}	---	60	---	mA
Output High Voltage	V_{OH}	I_{OH} = -6.0 mA RQ = 250Ω	V_{DDQ}-0.4	---	---	V
Output Low Voltage	V_{OL}	I_{OL} = 6.0 mA RQ = 250Ω	---	---	0.4	V
Output Driver Impedance	R_{OUT}[1,2,3]	$V_{OH} = V_{DDQ}/2$ $V_{OL} = V_{DDQ}/2$	15	RQ/5	50	Ω

1. RQ needs to be in the range of 100Ω to 200Ω for proper control of the value of R_{OUT}.
   1.1 $R_{OUT} \geq 15\Omega$ when RQ ≤ 100Ω
   1.2 $R_{OUT} \leq 50\Omega$ when RQ ≥ 200Ω
2. For maximum output drive, ZQ pin can be tied directly to V_{SS}. The output impedance is as described in note 1.1.
3. For minimum output drive, ZQ pin can be no connect or tied to V_{DDQ}. The output impedance is as described in note 1.2.
4. Typical I_{DD} values measured at V_{DD}=3.3V and T_A = 25°C, with a 75% read / 25% write operation distribution.

•AC Electrical Characteristics (Register - Register Mode)

Item	Symbol	-37		-38		-4		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t_{KHKH}	3.45	---	3.8	---	3.8	---	5.0	---	ns
Clock High Pulse Width	t_{KHKL}	1.3*3	---	1.3*3	---	1.5	---	1.5	---	ns
Clock Low Pulse Width	t_{KLKH}	1.3*3	---	1.3*3	---	1.5	---	1.5	---	ns
Address Setup Time	t_{AVKH}	0.3	---	0.3	---	0.3	---	0.5	---	ns
Address Hold Time	t_{KHAX}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Write Enables Setup Time	t_{WVKH}	0.3	---	0.3	---	0.3	---	0.5	---	ns
Write Enables Hold Time	t_{KHWX}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Synchronous Select Setup Time	t_{SVKH}	0.3	---	0.3	---	0.3	---	0.5	---	ns
Synchronous Select Hold Time	t_{KHSX}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Data Input Setup Time	t_{DVKH}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Data Input Hold Time	t_{KHDX}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Clock High to Output Valid	t_{KHQV}	---	2.25	---	2.25	---	2.25	---	2.5	ns
Clock High to Output Hold	t_{KHQX}*2	0.7	---	0.7	---	0.7	---	0.7	---	ns
Clock High to Output Low-Z	t_{KHQX1}*2	0.7	---	0.7	---	0.7	---	0.7	---	ns
Clock High to Output High-Z	t_{KHQZ}*2	---	2.25	---	2.25	---	2.25	---	2.5	ns
Output Enable Low to Output Valid	t_{GLQV}	---	2.25	---	2.25	---	2.25	---	2.5	ns
Output Enable Low to Output Low-Z	t_{GLQX}*2	0.5	---	0.5	---	0.5	---	0.5	---	ns
Output Enable High to Output High-Z	t_{GHQZ}*2	---	2.25	---	2.25	---	2.25	---	2.3	ns
Sleep Mode Enable Time	t_{ZZE}*2	---	20.0	---	20.0	---	20.0	---	20.0	ns
Sleep Mode Recovery Time	t_{ZZR}*2	20.0	---	20.0	---	20.0	---	20.0		ns

1. All parameters are specified over the range T_A = 0 to 85°C.
2. These parameters are sampled and are not 100% tested.
3. These parameters are characterized but not 100% tested at 1.3ns. They are 100% tested at 1.5ns.

•AC Electrical Characteristics (Register - Latch & Register - Flow Thru Modes)

Item	Symbol	-37		-38		-4		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t_{KHKH}	4.8	---	4.8	---	5.2	---	6.0	---	ns
Clock High Pulse Width	t_{KHKL}	1.5	---	1.5	---	1.5	---	1.5	---	ns
Clock Low Pulse Width	t_{KLKH}	1.5	---	1.5	---	1.5	---	1.5	---	ns
Address Setup Time	t_{AVKH}	0.4*3	---	0.4*3	---	0.5	---	0.5	---	ns
Address Hold Time	t_{KHAX}	0.8*3	---	0.8*3	---	1.0	---	1.0	---	ns
Write Enables Setup Time	t_{WVKH}	0.4*3	---	0.4*3	---	0.5	---	0.5	---	ns
Write Enables Hold Time	t_{KHWX}	0.8*3	---	0.8*3	---	1.0	---	1.0	---	ns
Synchronous Select Setup Time	t_{SVKH}	0.4*3	---	0.4*3	---	0.5	---	0.5	---	ns
Synchronous Select Hold Time	t_{KHSX}	0.8*3	---	0.8*3	---	1.0	---	1.0	---	ns
Data Input Setup Time	t_{DVKH}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Data Input Hold Time	t_{KHDX}	0.8*3	---	0.8*3	---	1.0	---	1.0	---	ns
Clock High to Output Valid	t_{KHQV}	---	4.6	---	4.8	---	5.2	---	6.0	ns
Clock High to Output Hold (R-FT mode only)	t_{KHQX}*2	2.0	---	2.0	---	2.0	---	2.0	---	ns
Clock High to Output Low-Z (R-FT mode only)	t_{KHQX1}*2	2.5	---	2.5	---	2.5	---	3.0	---	ns
Clock Low to Output Valid (R-L mode only)	t_{KLQV}	---	2.2	---	2.2	---	2.3	---	2.5	ns
Clock Low to Output Hold (R-L mode only)	t_{KLQX}*2	0.7	---	0.7	---	0.7	---	0.7	---	ns
Clock Low to Output Low-Z (R-L mode only)	t_{KLQX1}*2	0.7	---	0.7	---	0.7	---	0.7	---	ns
Clock High to Output High-Z	t_{KHQZ}*2	---	2.1	---	2.2	---	2.3	---	2.5	ns
Output Enable Low to Output Valid	t_{GLQV}	---	2.1	---	2.2	---	2.3	---	2.5	ns
Output Enable Low to Output Low-Z	t_{GLQX}*2	0.5	---	0.5	---	0.5	---	0.5	---	ns
Output Enable High to Output High-Z	t_{GHQZ}*2	---	2.1	---	2.2	---	2.3	---	2.3	ns
Sleep Mode Enable Time	t_{ZZE}*2	---	20.0	---	20.0	---	20.0	---	20.0	ns
Sleep Mode Recovery Time	t_{ZZR}*2	20.0	---	20.0	---	20.0	---	20.0	---	ns

1. All parameters are specified over the range T_A = 0 to 85°C.
2. These parameters are sampled and are not 100% tested.
3. These parameters are measured from valid V_{IH}/V_{IL} levels to the clock mid-point.
4. R-FT mode operation is verified functionally, but associated timing parameters are guaranteed by design only and are not 100% tested.

•AC Electrical Characteristics (Dual Clock Mode)

Item	Symbol	-37		-38		-4		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
K Clock Cycle Time	t_{KHKH}	3.7	---	3.8	---	4.0	---	4.5	---	ns
K Clock High Pulse Width	t_{KHKL}	1.3*3	---	1.3*3	---	1.5	---	1.5	---	ns
K Clock Low Pulse Width	t_{KLKH}	1.3*3	---	1.3*3	---	1.5	---	1.5	---	ns
C Clock Cycle Time	t_{CHCH}	3.7	---	3.8	---	4.0	---	4.5	---	ns
C Clock High Pulse Width	t_{CHCL}	1.3*3	---	1.3*3	---	1.5	---	1.5	---	ns
C Clock Low Pulse Width	t_{CLCH}	1.3*3	---	1.3*3	---	1.5	---	1.5	---	ns
K to C Clock Delay	t_{KHCH}	1.5	---	1.5	---	1.5	---	1.5	---	ns
C to K Clock Delay	t_{CHKH}	0.8	---	0.8	---	0.8	---	0.8	---	ns
Address Setup Time	t_{AVKH}	0.5	---	0.5	---	0.5	---	0.5	---	ns
Address Hold Time	t_{KHAX}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Write Enables Setup Time	t_{WVKH}	0.5	---	0.5	---	0.5	---	0.5	---	ns
Write Enables Hold Time	t_{KHWX}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Synchronous Select Setup Time	t_{SVKH}	0.5	---	0.5	---	0.5	---	0.5	---	ns
Synchronous Select Hold Time	t_{KHSX}	1.0	---	1.0	---	1.0	---	1.0	---	ns
Data Input Setup Time	t_{DVKH}	0.5	---	0.5	---	0.5	---	0.5	---	ns
Data Input Hold Time	t_{KHDX}	0.7	---	0.7	---	0.8	---	1.0	---	ns
K Clock High to Output Valid	t_{KHQV}	---	4.9	---	4.9	---	5.2	---	6.0	ns
C Clock High to Output Valid	t_{CHQV}	---	2.1	---	2.1	---	2.3	---	2.5	ns
C Clock High to Output Hold	t_{CHQX}*2	0.7	---	0.7	---	0.7	---	0.7	---	ns
C Clock High to Output Low-Z	t_{CHQX1}*2	0.7	---	0.7	---	0.7	---	0.7	---	ns
C Clock High to Output High-Z	t_{CHQZ}*2	---	2.1	---	2.1	---	2.3	---	2.5	ns
Output Enable Low to Output Valid	t_{GLQV}	---	1.8	---	1.8	---	2.1	---	2.5	ns
Output Enable Low to Output Low-Z	t_{GLQX}*2	0.5	---	0.5	---	0.5	---	0.5	---	ns
Output Enable High to Output High-Z	t_{GHQZ}*2	---	1.8	---	1.8	---	2.0	---	2.3	ns
Sleep Mode Enable Time	t_{ZZE}*2	---	20.0	---	20.0	---	20.0	---	20.0	ns
Sleep Mode Recovery Time	t_{ZZR}*2	20.0	---	20.0	---	20.0	---	20.0	---	ns

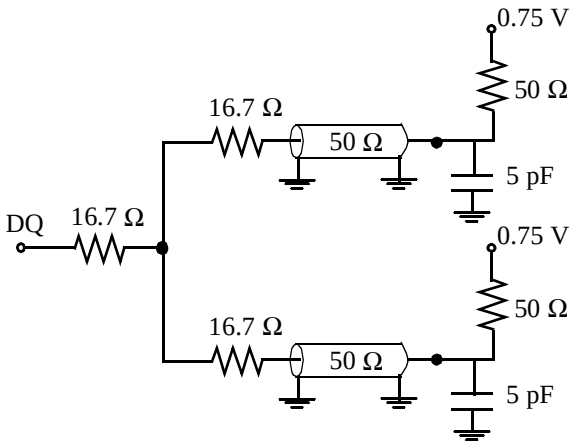
1. All parameters are specified over the range T_A = 0 to 85°C.
2. These parameters are sampled and are not 100% tested.
3. These parameters are characterized but not 100% tested at 1.3ns. They are 100% tested at 1.5ns.
4. DC mode operation and timing parameters are tested in the CXK77B3640A only.

•AC Test Conditions (V_{DDQ} = 1.5V)

(V_{DD} = 3.3V ± 5%, V_{DDQ} = 1.5V, T_A = 0 to 85°C)

Item	Symbol	Conditions	Units	Notes
Input Reference Voltage	V_{REF}	0.75	V	
Input High Level	V_{IH}	1.25	V	
Input Low Level	V_{IL}	0.25	V	
Input Rise & Fall Time		1.0	V/ns	
Input Reference Level		0.75	V	
Clock Input High Voltage	V_{KIH}	1.25	V	$V_{DIF} \geq 0.5V$
Clock Input Low Voltage	V_{KIL}	0.25	V	$V_{DIF} \geq 0.5V$
Clock Input Common Mode Voltage	V_{CM}	0.75	V	
Clock Input Rise & Fall Time		1.0	V/ns	
Clock Input Reference Level		K/$\overline{K}$ cross; C/$\overline{C}$ cross	V	
Output Reference Level		0.75	V	
Output Load Conditions				Fig.1 RQ = 250Ω

Fig. 1: AC Test Output Load (V_{DDQ} = 1.5V)

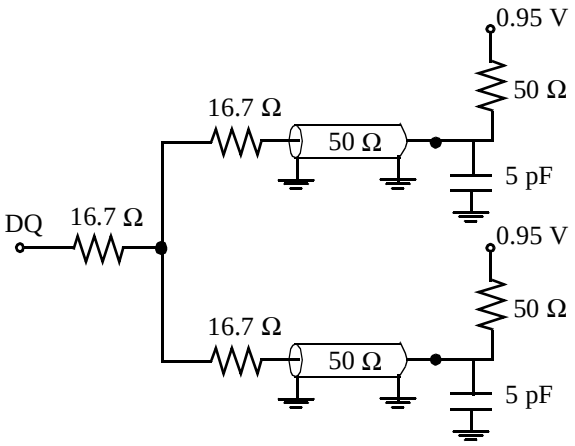


•AC Test Conditions (V_{DDQ} = 1.9V) .... for extended HSTL (R-L mode only)

(V_{DD} = 3.3V ± 5%, V_{DDQ} = 1.9V ± 0.1V, T_A = 0 to 85°C)

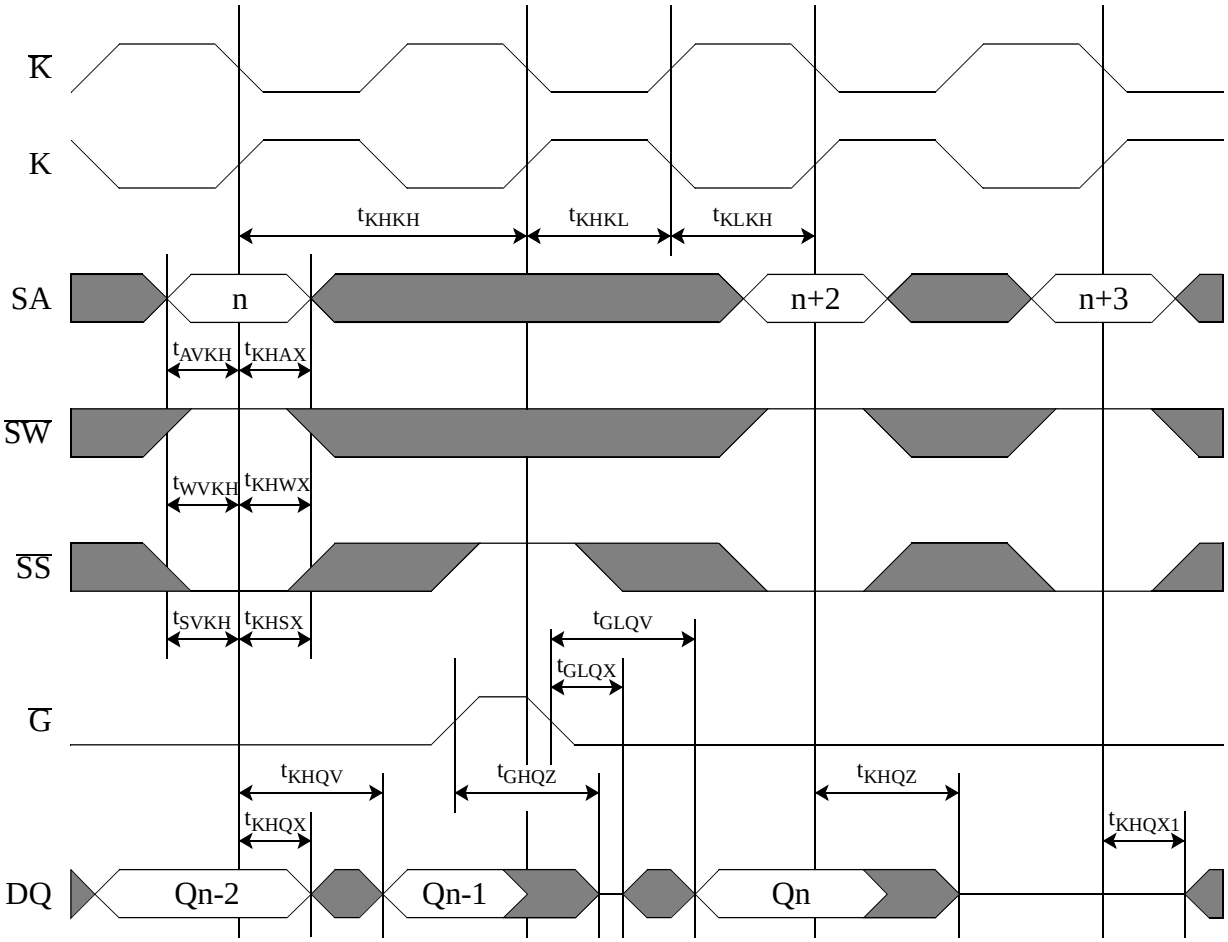
Item	Symbol	Conditions	Units	Notes
Input Reference Voltage	V_{REF}	0.85	V	
Address / Control Input High Level	V_{CAIH}	1.45	V	
Address / Control Input Low Level	V_{CAIL}	0.35	V	
Data Input High Level	V_{DIH}	1.25	V	
Data Input Low Level	V_{DIL}	0.55	V	
Input Rise & Fall Time		1.0	V/ns	
Input Reference Level		0.85	V	
Clock Input High Voltage	V_{KIH}	1.45	V	V_{DIF} = 0.7V
Clock Input Low Voltage	V_{KIL}	0.75	V	V_{DIF} = 0.7V
Clock Input Common Mode Voltage	V_{CM}	1.1	V	
Clock Input Rise & Fall Time		1.0	V/ns	
Clock Input Reference Level		K/$\overline{K}$ cross	V	
Output Reference Level		0.95	V	
Output Load Conditions				Fig.2 RQ = 250Ω

Fig. 2: AC Test Output Load (V_{DDQ} = 1.9V)

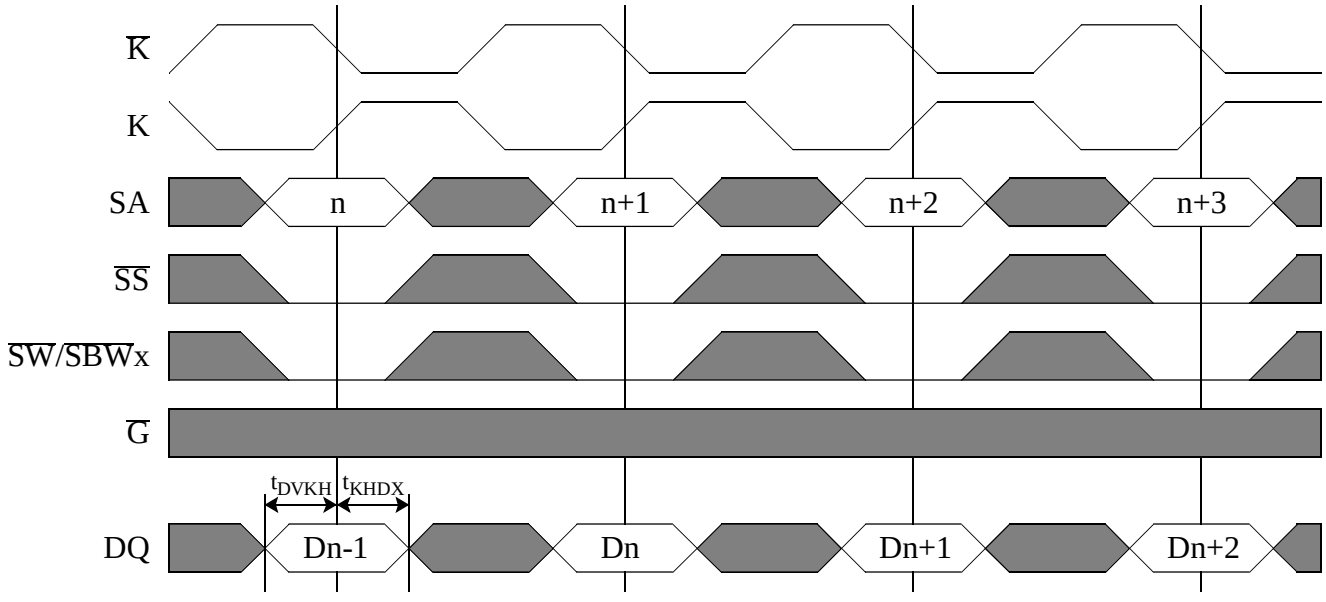


Register - Register Mode

Timing Diagram of Read and Deselect Operations

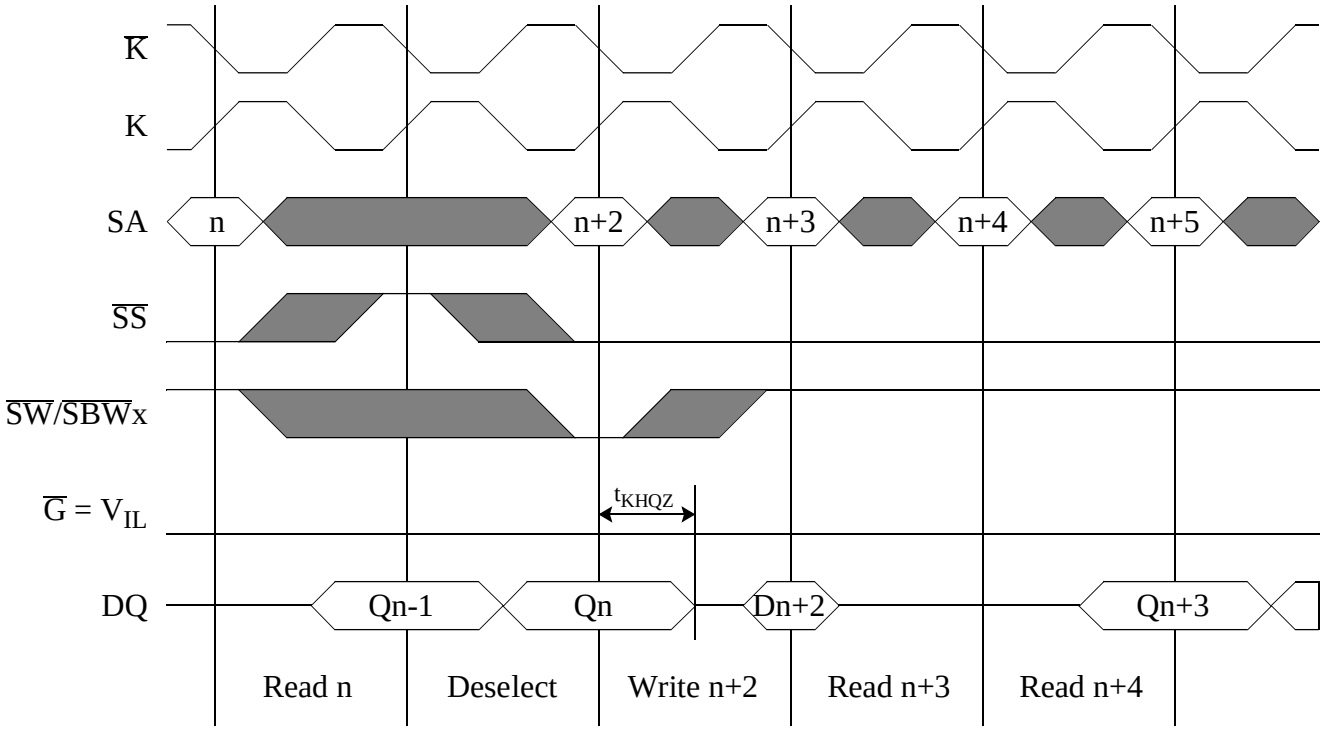


Timing Diagram of Write Operations

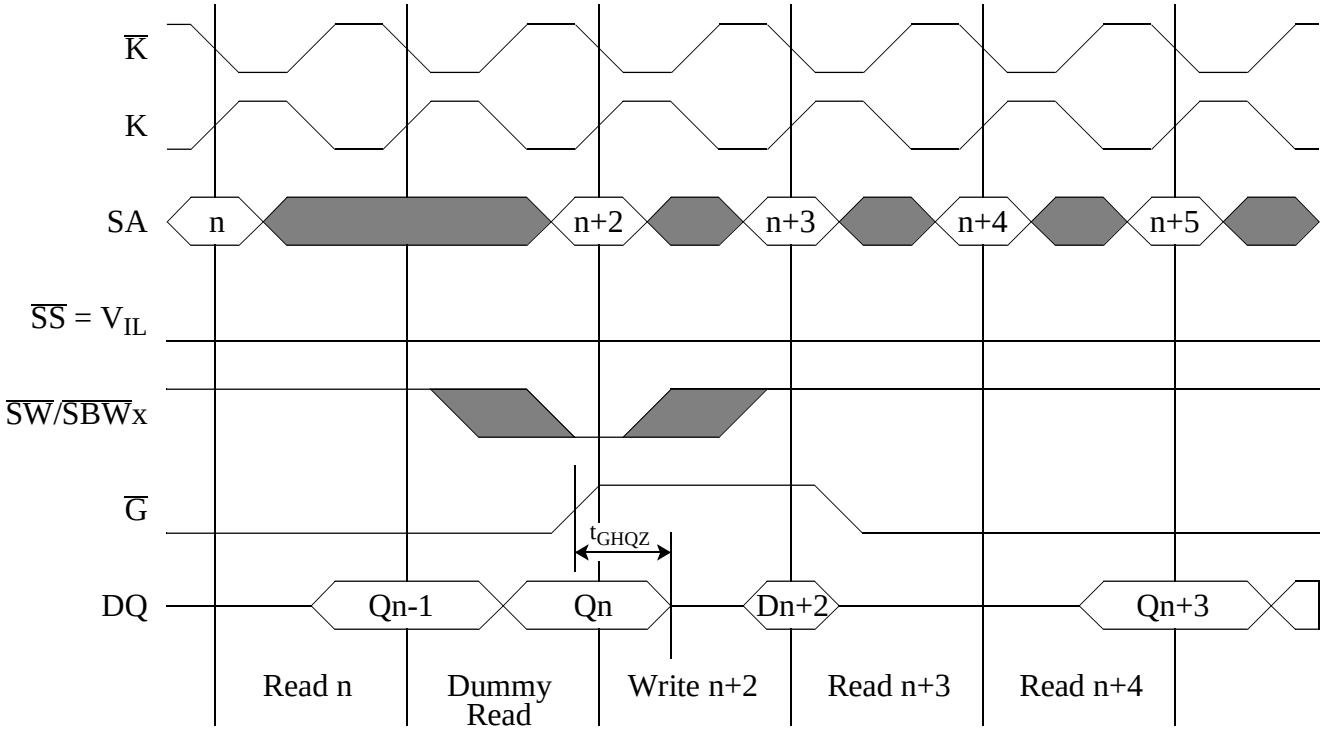


Register - Register Mode

Timing Diagram I of Read-Write-Read Operations ($\overline{SS}$ Controlled)

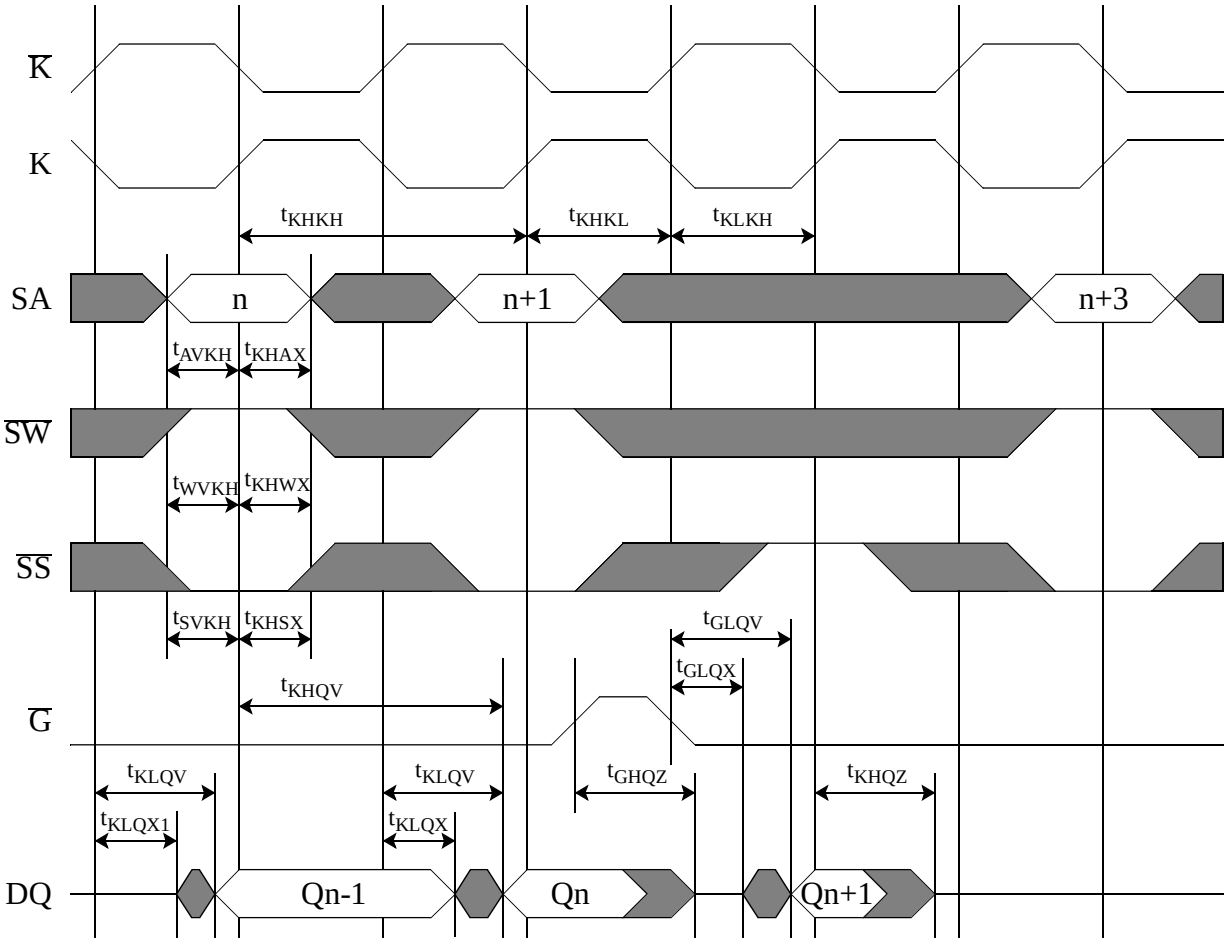


Timing Diagram II of Read-Write-Read Operations ($\overline{G}$ Controlled)

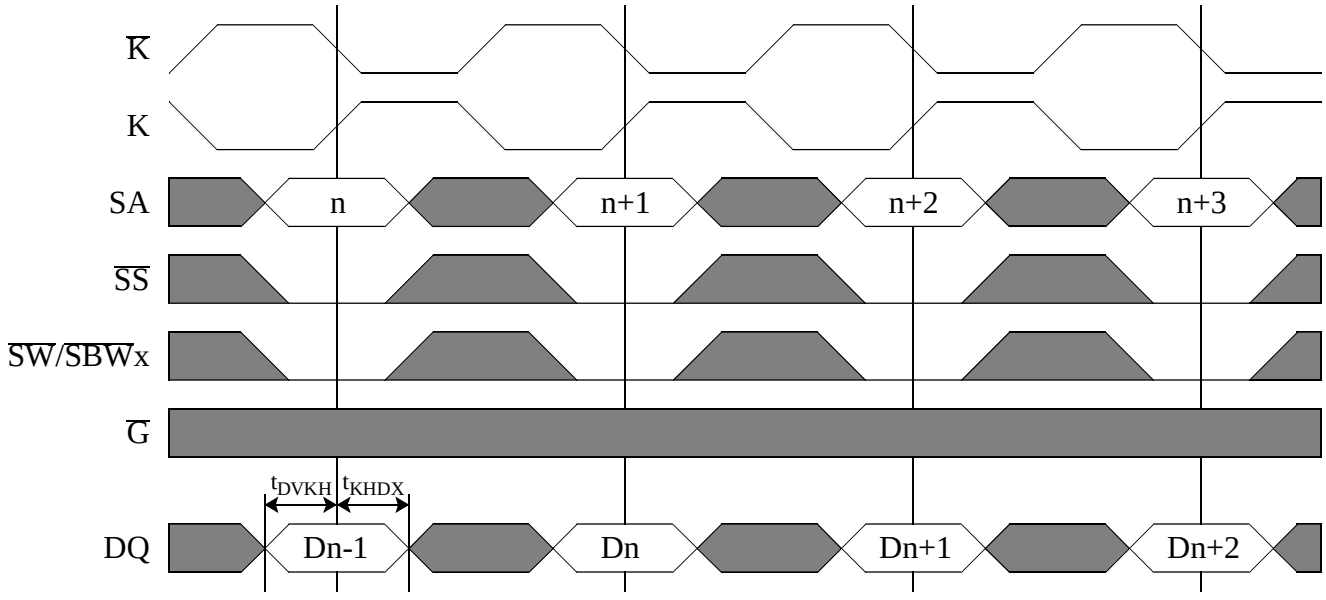


Register - Latch Mode

Timing Diagram of Read and Deselect Operations

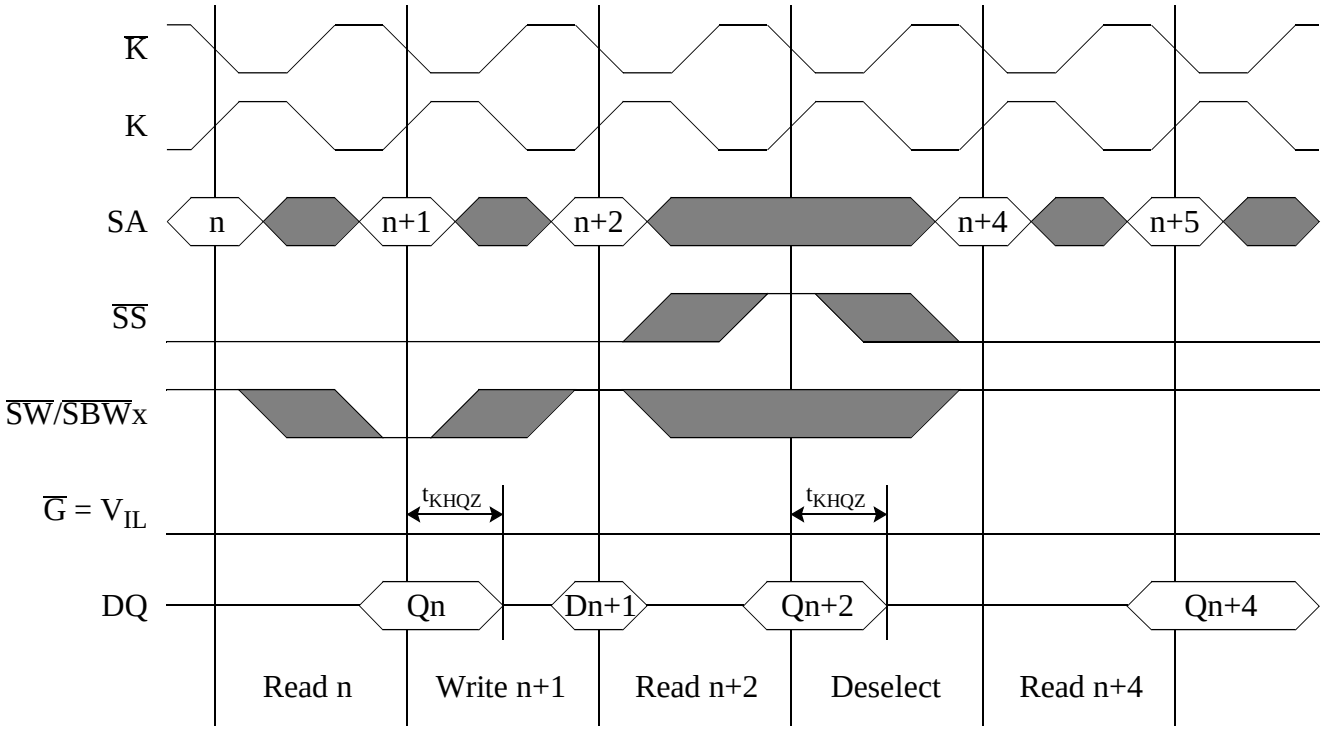


Timing Diagram of Write Operations



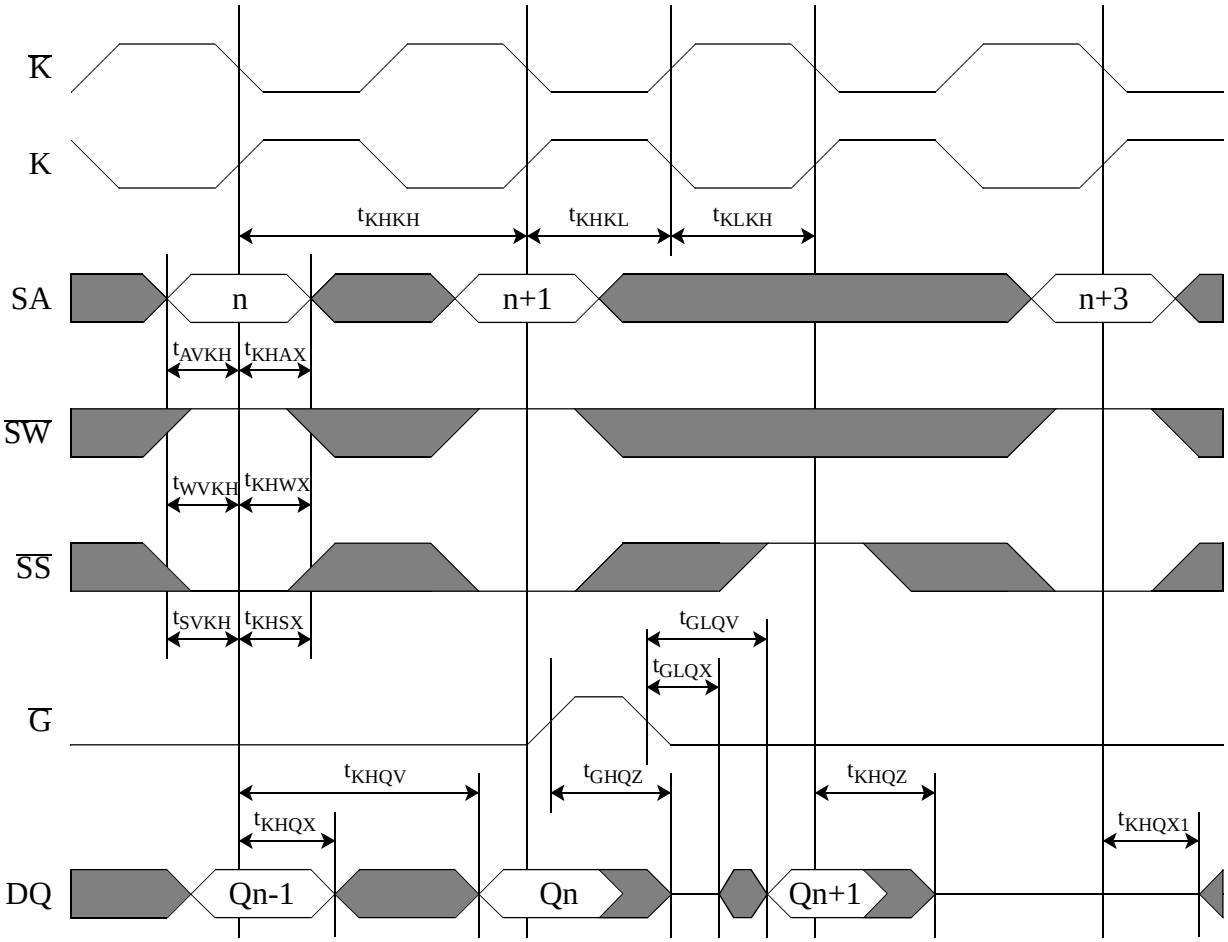
Register - Latch Mode

Timing Diagram of Read-Write-Read Operations

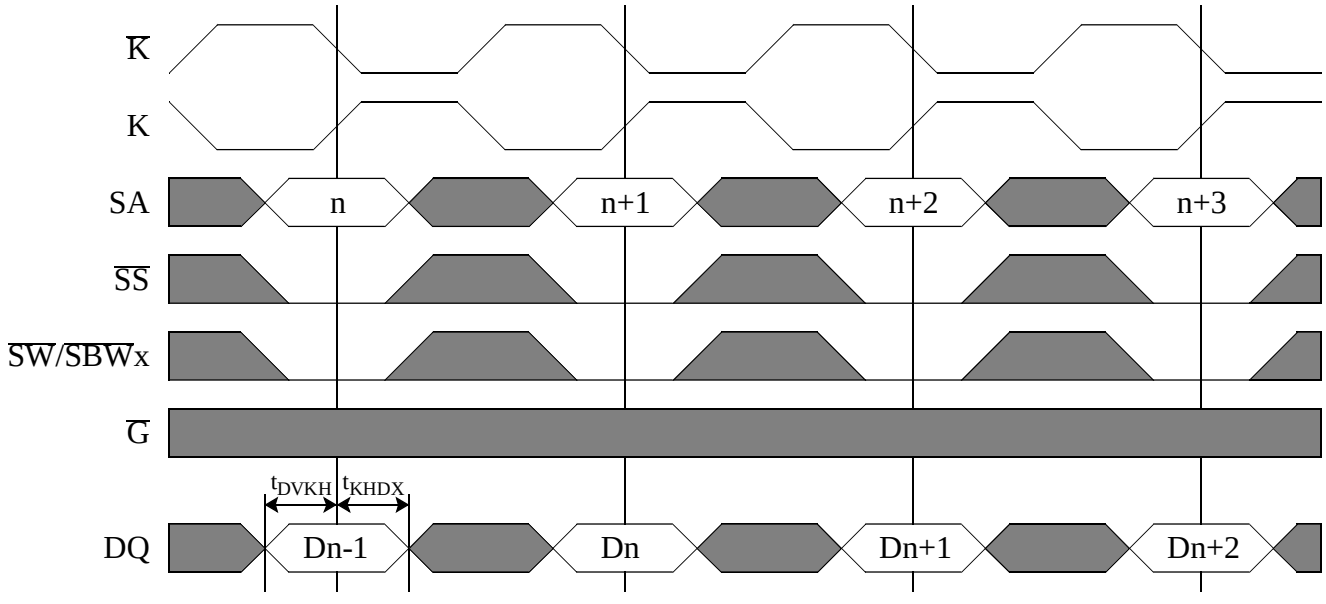


Register - Flow Thru Mode

Timing Diagram of Read and Deselect Operations

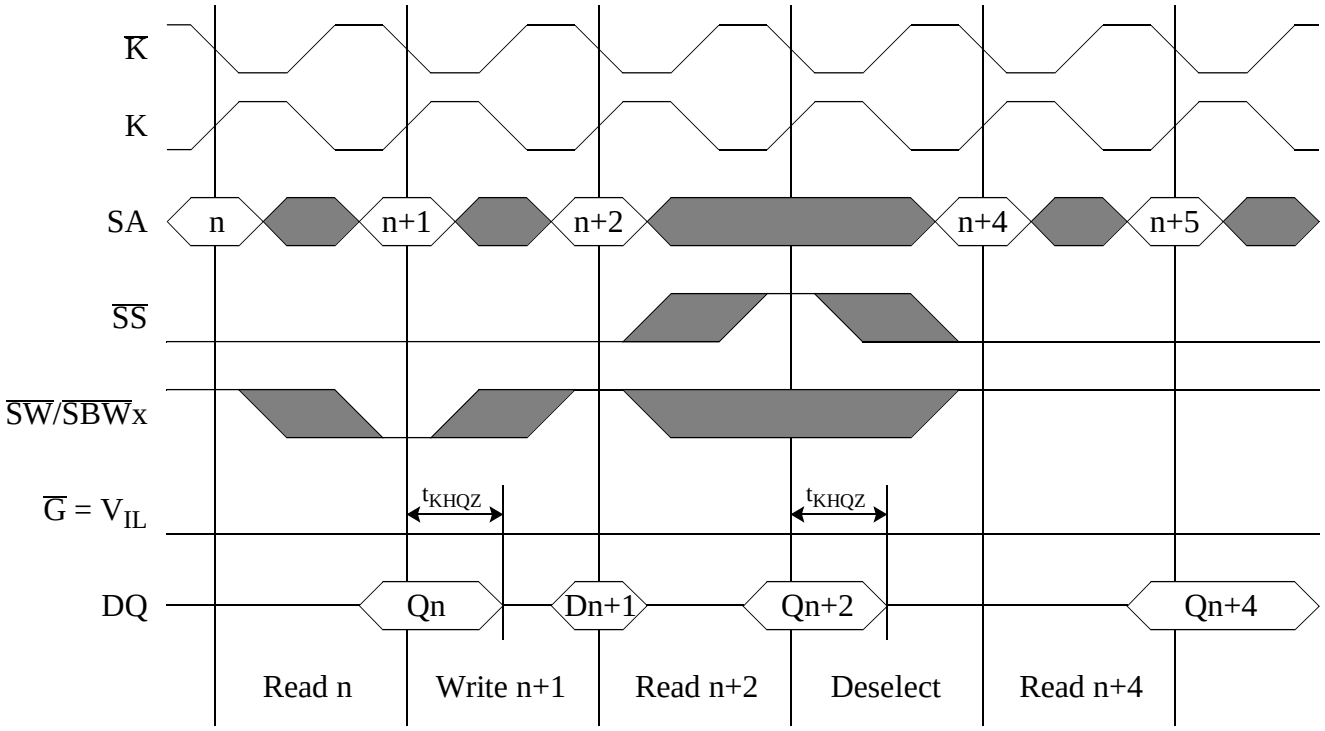


Timing Diagram of Write Operations



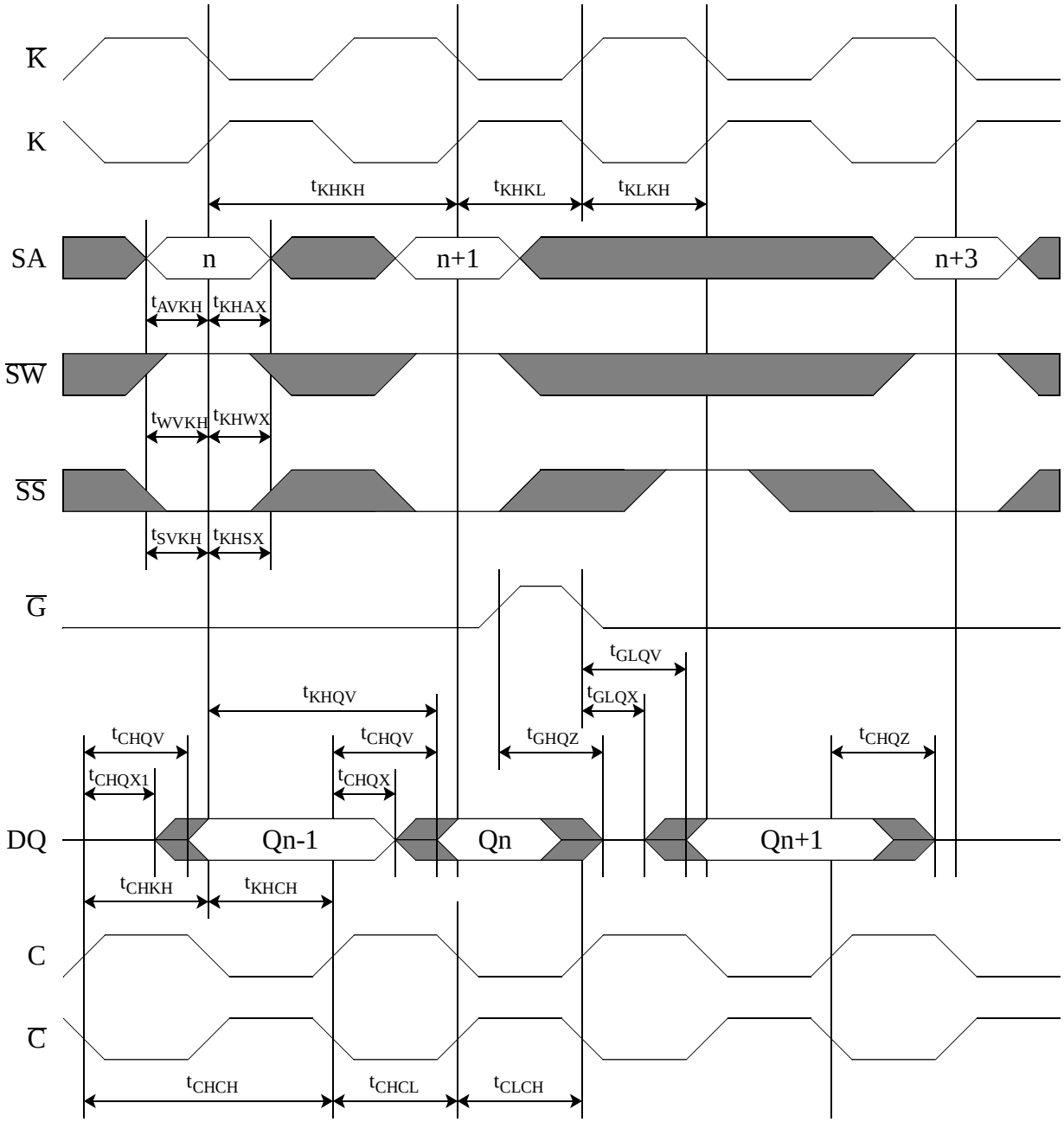
Register - Flow Thru Mode

Timing Diagram of Read-Write-Read Operations



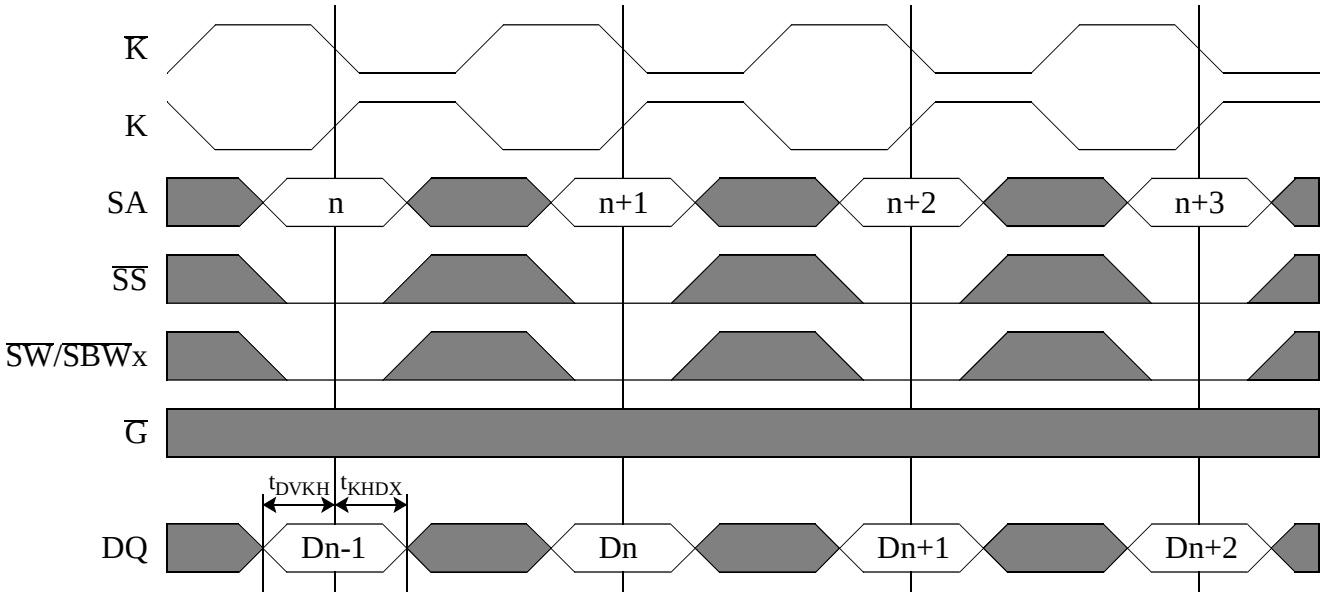
Dual Clock Mode

Timing Diagram of Read and Deselect Operations

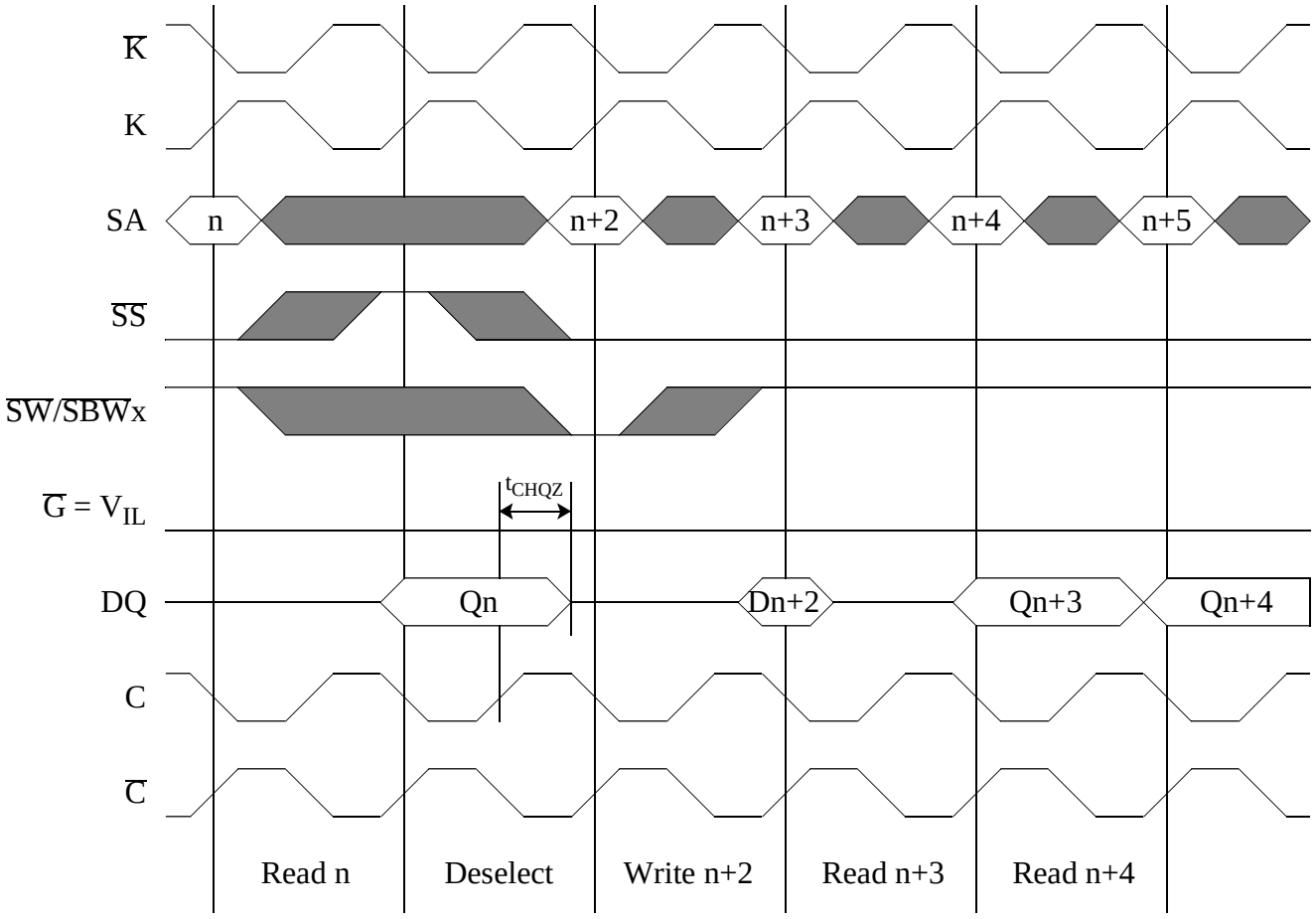


Dual Clock Mode

Timing Diagram of Write Operations

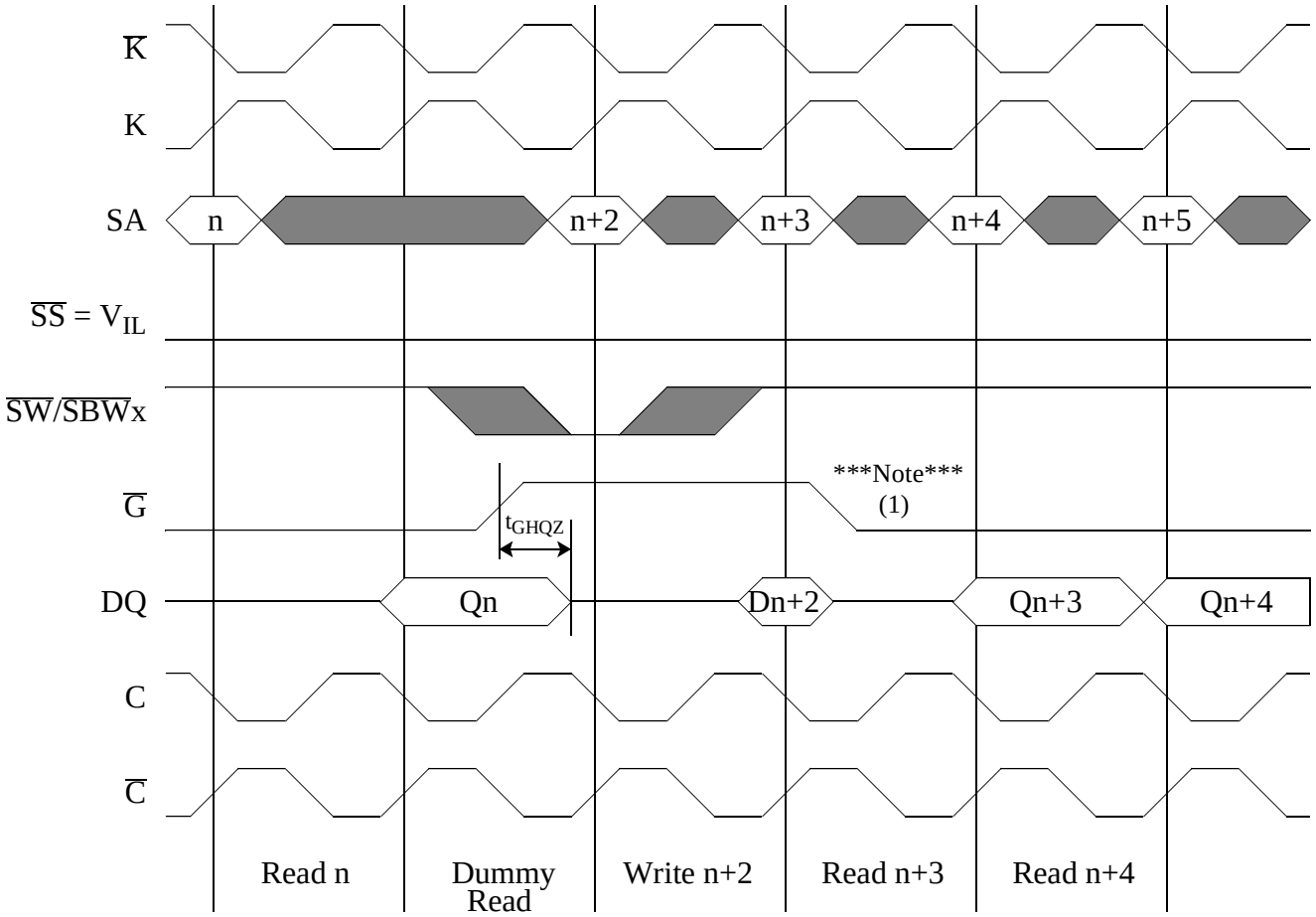


Timing Diagram I of Read-Write-Read Operations (SS Controlled)



Dual Clock Mode

Timing Diagram II of Read-Write-Read Operations ($\overline{G}$ Controlled)



Note 1: In order to prevent glitches on the data bus during write-read operations, when $\overline{G}$ is driven active (low) following the rising edge of K, the data bus will remain tri-stated until valid data from the most recent read operation is available. Specifically, the data bus will remain tri-stated for the **maximum** of the following three times:

1.T_{KHQV}
2.$T_{KHCH} + T_{CHQV}$
3.(K high to $\overline{G}$ low) + T_{GLQV}

Test Mode Description

Functional Description

These devices provide a JTAG boundary scan interface using a limited set of IEEE std. 1149.1 functions. The test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP controller, Instruction register, Boundary Scan register and Bypass register.

JTAG Inputs/Outputs are LVTTL compatible only.

Test Access Port (TAP)

4 pins as defined in the Pin Description table are used to perform JTAG functions. The TDI input pin is used to scan test data serially into one of three registers (Instruction register, Boundary Scan register and Bypass register). TDO is the output pin used to scan test data serially out. The TDI pin sends the data into LSB of the selected register and the MSB of the selected register feeds the data to TDO. The TMS input pin controls the state transition of 16 state TAP controller as specified in IEEE std. 1149.1. Inputs on TDI and TMS are registered on the rising edge of TCK clock. The output data on TDO is presented on the falling edge of TCK. TDO driver is in active state only when TAP controller is in Shift-IR state or in Shift-DR state.

TCK, TMS, TDI must be tied low when JTAG is not used.

TAP Controller

16 state controller is implemented as specified in IEEE std. 1149.1.

The controller enters reset state in one of two ways:

1. Power up.

2. Apply a logic 1 on TMS input pin on 5 consecutive TCK rising edges.

Instruction Register (3 bits)

The JTAG Instruction register consists of a shift register stage and parallel output latch. The register is 3 bits wide and is encoded as follow:

Octal	MSB.....LSB			Instruction
0	0	0	0	Bypass
1	0	0	1	IDCODE. Read device ID
2	0	1	0	Sample-Z. Sample Inputs and tri-state DQs
3	0	1	1	Bypass
4	1	0	0	Sample. Sample Inputs.
5	1	0	1	Private. Manufacturer use only.
6	1	1	0	Bypass
7	1	1	1	Bypass

Bypass Register (1 bit)

The Bypass Register is one bit wide and is connected electrically between TDI and TDO and provides the minimum length serial path between TDI and TDO.

ID Registers (32 bits)

The ID Register is 32 bits wide and is encoded as follows:

Device	Revision Number (31:28)	Part Number (27:12)	Sony ID (11:1)	Start Bit (0)
128K x 36	xxxx	0000 0000 0001 1111	0000 1110 001	1
256K x 18	xxxx	0000 0000 0010 0000	0000 1110 001	1

Boundary Scan Register (70 bits for 128Kx36, 51 bits for 256Kx18)

The Boundary Scan Register contains the following bits:

128K x 36		256K x 18	
DQ	36	DQ	18
SA	17	SA	18
$\overline{SW}$, $\overline{SBW}$x	5	$\overline{SW}$, $\overline{SBW}$x	3
$\overline{SS}$, $\overline{G}$	2	$\overline{SS}$, $\overline{G}$	2
K, $\overline{K}$, C, $\overline{C}$	4	K, $\overline{K}$, C, $\overline{C}$	4
ZZ	1	ZZ	1
M1, M2	2	M1, M2	2
ZQ	1	ZQ	1
Place Holder	2	Place Holder	2

K/$\overline{K}$, C/$\overline{C}$ inputs are sampled through one differential stage and inverted internally to generate internal K/$\overline{K}$, C/$\overline{C}$ signals for scan registers. Place Holders are required for some NC pins to allow for future density upgrades, and are connected to V_{SS} internally regardless of pin connection externally.

128K x 36 Scan Order Assignment (By Exit Sequence)

1	5R	M2		SA	3B	36
2	4P	SA		NC	2B	37
3	4T	SA		SA	3A	38
4	6R	SA		SA	3C	39
5	5T	SA		SA	2C	40
6	7T	ZZ		SA	2A	41
7	6P	DQa		DQc	2D	42
8	7P	DQa		DQc	1D	43
9	6N	DQa		DQc	2E	44
10	7N	DQa		DQc	1E	45
11	6M	DQa		DQc	2F	46
12	6L	DQa		DQc	2G	47
13	7L	DQa		DQc	1G	48
14	6K	DQa		DQc	2H	49
15	7K	DQa		DQc	1H	50
16	5L	$\overline{\text{SBW}}$a		$\overline{\text{SBW}}$c	3G	51
17	4L	$\overline{\text{K}}$		ZQ	4D	52
18	4K	K		$\overline{\text{SS}}$	4E	53
19	4F	$\overline{\text{G}}$		$\overline{\text{C}}$	4G	54
20	5G	$\overline{\text{SBW}}$b		C	4H	55
21	7H	DQb		$\overline{\text{SW}}$	4M	56
22	6H	DQb		$\overline{\text{SBW}}$d	3L	57
23	7G	DQb		DQd	1K	58
24	6G	DQb		DQd	2K	59
25	6F	DQb		DQd	1L	60
26	7E	DQb		DQd	2L	61
27	6E	DQb		DQd	2M	62
28	7D	DQb		DQd	1N	63
29	6D	DQb		DQd	2N	64
30	6A	SA		DQd	1P	65
31	6C	SA		DQd	2P	66
32	5C	SA		SA	3T	67
33	5A	SA		SA	2R	68
34	6B	NC		SA	4N	69
35	5B	SA		M1	3R	70

Note: NC pins at pad locations 6B (#34) and 2B (#37) are connected to V_{SS} internally, regardless of pin connection externally.

256K x 18 Scan Order Assignment (By Exit Sequence)

1	5R	M2		SA	3B	26
2	6T	SA		NC	2B	27
3	4P	SA		SA	3A	28
4	6R	SA		SA	3C	29
5	5T	SA		SA	2C	30
6	7T	ZZ		SA	2A	31
7	7P	DQa		DQb	1D	32
8	6N	DQa		DQb	2E	33
9	6L	DQa		DQb	2G	34
10	7K	DQa		DQb	1H	35
11	5L	$\overline{\text{SBW}}$a		$\overline{\text{SBW}}$b	3G	36
12	4L	$\overline{\text{K}}$		ZQ	4D	37
13	4K	K		$\overline{\text{SS}}$	4E	38
14	4F	$\overline{\text{G}}$		$\overline{\text{C}}$	4G	39
15	6H	DQb		C	4H	40
16	7G	DQb		$\overline{\text{SW}}$	4M	41
17	6F	DQb		DQb	2K	42
18	7E	DQb		DQb	1L	43
19	6D	DQb		DQb	2M	44
20	6A	SA		DQb	1N	45
21	6C	SA		DQb	2P	46
22	5C	SA		SA	3T	47
23	5A	SA		SA	2R	48
24	6B	NC		SA	4N	49
25	5B	SA		SA	2T	50
				M1	3R	51

Note: NC pins at pad locations 6B (#24) and 2B (#27) are connected to V_{SS} internally, regardless of pin connection externally.

Ordering Information.

Part Number	V_{DD}	Size	Speed (Cycle Time / Access Time)		
			R-R	R-L & R-FT	DC
CXK77B3640A-37	3.3V	128K x 36	3.45ns / 2.25ns	4.8ns / 4.6ns	3.7ns / 4.9ns
CXK77B3640A-38	3.3V	128K x 36	3.8ns / 2.25ns	4.8ns / 4.8ns	3.8ns / 4.9ns
CXK77B3640A-4	3.3V	128K x 36	3.8ns / 2.25ns	5.2ns / 5.2ns	4.0ns / 5.2ns
CXK77B3640A-45	3.3V	128K x 36	5.0ns / 2.50ns	6.0ns / 6.0ns	4.5ns / 6.0ns
CXK77B1840A-37	3.3V	256K x 18	3.45ns / 2.25ns	4.8ns / 4.6ns	---
CXK77B1840A-38	3.3V	256K x 18	3.8ns / 2.25ns	4.8ns / 4.8ns	---
CXK77B1840A-4	3.3V	256K x 18	3.8ns / 2.25ns	5.2ns / 5.2ns	---
CXK77B1840A-45	3.3V	256K x 18	5.0ns / 2.50ns	6.0ns / 6.0ns	---

Note: Contact Sony Memory Marketing for availability of DC mode functionality in CXK77B1840A.

Revision History

Rev. #	Rev. date	Description of Modification
rev 0.0	02/10/98	Initial Version
rev 0.0	02/20/98	1. Changed DC Recommended Operating Conditions (p. 10). 2. Added x36 and x18 typical I_{DD} values (p. 11). 3. Changed 1.5V V_{DDQ} AC Test Conditions (p. 15). 4. Changed 1.9V V_{DDQ} AC Test Conditions (p. 16). 5. Added x36 and x18 part numbers in boundary scan ID Registers (p. 27).
rev 1.0	04/14/98	1. Modified AC Timing Characteristics Renamed "-40" bin to "-4" bin in all modes. R-R Mode: Added "Clock Pulse Width timing parameters characterized but not 100% tested at 1.3ns" note for -37 and -38 bins. -37 T_{KHKH} 4.0ns to 3.7ns T_{AVKH}, T_{WVKH} T_{SVKH} 0.5ns to 0.3ns T_{KHQV}, T_{KHQZ}, T_{GLQV}, T_{GHQZ} 2.0ns to 2.25ns -38 T_{KHKH} 4.0ns to 3.8ns T_{KHKL}, T_{KLKH} 1.4ns to 1.3ns T_{AVKH}, T_{WVKH} T_{SVKH} 0.5ns to 0.3ns T_{KHQV}, T_{KHQZ}, T_{GLQV}, T_{GHQZ} 2.1ns to 2.25ns -4 T_{KHKH} 4.5ns to 5.0ns T_{AVKH}, T_{WVKH} T_{SVKH} 0.5ns to 0.3ns T_{KHQV}, T_{KHQZ}, T_{GLQV}, T_{GHQZ} 2.3ns to 2.25ns R-L, R-FT Modes: Added "Address, Control, and Data input setup and hold timing parameter measurement" note for -37 and -38 bins. Added "R-FT timing parameters guaranteed by design only" note for all bins. Removed T_{KHQZ1} from all bins. -37 T_{KHKL}, T_{KLKH} 1.3ns to 1.5ns T_{AVKH}, T_{WVKH}, T_{SVKH}, T_{DVKH} 0.5ns to 0.4ns T_{KHAX}, T_{KHWX}, T_{KHSX}, T_{KHDX} 1.0ns to 0.8ns T_{KHQV} 5.0ns to 4.5ns T_{KLQV}, T_{KHQZ}, T_{GLQV}, T_{GHQZ} 2.0ns to 2.1ns -38 T_{KHKH} 4.5ns to 5.0ns T_{KHKL}, T_{KLKH} 1.4ns to 1.5ns T_{AVKH}, T_{WVKH}, T_{SVKH}, T_{DVKH} 0.5ns to 0.4ns T_{KHAX}, T_{KHWX}, T_{KHSX}, T_{KHDX} 1.0ns to 0.8ns T_{KLQV}, T_{KHQZ}, T_{GLQV}, T_{GHQZ} 2.1ns to 2.2ns -4 T_{KHKH} 5.0ns to 5.5ns -45 T_{KHKH} 5.5ns to 6.0ns T_{KHQV} 6.5ns to 6.0ns

Rev. #	Rev. date	Description of Modification
rev 1.0	04/14/98	1. Modified AC Timing Characteristics (continued) DC Mode: Added "Clock Pulse Width timing parameters characterized but not 100% tested at 1.3ns" note for -37 and -38 bins. -37 T_{CHQV}, T_{CHQZ} 2.0ns to 2.1ns -38 T_{KHKL}, T_{KLKH}, T_{CHCL}, T_{CLCH} 1.4ns to 1.3ns T_{KHDX} 0.8ns to 0.7ns T_{KHQV} 5.1ns to 4.9ns T_{GLQV}, T_{GHQZ} 1.9ns to 1.8ns -4 T_{KHQV} 5.3ns to 5.2ns -45 T_{KHQV} 6.5ns to 6.0ns 2. Changed all maximum ambient temperature references (T_A Max) from 70°C to 85°C (pp. 9-16).
rev 1.1	05/08/98	1. Changed 1.9V V_{DDQ} AC Test Conditions (p. 16). Deleted Input High and Low Levels. Added Address / Control Input High and Low Levels. Added Data Input High and Low Levels. Changed Input Reference Voltage (V_{REF}) from 0.75V to 0.85V.
rev 1.2	05/18/98	1. Changed V_{IH} / V_{IL} levels for Boundary Scan chain signals during Boundary Scan test mode (p. 10).
rev 1.3	05/26/98	1. Modified AC Timing Characteristics R-R Mode: -4 T_{KHKH} 5.0ns to 3.8ns
rev 1.4	06/18/98	1. Modified AC Timing Characteristics R-R Mode: Changed T_{DVKH} to 1.0ns in all bins. -37 T_{KHKH} 3.7ns to 3.45ns R-L, R-FT Modes: Changed T_{DVKH} to 1.0ns in all bins. -37 T_{KHKH} 4.5ns to 4.8ns T_{KHQV} 4.5ns to 4.6ns T_{KLQV} 2.1ns to 2.2ns -38 T_{KHKH} 5.0ns to 4.8ns T_{KHQV} 5.0ns to 4.8ns -4 T_{KHKH} 5.5ns to 5.2ns T_{KHQV} 5.5ns to 5.2ns DC Mode: Added "DC operation and timing parameters tested in CXK77B3640A only" note for all bins.

Rev. #	Rev. date	Description of Modification
rev 1.5	07/23/98	1. Modified Output Driver Impedance (R_{OUT}) section of DC Electrical Characteristics (p. 11). Changed “Min” and “Max” parameters to absolute values.