TigerSHARC® Embedded Processor

Preliminary Technical Data ADSP-TS201S

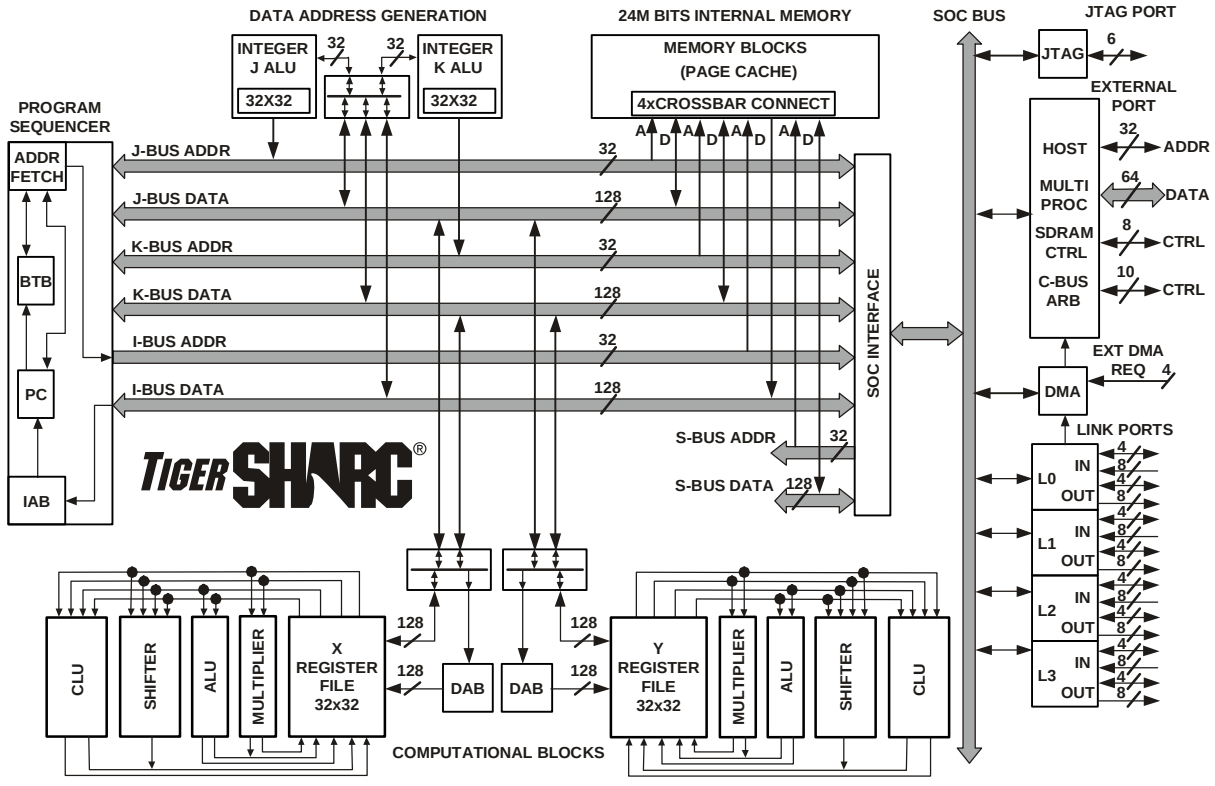
KEY FEATURES

- 500 MHz, 2.0 ns Instruction Cycle Rate
- 24M Bits of Internal—On-Chip—DRAM Memory
- 25×25 mm (576-Ball) Thermally Enhanced Ball Grid Array Package
- Dual Computation Blocks—Each Containing an ALU, a Multiplier, a Shifter, a Register File, and a Communications Logic Unit (CLU)
- Dual Integer ALUs, providing Data Addressing and Pointer Manipulation
- Integrated I/O Includes 14 Channel DMA Controller, External Port, Four Link Ports, SDRAM Controller, Programmable Flag Pins, Two Timers, and Timer Expired Pin for System Integration
- 1149.1 IEEE Compliant JTAG Test Access Port for On-Chip Emulation
- On-Chip Arbitration for Glueless Multiprocessing

KEY BENEFITS

- Provides High-Performance Static Superscalar DSP Operations, Optimized for Telecommunications Infrastructure and Other Large, Demanding Multiprocessor DSP Applications
- Performs Exceptionally Well on DSP Algorithm and I/O Benchmarks (See Benchmarks in Table 1)
- Supports Low-Overhead DMA Transfers Between Internal Memory, External Memory, Memory-Mapped Peripherals, Link Ports, Host Processors, and Other (Multiprocessor) DSPs
- Eases DSP Programming Through Extremely Flexible Instruction Set and High-Level-Language Friendly DSP Architecture
- Enables Scalable Multiprocessing Systems With Low Communications Overhead

FUNCTIONAL BLOCK DIAGRAM



REV. PrG

One Technology Way, P.O.Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel:781/329-4700 www.analog.com
Fax:781/326-8703

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GENERAL DESCRIPTION

The ADSP-TS201S TigerSHARC processor is an ultra-high performance, static superscalar processor optimized for large signal processing tasks and communications infrastructure. The DSP combines very wide memory widths with dual computation blocks—supporting 32- and 40-bit floating-point and supporting 8-, 16-, 32-, and 64-bit fixed-point processing—to set a new standard of performance for digital signal processors. The TigerSHARC static superscalar architecture lets the DSP execute up to four instructions each cycle, performing twenty-four 16-bit fixed-point operations or six floating-point operations.

Four independent 128-bit wide internal data buses, each connecting to the six 4M bit memory banks, enable quad-word data, instruction, and I/O accesses and provide 28G bytes per second of internal memory bandwidth. Operating at 500 MHz, the ADSP-TS201S processor's core has a 2.0 ns instruction cycle time. Using its Single-Instruction, Multiple-Data (SIMD) features, the ADSP-TS201S processor can perform four billion 40-bit MACs or one billion 80-bit MACs per second. Table 1 shows the DSP's performance benchmarks.

Table 1. General Purpose Algorithm Benchmarks at 500 MHz

Benchmark	Speed	Clock Cycles
32-bit Algorithm, 500 million MACs/s peak performance		
1024 Point Complex FFT[1] (Radix 2)	20 µs	10061
FIR Filter (per real tap)	1 ns	0.5
[8 × 8] [8 × 8] Matrix Multiply (Complex, Floating-point)	2.8 µs	1399
16-bit Algorithm, 2 billion MACs/s peak performance		
256 Point Complex FFT[1] (Radix 2)	1.9 µs	928
I/O DMA Transfer Rate		
External port	1G bytes/s	n/a
Link ports (each)	1G bytes/s	n/a

[1] Cache preloaded

The ADSP-TS201S processor is code-compatible with the other TigerSHARC processors.

The Functional Block Diagram on page 1 shows the ADSP-TS201S processor's architectural blocks. These blocks include:

- Dual compute blocks, each consisting of an ALU, multiplier, 64-bit shifter, 128-bit CLU, and 32-word register file and associated Data Alignment Buffers (DABs)
- Dual integer ALUs (IALUs), each with its own 31-word register file for data addressing and a status register
- A program sequencer with Instruction Alignment Buffer (IAB) and Branch Target Buffer (BTB)
- An interrupt controller that supports hardware and software interrupts, supports level- or edge-triggers, and supports prioritized, nested interrupts

- Four 128-bit internal data buses, each connecting to the six 4M bit memory banks
- On-chip DRAM (24M bit)
- An external port that provides the interface to host processors, multiprocessing space (DSPs), off-chip memory-mapped peripherals, and external SRAM and SDRAM
- A 14 channel DMA controller
- Four full-duplex LVDS link ports
- Two 64-bit interval timers and timer expired pin
- A 1149.1 IEEE compliant JTAG test access port for on-chip emulation

Figure 1 on page 3 shows a typical single-processor system with external SRAM and SDRAM. Figure 3 on page 7 shows a typical multiprocessor system.

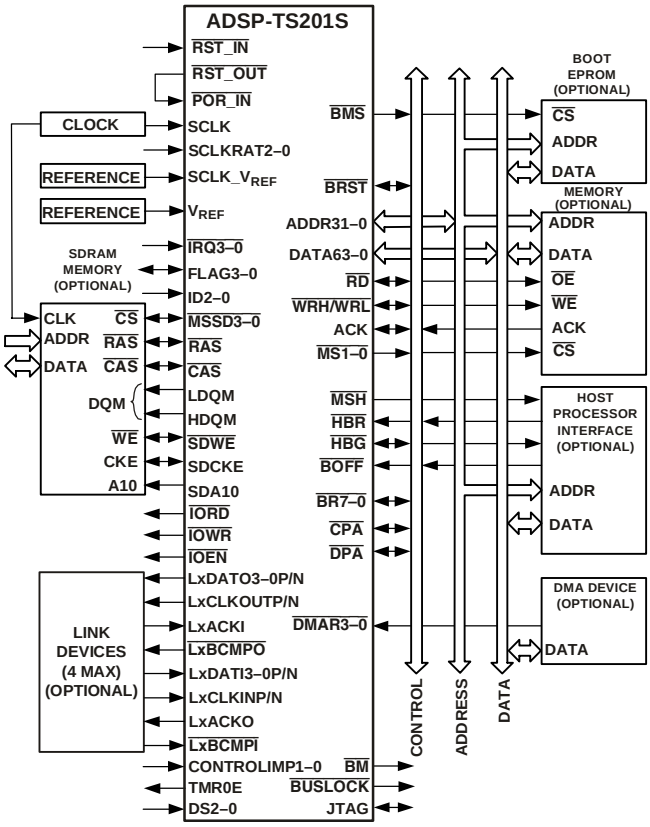


Figure 1. ADSP-TS201S Single-Processor System With External SDRAM

The TigerSHARC DSP uses a Static Superscalar[1] architecture. This architecture is superscalar in that the ADSP-TS201S processor's core can execute simultaneously from one to four 32-bit instructions encoded in a Very Large Instruction Word (VLIW) instruction line using the DSP's dual compute blocks. Because the DSP does not perform instruction re-ordering at runtime—the programmer selects which operations will execute in parallel prior to runtime—the order of instructions is static.

With few exceptions, an instruction line, whether it contains one, two, three, or four 32-bit instructions, executes with a throughput of one cycle in a ten-deep processor pipeline.

For optimal DSP program execution, programmers must follow the DSP's set of instruction parallelism rules when encoding an instruction line. In general, the selection of instructions that the DSP can execute in parallel each cycle depends on the instruction line resources each instruction requires and on the source and destination registers used in the instructions. The programmer has direct control of three core components—the IALUs, the compute blocks, and the program sequencer.

The ADSP-TS201S processor, in most cases, has a two-cycle execution pipeline that is fully interlocked, so—whenever a computation result is unavailable for another operation dependent on it—the DSP automatically inserts one or more stall cycles as needed. Efficient programming with dependency-free instructions can eliminate most computational and memory transfer data dependencies.

In addition, the ADSP-TS201S processor supports SIMD operations two ways—SIMD compute blocks and SIMD computations. The programmer can load both compute blocks with the same data (broadcast distribution) or different data (merged distribution).

Dual Compute Blocks

The ADSP-TS201S processor has compute blocks that can execute computations either independently or together as a Single-Instruction, Multiple-Data (SIMD) engine. The DSP can issue up to two compute instructions per compute block each cycle, instructing the ALU, multiplier, shifter, or CLU to perform independent, simultaneous operations. Each compute block can execute eight 8-bit, four 16-bit, two 32-bit, or one 64-bit SIMD computations in parallel with the operation in the other block.

The compute blocks are referred to as X and Y in assembly syntax, and each block contains four computational units—an ALU, a multiplier, a 64-bit shifter, a 128-bit CLU—and a 32-word register file.

- Register File—Each Compute Block has a multiported 32-word, fully orthogonal register file used for transferring data between the computation units and data buses and for storing intermediate results. Instructions can access the registers in the register file individually (word-aligned), in sets of two (dual-aligned), or in sets of four (quad-aligned).
- ALU—The ALU performs a standard set of arithmetic operations in both fixed- and floating-point formats. It also performs logic operations.
- Multiplier—The multiplier performs both fixed- and floating-point multiplication and fixed-point multiply and accumulate.

[1] Static Superscalar™ is a trademark of Analog Devices, Inc.

- Shifter—The 64-bit shifter performs logical and arithmetic shifts, bit and bitstream manipulation, and field deposit and extraction operations.
- Communications Logic Unit (CLU)—This is a 128-bit unit provides Trellis Decoding (for example, Viterbi and Turbo decoders) and executes complex correlations for CDMA communication applications (for example chip-rate and symbol-rate functions).

Using these features, the compute blocks can:

- Provide 8 MACs per cycle peak and 7.1 MACs per cycle sustained 16-bit performance and provide 2 MACs per cycle peak and 1.8 MACs per cycle sustained 32-bit performance (based on FIR)
- Execute six single-precision floating-point or execute twenty-four 16-bit fixed-point operations per cycle, providing 3 GFLOPS or 12.0 GOPS performance
- Perform two complex 16-bit MACs per cycle
- Execute eight Trellis butterflies in one cycle

Data Alignment Buffer (DAB)
The DAB is a quad-word FIFO that enables loading of quad-word data from nonaligned addresses. Normally, load instructions must be aligned to their data size so that quad words are loaded from a quad-aligned address. Using the DAB significantly improves the efficiency of some applications, such as FIR filters.

Dual Integer ALUs (IALUs)
The ADSP-TS201S processor has two IALUs that provide powerful address generation capabilities and perform many general-purpose integer operations. The IALUs are referred to as J and K in assembly syntax and have the following features:

- Provides memory addresses for data and update pointers
- Supports circular buffering and bit-reverse addressing
- Performs general-purpose integer operations, increasing programming flexibility
- Includes a 31-word register file for each IALU

As address generators, the IALUs perform immediate or indirect (pre- and post-modify) addressing. They perform modulus and bit-reverse operations with no constraints placed on memory addresses for the modulus data buffer placement. Each IALU can specify either a single-, dual-, or quad-word access from memory.

The IALUs have hardware support for circular buffers, bit reverse, and zero-overhead looping. Circular buffers facilitate efficient programming of delay lines and other data structures required in digital signal processing, and they are commonly used in digital filters and Fourier transforms. Each IALU provides registers for four circular buffers, so applications can set up a total of eight circular buffers. The IALUs handle address pointer wraparound automatically, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Because the IALU's computational pipeline is one cycle deep, in most cases integer results are available in the next cycle. Hardware (register dependency check) causes a stall if a result is unavailable in a given cycle.

Program Sequencer
The ADSP-TS201S processor's program sequencer supports the following:

- A fully interruptible programming model with flexible programming in assembly and C/C++ languages; handles hardware interrupts with high throughput and no aborted instruction cycles
- A ten-cycle instruction pipeline—four-cycle fetch pipe and six-cycle execution pipe—computation results available two cycles after operands are available
- Supply of instruction fetch memory addresses; the sequencer's Instruction Alignment Buffer (IAB) caches up to five fetched instruction lines waiting to execute; the program sequencer extracts an instruction line from the IAB and distributes it to the appropriate core component for execution
- Management of program structures and program flow determined according to JUMP, CALL, RTI, RTS instructions, loop structures, conditions, interrupts, and software exceptions
- Branch prediction and a 128-entry branch target buffer (BTB) to reduce branch delays for efficient execution of conditional and unconditional branch instructions and zero-overhead looping; correctly predicted branches that are taken occur with zero overhead cycles, overcoming the five-to-nine stage branch penalty
- Compact code without the requirement to align code in memory; the IAB handles alignment

Interrupt Controller
The DSP supports nested and nonnested interrupts. Each interrupt type has a register in the interrupt vector table. Also, each has a bit in both the interrupt latch register and the interrupt mask register. All interrupts are fixed as either level-sensitive or edge-sensitive, except the $\overline{\text{IRQ3–0}}$ hardware interrupts, which are programmable.

The DSP distinguishes between hardware interrupts and software exceptions, handling them differently. When a software exception occurs, the DSP aborts all other instructions in the instruction pipe. When a hardware interrupt occurs, the DSP continues to execute instructions already in the instruction pipe.

Flexible Instruction Set
The 128-bit instruction line, which can contain up to four 32-bit instructions, accommodates a variety of parallel operations for concise programming. For example, one instruction line can direct the DSP to conditionally execute a multiply, an add, and

a subtract in both computation blocks while it also branches to another location in the program. Some key features of the instruction set include:

- CLU instructions for communications infrastructure to govern Trellis Decoding (for example, Viterbi and Turbo decoders) and Despreading via complex correlations
- Algebraic assembly language syntax
- Direct support for all DSP, imaging, and video arithmetic types
- Eliminates toggling DSP hardware modes because modes are supported as options (for example, rounding, saturation, and others) within instructions
- Branch prediction encoded in instruction; enables zero-overhead loops
- Parallelism encoded in instruction line
- Conditional execution optional for all instructions
- User defined partitioning between program and data memory

DSP Memory

The DSP's internal and external memory is organized into a unified memory map, which defines the location (address) of all elements in the system, as shown in Figure 2.

The memory map is divided into four memory areas—host space, external memory, multiprocessor space, and internal memory—and each memory space, except host memory, is subdivided into smaller memory spaces.

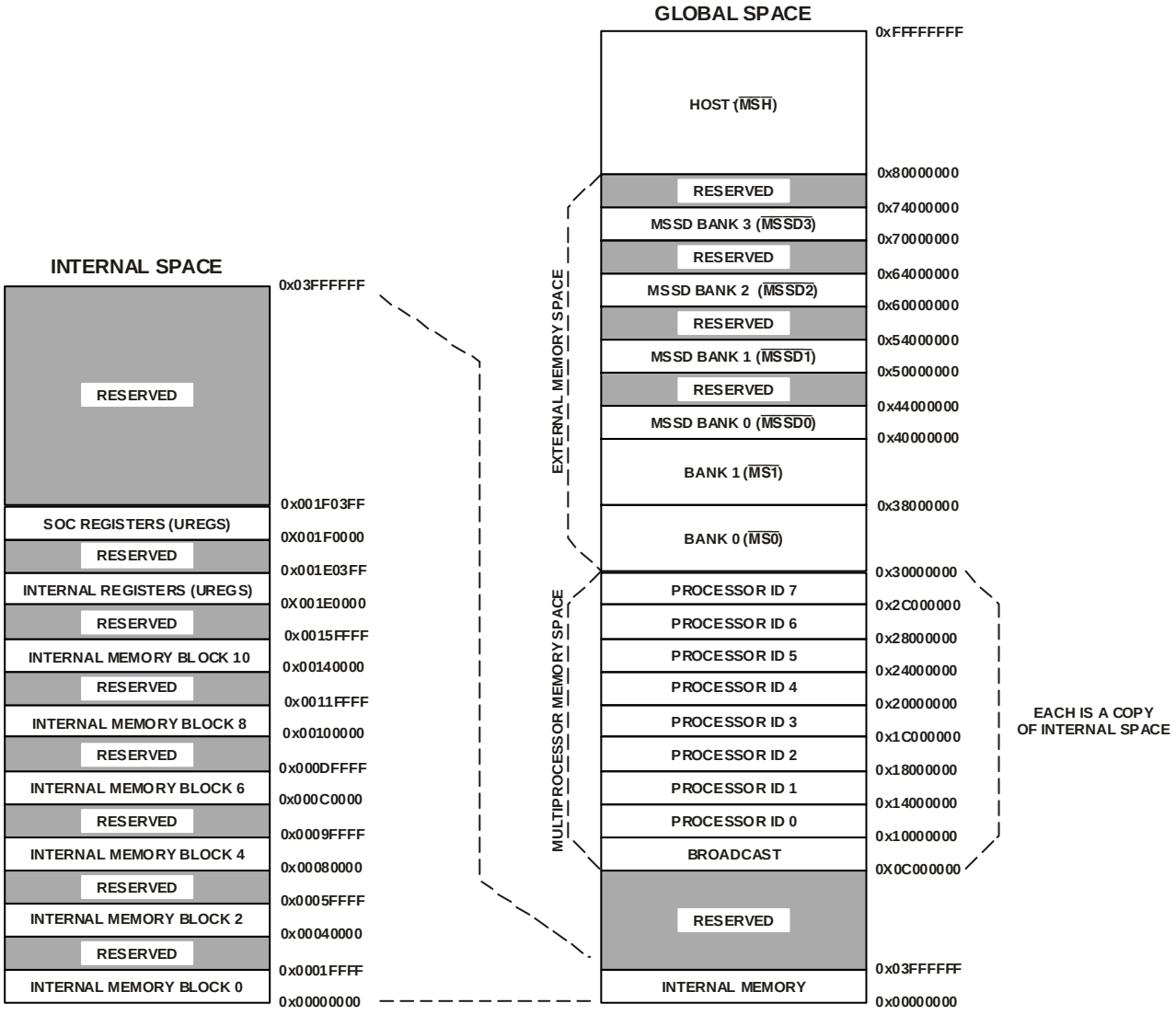


Figure 2. ADSP-TS201S Memory Map

The ADSP-TS201S processor internal memory has 24M bits of on-chip DRAM memory, divided into six blocks of 4M bits (128K words × 32 bits). Each block—M0, M2, M4, M6, M8, and M10—can store program, data, or both, so applications can configure memory to suit specific needs. Placing program instructions and data in different memory blocks, however, enables the DSP to access data while performing an instruction fetch. Each memory segment contains a 128K bit cache to enable single cycle accesses to internal DRAM.

The six internal memory blocks connect to the four 128-bit wide internal buses through a crossbar connection, enabling the DSP to perform four memory transfers in the same cycle. The DSP's internal bus architecture provides a total memory bandwidth of 28G bytes per second, enabling the core and I/O to access eight 32-bit data words and four 32-bit instructions each cycle. The DSP's flexible memory structure enables:

- DSP core and I/O accesses to different memory blocks in the same cycle
- DSP core access to three memory blocks in parallel—one instruction and two data accesses
- Programmable partitioning of program and data memory
- Program access of all memory as 32-, 64-, or 128-bit words—16-bit words with the DAB

External Port (Off-Chip Memory/Peripherals Interface)
The ADSP-TS201S processor's external port provides the DSP's interface to off-chip memory and peripherals. The 4G word address space is included in the DSP's unified address space. The separate on-chip buses—four 128-bit data buses and four 32-bit address buses—are multiplexed at the SOC interface and transferred to the external port over the SOC bus to create an external system bus transaction. The external system bus provides a single 64-bit data bus and a single 32-bit address bus. The external port supports data transfer rates of 1G bytes per second over the external bus.

The external bus can be configured for 32- or 64-bit, little-endian operations. When the system bus is configured for 64-bit operations, the lower 32 bits of the external data bus connect to even addresses, and the upper 32 bits connect to odd addresses.

The external port supports pipelined, slow, and SDRAM protocols. Addressing of external memory devices and memory-mapped peripherals is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals.

The ADSP-TS201S processor provides programmable memory, pipeline depth, and idle cycle for synchronous accesses, and external acknowledge controls to support interfacing to pipelined or slow devices, host processors, and other memory-mapped peripherals with variable access, hold, and disable time requirements.

Host Interface
The ADSP-TS201S processor provides an easy and configurable interface between its external bus and host processors through the external port. To accommodate a variety of host processors, the host interface supports pipelined or slow protocols for ADSP-TS201S processor accesses of the host as slave or pipelined for host accesses of the ADSP-TS201S processor as slave. Each protocol has programmable transmission parameters, such as idle cycles, pipe depth, and internal wait cycles.

The host interface supports burst transactions initiated by a host processor. After the host issues the starting address of the burst and asserts the $\overline{\text{BRST}}$ signal, the DSP increments the address internally while the host continues to assert $\overline{\text{BRST}}$.

The host interface provides a deadlock recovery mechanism that enables a host to recover from deadlock situations involving the DSP. The $\overline{\text{BOFF}}$ signal provides the deadlock recovery mechanism. When the host asserts $\overline{\text{BOFF}}$, the DSP backs off the current transaction and asserts $\overline{\text{HBG}}$ and relinquishes the external bus.

The host can directly read or write the internal memory of the ADSP-TS201S processor, and it can access most of the DSP registers, including DMA control (TCB) registers. Vector interrupts support efficient execution of host commands.

Multiprocessor Interface
The ADSP-TS201S processor offers powerful features tailored to multiprocessing DSP systems through the external port and link ports. This multiprocessing capability provides highest bandwidth for interprocessor communication, including:

- Up to eight DSPs on a common bus
- On-chip arbitration for glueless multiprocessing
- Link ports for point to point communication

The external port and link ports provide integrated, glueless multiprocessing support.

The external port supports a unified address space (see Figure 2) that enables direct interprocessor accesses of each ADSP-TS201S processor's internal memory and registers. The DSP's on-chip distributed bus arbitration logic provides simple, glueless connection for systems containing up to eight ADSP-TS201S processors and a host processor. Bus arbitration has a rotating priority. Bus lock supports indivisible read-modify-write sequences for semaphores. A bus fairness feature prevents one DSP from holding the external bus too long.

The DSP's four link ports provide a second path for interprocessor communications with throughput of 4G bytes per second. The cluster bus provides 1G bytes per second throughput—with a total of 4G bytes per second interprocessor bandwidth (limited by SOC bandwidth).

SDRAM Controller
The SDRAM controller controls the ADSP-TS201S processor's transfers of data to and from external synchronous DRAM (SDRAM) at a throughput of 32 or 64 bits per SCLK cycle using the external port and SDRAM control pins.

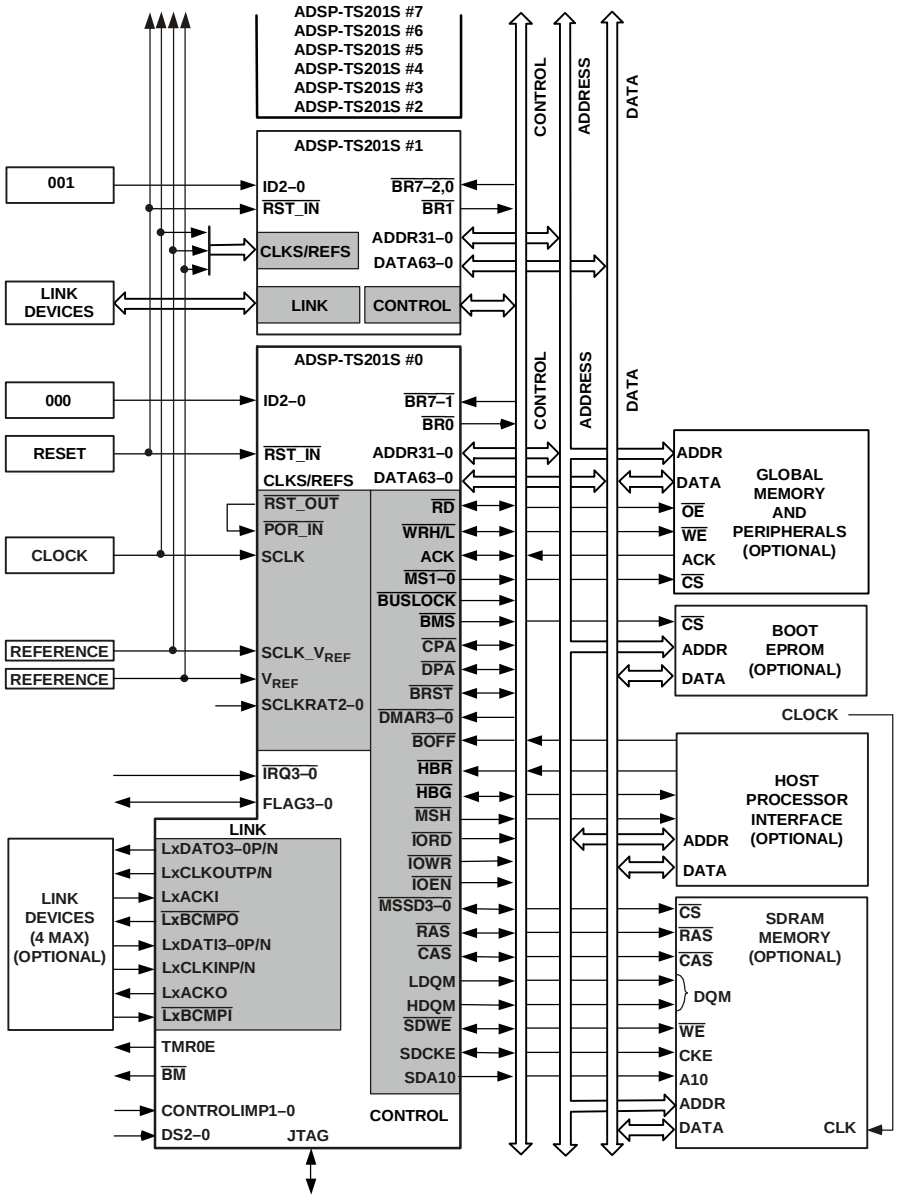


Figure 3. ADSP-TS201S Shared Memory Multiprocessing System

The SDRAM interface provides a glueless interface with standard SDRAMs—16M bit, 64M bit, 128M bit, and 256M bit. The DSP supports directly a maximum of four banks of 64M words × 32 bit of SDRAM. The SDRAM interface is mapped in external memory in each DSP's unified memory map.

EPROM Interface

The ADSP-TS201S processor can be configured to boot from an external 8-bit EPROM at reset through the external port. An automatic process (which follows reset) loads a program from the EPROM into internal memory. This process uses sixteen wait cycles for each read access. During booting, the $\overline{\text{BMS}}$ pin functions as the EPROM chip select signal. The EPROM boot procedure uses DMA channel 0, which packs the bytes into 32-bit instructions. Applications can also access the EPROM (write flash memories) during normal operation through DMA.

The EPROM or Flash Memory interface is not mapped in the DSP's unified memory map. It is a byte address space limited to a maximum of 16M bytes (twenty-four address bits). The EPROM or Flash Memory interface can be used after boot via a DMA.

DMA Controller

The ADSP-TS201S processor's on-chip DMA controller, with 14 DMA channels, provides zero-overhead data transfers without processor intervention. The DMA controller operates indepen-

dently and invisibly to the DSP's core, enabling DMA operations to occur while the DSP's core continues to execute program instructions.

The DMA controller performs DMA transfers between internal memory and external memory and memory-mapped peripherals, the internal memory of other DSPs on a common bus, a host processor, or link port I/O; between external memory and external peripherals or link port I/O; and between an external bus master and internal memory or link port I/O. The DMA controller performs the following DMA operations:

- External port block transfers. Four dedicated bidirectional DMA channels transfer blocks of data between the DSP's internal memory and any external memory or memory-mapped peripheral on the external bus. These transfers support master mode and handshake mode protocols.
- Link port transfers. Eight dedicated DMA channels (four transmit and four receive) transfer quad-word data only between link ports and between a link port and internal or external memory. These transfers only use handshake mode protocol. DMA priority rotates between the four receive channels.
- AutoDMA transfers. Two dedicated unidirectional DMA channels transfer data received from an external bus master to internal memory or to link port I/O. These transfers only use slave mode protocol, and an external bus master must initiate the transfer.

The DMA controller provides these additional features:

- Flyby transfers. Flyby operations only occur through the external port (DMA channel 0) and do not involve the DSP's core. The DMA controller acts as a conduit to transfer data from an I/O device to external SDRAM memory. During a transaction, the DSP relinquishes the external data bus; outputs addresses, memory selects ($\overline{\text{MSSD}}$3–0) and the $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{IOEN}}$, and $\overline{\text{RD}}$/$\overline{\text{WR}}$ strobes; and responds to ACK.
- DMA chaining. DMA chaining operations enable applications to automatically link one DMA transfer sequence to another for continuous transmission. The sequences can occur over different DMA channels and have different transmission attributes.
- Two-dimensional transfers. The DMA controller can access and transfer two-dimensional memory arrays on any DMA transmit or receive channel. These transfers are implemented with index, count, and modify registers for both the X and Y dimensions.

Link Ports (LVDS)

The DSP's four full-duplex link ports each provide additional four-bit receive and four-bit transmit I/O capability, using Low-Voltage, Differential-Signal (LVDS) technology. With the ability to operate at a double data rate—latching data on both the rising and falling edges of the clock—running at 500 MHz, each link port can support up to 500M bytes per second per direction, for a combined maximum throughput of 4G bytes per second.

The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications. Applications can also use the link ports for booting.

Each link port has its own triple-buffered quad-word input and double-buffered quad-word output registers. The DSP's core can write directly to a link port's transmit register and read from a receive register, or the DMA controller can perform DMA transfers through eight (four transmit and four receive) dedicated link port DMA channels.

Each link port direction has three signals that control its operation. For the transmitter, LxCLKOUT is the output transmit clock, LxACKI is the handshake input to control the data flow, and the $\overline{\text{LxBCMPO}}$ output indicates that the block transfer is complete. For the receiver, LxCLKIN is the input receive clock, LxACKO is the handshake output to control the data flow, and the $\overline{\text{LxBCMPI}}$ input indicates that the block transfer is complete. The LxDATO3–0 pins are the data output bus for the transmitter and the LxDATI3–0 pins are the input data bus for the receiver.

Applications can program separate error detection mechanisms for transmit and receive operations (applications can use the checksum mechanism to implement consecutive link port transfers), the size of data packets, and the speed at which bytes are transmitted.

Timer and General-Purpose I/O

The ADSP-TS201S processor has a timer pin (TMR0E) that generates output when a programmed timer counter has expired and four programmable general-purpose I/O pins (FLAG3–0) that can function as either single-bit input or output. As outputs, these pins can signal peripheral devices; as inputs, they can provide the test for conditional branching.

Reset and Booting

The ADSP-TS201S processor has three levels of reset:

- Power-up reset—After power-up of the system (SCLK, all static inputs, and strap pins are stable), the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- Normal reset—For any chip reset following the power-up reset, the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- DSP-core reset—When setting the SWRST bit in EMUCTL, the DSP core is reset, but not the external port or I/O.

For normal operations, tie the $\overline{\text{RST\_OUT}}$ pin to the $\overline{\text{POR\_IN}}$ pin.

After reset, the ADSP-TS201S processor has four boot options for beginning operation:

- Boot from EPROM.
- Boot by an external master (host or another ADSP-TS201S processor).

- Boot by link port.
- No boot—Start running from memory address selected with one of the $\overline{\text{IRQ3–0}}$ interrupt signals. See Table 2.

Using the 'no boot' option, the ADSP-TS201S processor must start running from memory when one of the interrupts is asserted.

Table 2. No Boot, Run From Memory Addresses

Interrupt	Address
$\overline{\text{IRQ0}}$	0x3000 0000 (External Memory)
$\overline{\text{IRQ1}}$	0x3800 0000 (External Memory)
$\overline{\text{IRQ2}}$	0x8000 0000 (External Memory)
$\overline{\text{IRQ3}}$	0x0000 0000 (Internal Memory)

The ADSP-TS201S processor core always exits from reset in the idle state and waits for an interrupt. Some of the interrupts in the interrupt vector table are initialized and enabled after reset.

For more information on boot options, see the *EE-174: ADSP-TS101S Booting Methods* on the Analog Devices website (www.analog.com)

Clock Domains

The DSP uses calculated ratios of the SCLK clock to operate as shown in Figure 4. The instruction execution rate is equal to CCLK. A PLL from SCLK generates CCLK which is phase-locked. The SCLKRATx pins define the clock multiplication of SCLK to CCLK (see Table 4 on page 11). The link port clock is generated from CCLK via a software programmable divisor, and the SOC bus operates at 1/2 CCLK. Memory transfers to external and link port buffers operate at the SOCCLK rate. SCLK also provides clock input for the external bus interface and defines the AC specification reference for the external bus signals. The external bus interface runs at the SCLK frequency. The maximum SCLK frequency is one quarter the internal DSP clock (CCLK) frequency.

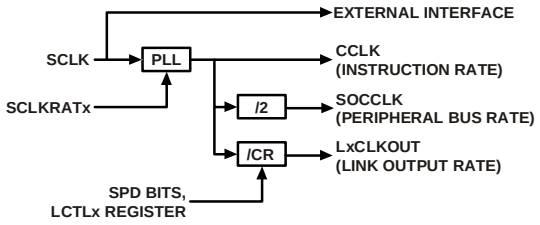


Figure 4. Clock Domains

Power Domains

The ADSP-TS201S processor has separate power supply connections for internal logic (V_{DD}), analog circuits (V_{DD_A}), I/O buffer (V_{DD_IO}), and internal DRAM (V_{DD_DRAM}) power supply.

Note that the analog (V_{DD_A}) supply powers the clock generator PLLs. To produce a stable clock, systems must provide a clean power supply to power input V_{DD_A}. Designs must pay critical attention to bypassing the V_{DD_A} supply.

Filtering Reference Voltage and Clocks

Figure 5 and Figure 6 show possible circuits for filtering V_{REF}, and SCLK_V_{REF}. These circuits provide the reference voltages for the switching voltage reference and system clock reference.

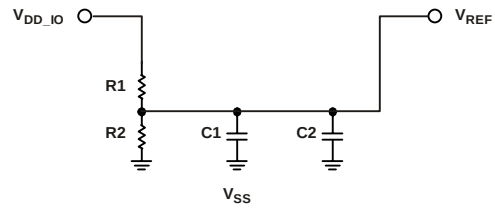


Figure 5. V_{REF} filtering scheme

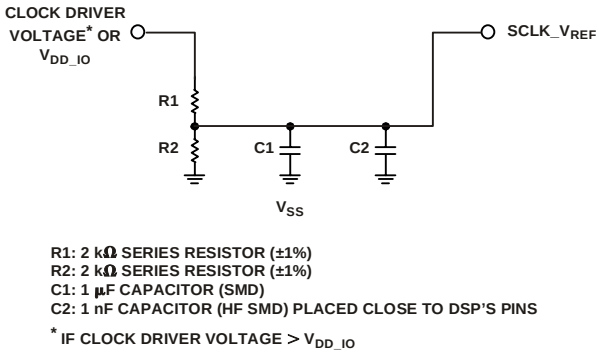


Figure 6. SCLK_V_{REF} filtering scheme

Development Tools

The ADSP-TS201S processor is supported with a complete set of CROSSCORE[2] software and hardware development tools, including Analog Devices emulators and VisualDSP++[3] development environment. The same emulator hardware that supports other TigerSHARC processors also fully emulates the ADSP-TS201S processor.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for theses tools is C/C++ code

[2] CROSSCORE is a trademark of Analog Devices, Inc.
[3] VisualDSP++ is a trademark of Analog Devices, Inc.

efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The DSP has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the realtime characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the TigerSHARC processor development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permit programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++™ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include Threads, Critical and Unscheduled regions, Semaphores, Events, and Device flags. The VDK also supports Priority-based, Preemptive, Cooperative and Time -Sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++™ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK based objects, and visualizing the system state, when debugging an application that uses the VDK.

VCSE is Analog Devices' technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. Download components from the Web and drop them into the application. Publish component archives from within VisualDSP++™. VCSE supports component implementation in C/C++ or assembly language.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the DSP or external memory with the drag of the mouse, examine run-time stack and heap usage. The Expert Linker is fully compatible with existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices DSP emulators use the IEEE 1149.1 JTAG Test Access Port of the ADSP-TS201S processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the TigerSHARC processor family. Hardware tools include TigerSHARC processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. The emulator uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68". This document is updated regularly to keep pace with improvements to emulator support.

Additional Information

This data sheet provides a general overview of the ADSP-TS201S processor's architecture and functionality. For detailed information on the ADSP-TS201S processor's core architecture and instruction set, see the *ADSP-TS201 TigerSHARC Processor Hardware Reference* and the *ADSP-TS201 TigerSHARC Processor Programming Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide for TigerSHARC Processors*.

PIN FUNCTION DESCRIPTIONS

While most of the ADSP-TS201S processor's input pins are normally synchronous—tied to a specific clock—a few are asynchronous. For these asynchronous signals, an on-chip synchronization circuit prevents metastability problems. Use the AC specification for asynchronous signals when the system design requires predictable, cycle-by-cycle behavior for these signals.

The output pins can be three-stated during normal operation. The DSP three-states all outputs during reset, allowing these pins to get to their internal pullup or pulldown state. Some pins have an internal pullup or pulldown resistor (±30% tolerance) that maintains a known value during transitions between different drivers.

Table 3. Pin Definitions—Clocks and Reset

Signal	Type	Description
SCLKRAT2–0	I (pd)	Core Clock Ratio. The DSP's core clock (CCLK) rate = n × SCLK, where n is user-programmable using the SCLKRATx pins to the values shown in Table 4. These pins must have a constant value while the DSP is powered. The core clock rate (CCLK) is the instruction cycle rate.
SCLK	I[1]	System Clock Input. The DSP's system input clock for cluster bus.The core clock rate is user-programmable using the SCLKRATx pins. For more information, see Clock Domains on page 9.
$\overline{\text{RST\_IN}}$	I/A	Reset. Sets the DSP to a known state and causes program to be in idle state. $\overline{\text{RST\_IN}}$ must be asserted a specified time according to the type of reset operation. For details, see Reset and Booting on page 8, Table 19 on page 22, and Figure 9 on page 23.
$\overline{\text{RST\_OUT}}$	O	Reset Output. Indicates that the DSP reset is complete. Connect to $\overline{\text{POR\_IN}}$.
$\overline{\text{POR\_IN}}$	I/A	Power On Reset for internal DRAM. Connect to $\overline{\text{RST\_OUT}}$.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

[1] For more information on SCLK and SCLK_V_{REF} on revision 0.0 silicon, see the *EE-179: ADSP-TS201S System Design Guidelines* on the Analog Devices website (www.analog.com).

Table 4. SCLK Ratio

SCLKRAT2–0	Ratio
000 (default)	4
001	5
010	6
011	7
100	8
101	10
110	12
111	Reserved

Table 5. Pin Definitions—External Port Bus Controls

Signal	Type	Description
ADDR31–0	I/O/T (pu_ad)	Address Bus. The DSP issues addresses for accessing memory and peripherals on these pins. In a multiprocessor system, the bus master drives addresses for accessing internal memory or I/O processor registers of other ADSP-TS201S processors. The DSP inputs addresses when a host or another DSP accesses its internal memory or I/O processor registers.
DATA63–0	I/O/T (pu_ad)	External Data Bus. The DSP drives and receives data and instructions on these pins. Pullup/down resistors on unused DATA pins are unnecessary.
$\overline{RD}$	I/O/T (pu_0)	Memory Read. $\overline{RD}$ is asserted whenever the DSP reads from any slave in the system, excluding SDRAM. When the DSP is a slave, $\overline{RD}$ is an input and indicates read transactions that access its internal memory or universal registers. In a multiprocessor system, the bus master drives $\overline{RD}$. $\overline{RD}$ changes concurrently with ADDR pins.
$\overline{WRL}$	I/O/T (pu_0)	Write Low. $\overline{WRL}$ is asserted in two cases: When the ADSP-TS201S processor writes to an even address word of external memory or to another external bus agent; and when the ADSP-TS201S processor writes to a 32-bit zone (host, memory or DSP programmed to 32-bit bus). An external master (host or DSP) asserts $\overline{WRL}$ for writing to a DSP's low word of internal memory. In a multiprocessor system, the bus master drives $\overline{WRL}$. $\overline{WRL}$ changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRL}$ is an input and indicates write transactions that access its internal memory or universal registers.
$\overline{WRH}$	I/O/T (pu_0)	Write High. $\overline{WRH}$ is asserted when the ADSP-TS201S processor writes a long word (64 bits) or writes to an odd address word of external memory or to another external bus agent on a 64-bit data bus. An external master (host or another DSP) must assert $\overline{WRH}$ for writing to a DSP's high word of 64-bit data bus. In a multiprocessing system, the bus master drives $\overline{WRH}$. $\overline{WRH}$ changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRH}$ is an input and indicates write transactions that access its internal memory or universal registers.
ACK	I/O/T/OD (pu_od_0)	Acknowledge. External slave devices can de-assert ACK to add wait states to external memory accesses. ACK is used by I/O devices, memory controllers and other peripherals on the data phase. The DSP can de-assert ACK to add wait states to read and write accesses of its internal memory. The pullup is 50 Ω on low-to-high transactions and is 500 Ω on all other transactions.
$\overline{BMS}$	O/T (pu_0)	Boot Memory Select. $\overline{BMS}$ is the chip select for boot EPROM or flash memory. During reset, the DSP uses $\overline{BMS}$ as a strap pin (EBOOT) for EPROM boot mode. In a multiprocessor system, the DSP bus master drives $\overline{BMS}$. For details, see Reset and Booting on page 8 and see the EBOOT signal description in Table 15 on page 18.
$\overline{MS1–0}$	O/T (pu_0)	Memory Select. $\overline{MS0}$ or $\overline{MS1}$ is asserted whenever the DSP accesses memory banks 0 or 1 respectively. $\overline{MS1–0}$ are decoded memory address pins that change concurrently with ADDR pins. When ADDR31:27 = 0b00110, $\overline{MS0}$ is asserted. When ADDR31:27 = 0b00111, $\overline{MS1}$ is asserted. In multiprocessor systems, the master DSP drives $\overline{MS1–0}$.
$\overline{MSH}$	O/T (pu_0)	Memory Select Host. $\overline{MSH}$ is asserted whenever the DSP accesses the host address space (ADDR31 = 0b1). $\overline{MSH}$ is a decoded memory address pin that changes concurrently with ADDR pins. In a multiprocessor system, the bus master DSP drives $\overline{MSH}$.
$\overline{BRST}$	I/O/T (pu_0)	Burst. The current bus master (DSP or host) asserts this pin to indicate that it is reading or writing data associated with consecutive addresses. A slave device can ignore addresses after the first one and increment an internal address counter after each transfer. For host-to-DSP burst accesses, the DSP increments the address automatically while $\overline{BRST}$ is asserted.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 6. Pin Definitions—External Port Arbitration

Signal	Type	Description
$\overline{BR7–0}$	I/O	Multiprocessing Bus Request Pins. Used by the DSPs in a multiprocessor system to arbitrate for bus mastership. Each DSP drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In systems with fewer than eight DSPs, set the unused $\overline{BRx}$ pins high (V_{DD_IO}).
ID2–0	I (pd)	Multiprocessor ID. Indicates the DSP's ID, from which the DSP determines its order in a multiprocessor system. These pins also indicate to the DSP which bus request ($\overline{BR0}$–$\overline{BR7}$) to assert when requesting the bus: 000 = $\overline{BR0}$, 001 = $\overline{BR1}$, 010 = $\overline{BR2}$, 011 = $\overline{BR3}$, 100 = $\overline{BR4}$, 101 = $\overline{BR5}$, 110 = $\overline{BR6}$, or 111 = $\overline{BR7}$. ID2–0 must have a constant value during system operation and can change during reset only.
$\overline{BM}$	O	Bus Master. The current bus master DSP asserts $\overline{BM}$. For debugging only. At reset this is a strap pin. For more information, see Table 15 on page 18.
$\overline{BOFF}$	I	Back Off. A deadlock situation can occur when the host and a DSP try to read from each other's bus at the same time. When deadlock occurs, the host can assert $\overline{BOFF}$ to force the DSP to relinquish the bus before completing its outstanding transaction.
$\overline{BUSLOCK}$	O/T (pu_0)	Bus Lock Indication. Provides an indication that the current bus master has locked the bus. At reset, this is a strap pin. For more information, see Table 15 on page 18.
$\overline{HBR}$	I	Host Bus Request. A host must assert $\overline{HBR}$ to request control of the DSP's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the bus master relinquishes the bus and asserts $\overline{HBG}$ once the outstanding transaction is finished.
$\overline{HBG}$	I/O/T (pu_0)	Host Bus Grant. Acknowledges $\overline{HBR}$ and indicates that the host can take control of the external bus. When relinquishing the bus, the master DSP three-states the ADDR31–0, DATA63–0, $\overline{MSH}$, $\overline{MSSD3–0}$, $\overline{MS1–0}$, $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{BMS}$, $\overline{BRST}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{IOEN}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, SDCKE, LDQM and HDQM pins, and the DSP puts the SDRAM in self-refresh mode. The DSP asserts $\overline{HBG}$ until the host deasserts $\overline{HBR}$. In multiprocessor systems, the current bus master DSP drives $\overline{HBG}$, and all slave DSPs monitor it.
$\overline{CPA}$	I/O/OD (pu_od_0)	Core Priority Access. Asserted while the DSP's core accesses external memory. This pin enables a slave DSP to interrupt a master DSP's background DMA transfers and gain control of the external bus for core-initiated transactions. $\overline{CPA}$ is an open drain output, connected to all DSPs in the system. If not required in the system, leave $\overline{CPA}$ unconnected (external pullups will be required for DSP ID=1 through ID=7).
$\overline{DPA}$	I/O/OD (pu_od_0)	DMA Priority Access. Asserted while a high-priority DSP DMA channel accesses external memory. This pin enables a high-priority DMA channel on a slave DSP to interrupt transfers of a normal-priority DMA channel on a master DSP and gain control of the external bus for DMA-initiated transactions. $\overline{DPA}$ is an open drain output, connected to all DSPs in the system. If not required in the system, leave $\overline{DPA}$ unconnected (external pullups will be required for DSP ID=1 through ID=7).

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 7. Pin Definitions—External Port DMA/Flyby

Signal	Type	Description
$\overline{\text{DMAR3–0}}$	I/A	DMA Request Pins. Enable external I/O devices to request DMA services from the DSP. In response to $\overline{\text{DMARx}}$, the DSP performs DMA transfers according to the DMA channel's initialization. The DSP ignores DMA requests from uninitialized channels.
$\overline{\text{IOWR}}$	O/T (pu_0)	I/O Write. When a DSP DMA channel initiates a flyby mode read transaction, the DSP asserts the $\overline{\text{IOWR}}$ signal during the data cycles. This assertion makes the I/O device sample the data instead of the TigerSHARC.
$\overline{\text{IORD}}$	O/T (pu_0)	I/O Read. When a DSP DMA channel initiates a flyby mode write transaction, the DSP asserts the $\overline{\text{IORD}}$ signal during the data cycle. This assertion with the $\overline{\text{IOEN}}$ makes the I/O device drive the data instead of the TigerSHARC.
$\overline{\text{IOEN}}$	O/T (pu_0)	I/O Device Output Enable. Enables the output buffers of an external I/O device for fly-by transactions between the device and external memory. Active on fly-by transactions.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground; **pd** = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0; **pu_od_0** = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master; **pu_ad** = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 8. Pin Definitions—External Port SDRAM Controller

Signal	Type	Description
$\overline{\text{MSSD3–0}}$	I/O/T (pu_0)	Memory Select SDRAM. $\overline{\text{MSSD0}}$, $\overline{\text{MSSD1}}$, $\overline{\text{MSSD2}}$, or $\overline{\text{MSSD3}}$ is asserted whenever the DSP accesses SDRAM memory space. $\overline{\text{MSSD3–0}}$ are decoded memory address pins that are asserted whenever the DSP issues an SDRAM command cycle (access to ADDR31:30 = 0b01—except reserved spaces shown in Figure 2 on page 5). In a multiprocessor system, the master DSP drives $\overline{\text{MSSD3–0}}$.
$\overline{\text{RAS}}$	I/O/T (pu_0)	Row Address Select. When sampled low, $\overline{\text{RAS}}$ indicates that a row address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to SDRAM specification.
$\overline{\text{CAS}}$	I/O/T (pu_0)	Column Address Select. When sampled low, $\overline{\text{CAS}}$ indicates that a column address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to the SDRAM specification.
LDQM	O/T (pu_0)	Low Word SDRAM Data Mask. When sampled high, three-states the SDRAM DQ buffers. LDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted, and inactive on read transactions. On write transactions, LDQM is active when accessing an odd address word on a 64-bit memory bus to disable the write of the low word.
HDQM	O/T (pu_0)	High Word SDRAM Data Mask. When sampled high, three-states the SDRAM DQ buffers. HDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted, and inactive on read transactions. On write transactions, HDQM is active when accessing an even address in word accesses or when memory is configured for a 32-bit bus to disable the write of the high word.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground; **pd** = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0; **pu_od_0** = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master; **pu_ad** = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 8. Pin Definitions—External Port SDRAM Controller (continued)

Signal	Type	Description
SDA10	O/T (pu_0)	SDRAM Address bit 10 pin. Separate A10 signals enable SDRAM refresh operation while the DSP executes non-SDRAM transactions.
SDCKE	I/O/T (pu_m/ pd_m)	SDRAM Clock Enable. Activates the SDRAM clock for SDRAM self-refresh or suspend modes. A slave DSP in a multiprocessor system does not have the pullup or pulldown. A master DSP (or ID=0 in a single processor system) has a pullup before granting the bus to the host, except when the SDRAM is put in self refresh mode. In self refresh mode, the master has a pulldown before granting the bus to the host.
$\overline{\text{SDWE}}$	I/O/T (pu_0)	SDRAM Write Enable. When sampled low while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM write access. When sampled high while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM read access. In other SDRAM accesses, $\overline{\text{SDWE}}$ defines the type of operation to execute according to SDRAM specification.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 9. Pin Definitions—JTAG Port

Signal	Type	Description
$\overline{\text{EMU}}$	O/OD	Emulation. Connected to the DSP's JTAG emulator target board connector only.
TCK	I	Test Clock (JTAG). Provides an asynchronous clock for JTAG scan.
TDI	I (pu_ad)	Test Data Input (JTAG). A serial data input of the scan path.
TDO	O/T	Test Data Output (JTAG). A serial data output of the scan path.
TMS	I (pu_ad)	Test Mode Select (JTAG). Used to control the test state machine.
$\overline{\text{TRST}}$	I/A (pu_ad)	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted or pulsed low after power up for proper device operation. For more information, see Reset and Booting on page 8.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20

Table 10. Pin Definitions—Flags, Interrupts, and Timer

Signal	Type	Description
FLAG3–0	I/O/A (pu)	FLAG pins. Bidirectional input/output pins can be used as program conditions. Each pin can be configured individually for input or for output. FLAG3–0 are inputs after power-up and reset.
$\overline{\text{IRQ3–0}}$	I/A (pu)	Interrupt Request. When asserted, the DSP generates an interrupt. Each of the $\overline{\text{IRQ3–0}}$ pins can be independently set for edge-triggered or level-sensitive operation. After reset, these pins are disabled unless the $\overline{\text{IRQ3–0}}$ strap option and interrupt vectors are initialized for booting.
TMR0E	O	Timer 0 expires. This output pulses whenever timer 0 expires. At reset, this is a strap pin. For more information, see Table 15 on page 18.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 11. Pin Definitions—Link Ports

Signal	Type	Description
LxDATO3–0P	O	Link Ports 3–0 Data 3–0 Transmit LVDS P
LxDATO3–0N	O	Link Ports 3–0 Data 3–0 Transmit LVDS N
LxCLKOUTP	O	Link Ports 3–0 Transmit Clock LVDS P
LxCLKOUTN	O	Link Ports 3–0 Transmit Clock LVDS N
LxACKI	I (pd)	Link Ports 3–0 Receive Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission
$\overline{\text{LxBCMPO}}$	O	Link Ports 3–0 Block Completion. When the transmission is executed using DMA, this signal indicates to the receiver that the transmitted block is completed. At reset, the $\overline{\text{L1BCMPO}}$, $\overline{\text{L2BCMPO}}$, and $\overline{\text{L3BCMPO}}$ pins are strap pins. For more information, see Table 15 on page 18.
LxDATI3–0P	I	Link Ports 3–0 Data 3–0 Receive LVDS P
LxDATI3–0N	I	Link Ports 3–0 Data 3–0 Receive LVDS N
LxCLKINP	I/A	Link Ports 3–0 Receive Clock LVDS P
LxCLKINN	I/A	Link Ports 3–0 Receive Clock LVDS N
LxACKO	O	Link Ports 3–0 Transmit Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission.
$\overline{\text{LxBCMPI}}$	I	Link Ports 3–0 Block Completion. When the reception is executed using DMA, this signal indicates to the transmitter that the receive block is completed.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground; **pd** = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0; **pu_od_0** = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master; **pu_ad** = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 12. Pin definitions—Impedance Control , Drive Strength Control, and Regulator Enable

Signal	Type	Description
CONTROLIMP0	I (pd)	Impedance Control. CONTROLIMP0 enables Pulse Mode. When CONTROLIMP0 = 0, Pulse Mode is disabled and the output drive strength is continuously controlled by DS2–0, both in the digital mode and in the analog mode (See analog and digital modes below). When CONTROLIMP0 = 1, Pulse Mode is enabled. In Pulse Mode, whenever a new value is driven to the output pin, drive strength is set to 100% for a short period of 1.5-2.5ns after rising edge of SCLK and afterwards it is set back to the value defined by the resistance control DS2–0 pins as shown in Table 13.
CONTROLIMP1	I (pu)	Impedance Control. CONTROLIMP1 enables A/D mode of the control impedance circuitry.When CONTROLIMP1 = 0, A/D mode is disabled, and output drive strength is set relative to maximum drive strength according to table in DS2–0 explanation. When CONTROLIMP1 = 1, A/D mode is enabled, and the resistance control operates in the analog mode, where drive strength is continuously controlled to match a specific line impedance as shown in Table 13.
DS2,0 DS1	I (pu) I (pd)	Digital Drive Strength Selection. Selected as shown in Table 13. For drive strength calculation, see Output Drive Currents on page 31. The drive strength for some pins is preset, not controlled by the DS2–0 pins. The pins that are always at drive strength 7 (100%) include: $\overline{\text{CPA}}$, $\overline{\text{DPA}}$, TDO, $\overline{\text{EMU}}$, and $\overline{\text{RST\_OUT}}$. The drive strength for the ACK pin is always x2 drive strength 7 (100%).
ENEDREG	I (pu)	Enable on-chip DRAM Regulator. This pin selects whether the internal DRAM is supplied from: 0 = V_{DD_DRAM}; connect V_{DD_DRAM} pins to properly decoupled DRAM power supply 1 = V_{DD_IO}; connect V_{DD_DRAM} pins to bulk and decoupling capacitors only (default)

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground; **pd** = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0; **pu_od_0** = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master; **pu_ad** = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 13. Drive Strength/Output Impedance Selection

DS2–0 Pins	Drive Strength[1]	Output Impedance [2]
000	Strength 0 (11.1%)	120 Ω
001	Strength 1 (23.8%)	96 Ω
010	Strength 2 (36.5%)	70 Ω
011	Strength 3 (49.2%)	62 Ω
100	Strength 4 (61.9%)	50 Ω
101 (default)	Strength 5 (74.6%)	40 Ω
110	Strength 6 (87.3%)	32 Ω
111	Strength 7 (100%)	26 Ω

[1] CONTROLIMP1 = 0, A/D mode disabled.
[2] CONTROLIMP1 = 1, A/D mode enabled.

Table 14. Pin Definitions—Power, Ground, and Reference

Signal	Type	Description
V_{DD}	P	V_{DD} pins for internal logic.
V_{DD_A}	P	V_{DD} pins for analog circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	V_{DD} pins for I/O buffers.
V_{DD_DRAM}	P	V_{DD} pins (optional) for internal DRAM; enabled with ENEDREG pin listed in Table 12.
V_{REF}	I	Reference voltage defines the trip point for all input buffers, except SCLK, $\overline{\text{RST\_IN}}$, $\overline{\text{POR\_IN}}$, $\overline{\text{IRQ3–0}}$, FLAG3–0, $\overline{\text{DMAR3–0}}$, ID2–0, CONTROLIMP1–0, LxDATO3–0P/N, LxCLKOUTP/N, LxDATI3–0P/N, LxCLKINP/N, TCK, TDI, TMS, and $\overline{\text{TRST}}$. V_{REF} can be connected to a power supply or set by a voltage divider circuit as shown in Figure 5. For more information, see Filtering Reference Voltage and Clocks on page 9.
SCLK_V_{REF}	I[1]	System Clock Reference. Connect this pin to a reference voltage as shown in Figure 6. For more information, see Filtering Reference Voltage and Clocks on page 9.
V_{SS}	G	Ground pins.
NC	—	No Connect. Do not connect these pins to anything (not to any supply, signal, or each other). These pins are reserved and must be left unconnected.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

[1] For more information on SCLK and SCLK_V_{REF} on revision 0.0 silicon, see the *EE-179: ADSP-TS201S System Design Guidelines* on the Analog Devices website (www.analog.com).

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set DSP operating modes. During reset, the DSP samples the strap option pins. Strap pins have an internal pullup or pulldown for the default value. If a strap pin is not connected to an overdriving external pullup, pulldown, or logic load, the DSP samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pullup or pulldown may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pullup or pulldown. Table 15 lists and describes each of the DSP's strap pins.

Table 15. Pin Definitions—I/O Strap Pins

Signal	Type (at Reset)	On Pin…	Description
EBOOT	I (pd_0)	$\overline{\text{BMS}}$	EPROM boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot DSP through the external port or a link port
IRQEN	I (pd)	$\overline{\text{BM}}$	Interrupt Enable. 0 = disable and set $\overline{\text{IRQ3–0}}$ interrupts to level-sensitive after reset (default) 1 = enable and set $\overline{\text{IRQ3–0}}$ interrupts to edge-sensitive immediately after reset
LINK_DWIDTH	I (pd)	TMR0E	Link Port Input Default Data Width. 0 = 1-bit (default) 1 = 4-bit

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

Table 15. Pin Definitions—I/O Strap Pins (continued)

Signal	Type (at Reset)	On Pin...	Description
SYS_REG_WE	I (pd_0)	$\overline{\text{BUSLOCK}}$	SYSCON and SDRCON Write Enable. 0 = one-time writable after reset (default) 1 = always writable
TM1	I (pu)	$\overline{\text{L1BCMPO}}$	Test Mode 1. Do not overdrive default value during reset.
TM2	I (pu)	$\overline{\text{L2BCMPO}}$	Test Mode 2. Do not overdrive default value during reset.
TM3	I (pu)	$\overline{\text{L3BCMPO}}$	Test Mode 3. Do not overdrive default value during reset.

I = input; **A** = asynchronous; **O** = output; **OD** = open drain output; **T** = Three-State; **P** = power supply; **G** = ground;
pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0;
pu_od_0 = internal pullup 500Ω on DSP ID=0; **pd_m** = internal pulldown 5 kΩ on DSP bus master; **pu_m** = internal pullup 5 kΩ on DSP bus master;
pu_ad = internal pullup 40 kΩ; For more pulldown and pullup information, see Electrical characteristics on page 20.

When default configuration is used, no external resistor is needed on the strap pins. To apply other configurations, a 500Ω resistor connected to V_{DD_IO} is required. If providing external pulldowns, do not strap these pins directly to V_{SS}; the strap pins require 500Ω resistor straps.

All strap pins are sampled on the rising edge of $\overline{\text{RST\_IN}}$ (de-assertion edge). Each pin latches the strapped pin state (state of the strap pin at the rising edge of $\overline{\text{RST\_IN}}$). Shortly after de-assertion of $\overline{\text{RST\_IN}}$, these pins are re-configured to their normal functionality.

These strap pins have an internal pull-down resistor, pull-up resistor, or no-resistor (three-state) on each pin. The resistor type, which is connected to the I/O pad, depends on whether $\overline{\text{RST\_IN}}$ is active (low) or if $\overline{\text{RST\_IN}}$ is de-asserted (high). Table 16 shows the resistors that are enabled during active reset and during normal operation

Table 16. Strap Pin Internal Resistors—Active Reset ($\overline{\text{RST\_IN}}$ = 0) Versus Normal Operation ($\overline{\text{RST\_IN}}$ = 1)

PIN	$\overline{\text{RST\_IN}}$ = 0	$\overline{\text{RST\_IN}}$ = 1
$\overline{\text{BMS}}$	(pd_0)	(pu_0)
$\overline{\text{BM}}$	(pd)	Driven
TMR0E	(pd)	Driven
$\overline{\text{BUSLOCK}}$	(pd_0)	(pu_0)
$\overline{\text{L1BCMPO}}$	(pu)	Driven
$\overline{\text{L2BCMPO}}$	(pu)	Driven
$\overline{\text{L3BCMPO}}$	(pu)	Driven

pd = internal pulldown 5 kΩ; **pu** = internal pullup 5 kΩ; **pd_0** = internal pulldown 5 kΩ on DSP ID=0; **pu_0** = internal pullup 5 kΩ on DSP ID=0

ADSP-TS201S—SPECIFICATIONS

Note that component specifications are subject to change without notice. For information on Link port electrical characteristics, see Link Port Low-Voltage, Differential-Signal (LVDS) Electrical Characteristics and Timing on page 26.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{DD}	Internal Supply Voltage		0.95		1.05	V
V_{DD_A}	Analog Supply Voltage		0.95		1.05	V
V_{DD_IO}	I/O Supply Voltage		2.38		2.63	V
V_{DD_DRAM}	Internal DRAM Supply Voltage		1.425		1.575	V
T_{CASE}	Case Operating Temperature		–40		+85	°C
V_{IH}	High-Level Input Voltage[1]	@ V_{DD}, V_{DD_IO} = max	1.7		3.63	V
V_{IL}	Low-Level Input Voltage[1]	@ V_{DD}, V_{DD_IO} = min	–0.5		0.8	V
I_{DD}	V_{DD} supply current for typical activity[2]	@ CCLK=500 MHz, V_{DD}=1.0 V, T_{CASE}=25°C		2.39		A
I_{DD_IO}	V_{DD_IO} supply current for typical activity[2] (DRAM Internal Regulator Disabled)	@ SCLK=100 MHz, V_{DD_IO}=2.5 V, T_{CASE}=25°C, ENEDREG=0		0.16		A
I_{DD_IO}	V_{DD_IO} supply current for typical activity[2] (DRAM Internal Regulator Enabled)	@ SCLK=100 MHz, V_{DD_IO}=2.5 V, T_{CASE}=25°C, ENEDREG=1		0.83		A
I_{DD_DRAM}	V_{DD_DRAM} supply current for typical activity[2,3]	@ CCLK=500 MHz, V_{DD_DRAM}=1.5 V, T_{CASE}=25°C, ENEDREG=0		0.67		A
V_{REF}	Voltage reference		(V_{DD_IO}/2) ±5%			V
SCLK_V_{REF}	Voltage reference		(V_{DD_IO}/2) ±5%[4]			V

[1]Applies to input and bidirectional pins.
[2]For details on internal and external power calculation issues, see the *EE-170, Estimating Power for the ADSP-TS201S* on the Analog Devices website.
[3]For ENEDREG=1, the internal DRAM supply is used; there is no I_{DD_DRAM} for this condition.
[4]If the clock driver voltage > V_{DD_IO} and the clock driver voltage is used to generate SCLK_V_{REF}, this formula becomes: (V_{CLOCK_DRIVE}/2) ±5%.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High-Level Output Voltage[1]	@V_{DD_IO} = min, I_{OH} = –2 mA	2.18		V
V_{OL}	Low-Level Output Voltage[1]	@V_{DD_IO} = min, I_{OL} = 4 mA		0.4	V
I_{IH}	High-Level Input Current	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max		10	µA
I_{IH_PD}	High-Level Input Current	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max	0.4	0.76	mA
I_{IL}	Low-Level Input Current	@V_{DD_IO} = max, V_{IN} = 0V		10	µA
I_{IL_PU}	Low-Level Input Current	@V_{DD_IO} = max, V_{IN} = 0V	0.4	0.76	mA
$I_{IL\_PU\_AD}$	Low-Level Input Current	@V_{DD_IO} = max, V_{IN} = 0V	0.05	0.1	mA
I_{OZH}	Three-State Leakage Current High	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max		10	µA
I_{OZH_PD}	Three-State Leakage Current High	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max	0.4	0.76	mA
I_{OZL}	Three-State Leakage Current Low	@V_{DD_IO} = max, V_{IN} = 0V		10	µA
I_{OZL_PU}	Three-State Leakage Current Low	@V_{DD_IO} = max, V_{IN} = 0	0.4	0.76	mA
$I_{OZL\_PU\_AD}$	Three-State Leakage Current Low	@V_{DD_IO} = max, V_{IN} = 0	0.05	0.1	mA
I_{OZL_OD}	Three-State Leakage Current Low	@V_{DD_IO} = max, V_{IN} = 0V	4	7.6	mA
C_{IN}	Input Capacitance[2,3]	@f_{IN} = 1MHz,T_{CASE} = 25C, V_{IN} = 2.5V		3	pF

Parameter name suffix conventions: no suffix = applies to pins without pullup or pull down resistors, **_PD** = applies to pin types (pd) or (pd_0), **_PU** = applies to pin types (pu) or (pu_0), **_PU_AD** = applies to pin types (pu_ad), **_OD** = applies to pin types OD

[1]Applies to output and bidirectional pins.
[2]Applies to all signals.
[3]Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

Internal (Core) Supply Voltage (V_{DD})[1] . . . –0.3 V to +1.40 V
Analog (PLL) Supply Voltage (V_{DD_A})[1] . . . –0.3 V to +1.40 V
External (I/O) Supply Voltage (V_{DD_IO})[1] . . . –0.3 V to +3.5 V
External (DRAM) Supply Voltage (V_{DD_DRAM})[1]–0.3 V to +2.1 V
Input Voltage[1] . . . . . –0.5 V to 3.63 V
Output Voltage Swing[1] . . . . . .–0.5 V to V_{DD_IO} + 0.5 V
Storage Temperature Range[1] . . . . . .–65°C to +150°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-TS201S features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

With the exception of $\overline{\text{DMAR3–0}}$, $\overline{\text{IRQ3–0}}$, TMR0E, and FLAG3–0 (input only) pins, all AC timing for the ADSP-TS201S processor is relative to a reference clock edge. Because input setup/hold, output valid/hold, and output enable/disable times are relative to a clock edge, the timing data for the ADSP-TS201S processor has few calculated (formula-based) values. For information on AC timing, see General AC Timing on page 21. For information on Link port transfer timing, see Link Port Low-Voltage, Differential-Signal (LVDS) Electrical Characteristics and Timing on page 26.

General AC Timing

Timing is measured on signals when they cross the 1.25 V level as described in Figure 10 on page 25. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.25 V and the point that the second signal reaches 1.25 V.

The general AC timing data appears in Table 18 and Table 22.

The AC asynchronous timing data for the $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, FLAG3–0, and TMR0E pins appears in Table 17.

Table 17. AC Asynchronous Signal Specifications (all values in this table are in nanoseconds)

Name	Description	Pulsewidth Low (min)	Pulsewidth High (min)
$\overline{IRQ3–0}$[1]	Interrupt Request	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
$\overline{DMAR3–0}$[1]	DMA Request	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
FLAG3–0[2]	FLAG3–0 Input	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
TMR0E[3]	Timer 0 Expired	$4 \times t_{SCLK}$ ns	–

[1]These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference.
[2]For output specifications on FLAG3–0 pins, see Table 22.
[3]This pin is a strap option. During reset, an internal resistor pulls the pin low.

Table 18. Reference Clocks

Signal	Type	Description	Speed Grade (MHz)	Clock Cycle Min (ns)	Clock Cycle Max (ns)	Clock High Min (ns)	Clock Low Min (ns)	Input Jitter[1] Tolerance (ps)
CCLK[2]	–	Core Clock	500	2.0	12.5	–	–	–
SCLK[3,4]	I	System Clock	All	Greater of 8 or CCLK×4	50	{40% to 60% Duty Cycle}		100
TCK	I	Test Clock (JTAG)	All	Greater of 30 or CCLK×4	–	12	12	–

[1]Actual input jitter should be combined with ac specifications for accurate timing analysis.
[2]CCLK is the internal DSP clock or instruction cycle time. The period of this clock is equal to the System Clock (SCLK) period divided by the System Clock Ratio (SCLKRAT2–0). For information on available internal DSP clock rates, see the Ordering Guide on page 40.
[3]For more information, see Table 3 on page 11.
[4]For more information, see Clock Domains on page 9.

Table 19. Power-Up Reset Timing

Parameter		Min	Max	Units
Timing Requirements				
t_{VDD_DRAM}[1]	V_{DD_DRAM} Stable After V_{DD}, V_{DD_A}, V_{DD_IO} Stable	0		ms
$t_{VDD\_DRAM\_RAMP}$	V_{DD_DRAM} Supply Rise Time		0.2	ms

[1]Applies only when the internal DRAM regulator is disabled (ENEDREG=0)

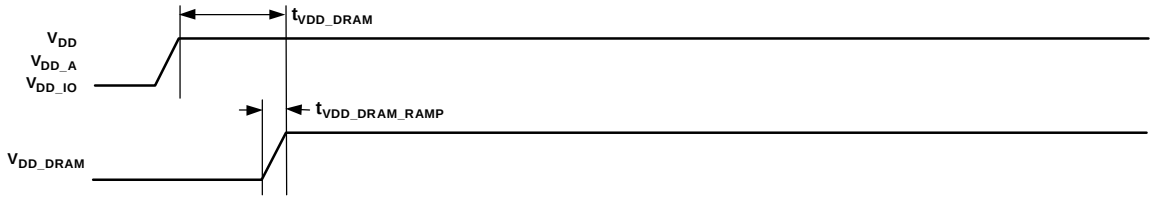


Figure 7. Power-Up Timing

Table 20. Power-Up Reset Timing

Parameter		Min	Max	Units
Timing Requirements				
t_{RST_PWR}	$\overline{RST\_IN}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM} (ENEDREG=0), SCLK, and Static/Strap Pins Stable	2		ms
$t_{TRST\_IN\_PWR}$[1]	$\overline{TRST}$ Asserted During Power-Up Reset	$100 \times t_{SCLK}$		ns
Switching Characteristic				
$t_{RST\_OUT\_PWR}$	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

[1]Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM} (ENEDREG=0), and SCLK are stable and before $\overline{RST\_IN}$ deasserted.

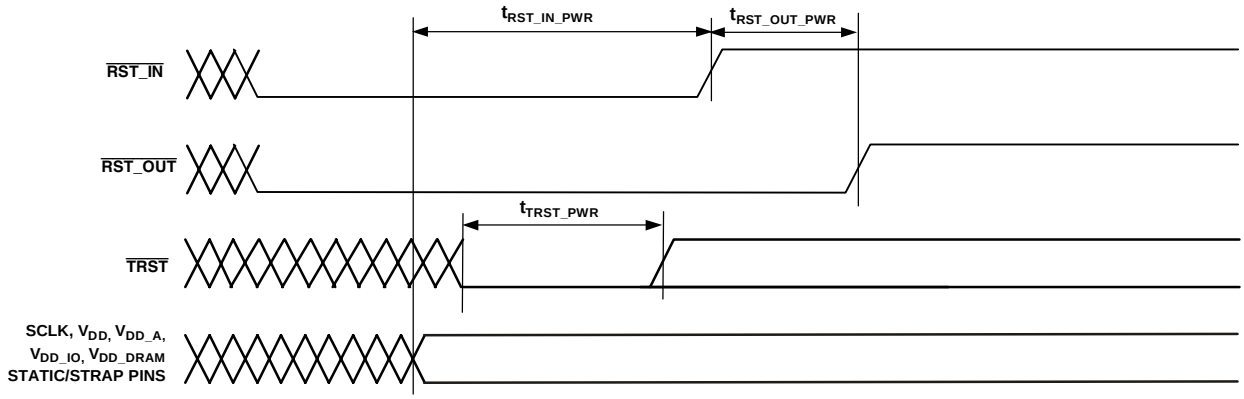


Figure 8. Power-Up Reset Timing

Table 21. Normal Reset Timing

Parameter		Min	Max	Units
Timing Requirements				
t_{RST_IN}	$\overline{RST\_IN}$ Asserted	2		ms
t_{STRAP}	$\overline{RST\_IN}$ Deasserted After Strap Pins Stable	1.5		ms
Switching Characteristic				
t_{RST_OUT}	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

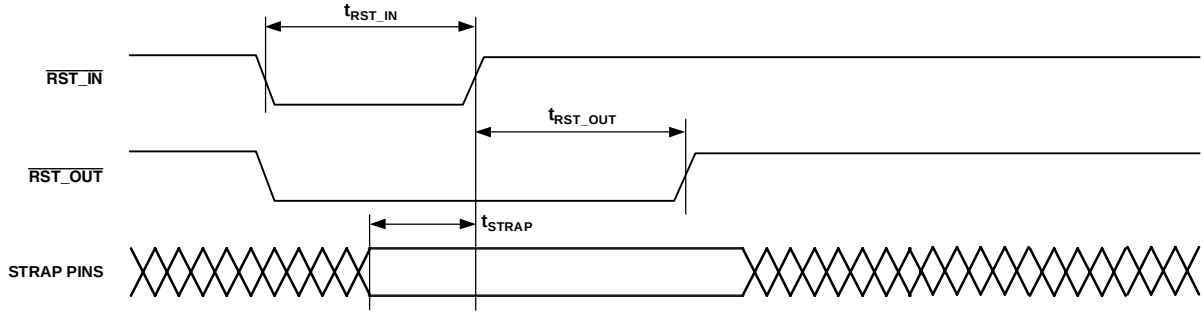


Figure 9. Normal Reset Timing

Table 22. AC Signal Specifications (all values in this table are in nanoseconds)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)	Output Hold (min)	Output Enable (min)[1]	Output Disable (max)[1]	Reference Clock
ADDR31–0	External Address Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
DATA63–0	External Data Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSH}}$	Memory Select HOST Line	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSSD3–0}}$	Memory Select SDRAM Lines	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RD}}$	Memory Read	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{WRL}}$	Write Low Word	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{WRH}}$	Write High Word	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
ACK	Acknowledge for Data Hi to Low	1.5	0.5	3.6	2.0	1.15	2.0	SCLK
	Acknowledge for Data Low to High	1.5	0.5	4.2	2.0	1.15	2.0	SCLK
SDCKE	SDRAM Clock Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RAS}}$	Row Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CAS}}$	Column Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
LDQM	Low Word SDRAM Data Mask	—	—	4.0	1.0	1.15	2.0	SCLK
HDQM	High Word SDRAM Data Mask	—	—	4.0	1.0	1.15	2.0	SCLK
SDA10	SDRAM ADDR10	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{HBR}}$	Host Bus Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{HBG}}$	Host Bus Grant	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BOFF}}$	Back Off Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BRST}}$	Burst pin	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request pins	1.5	0.5	4.0	1.0	—	—	SCLK
$\overline{\text{BM}}$	Bus Master Debug aid only	—	—	4.0	1.0	—	—	SCLK
$\overline{\text{IORD}}$	I/O Read pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{IOWR}}$	I/O Write pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{IOEN}}$	I/O Enable pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CPA}}$	Core Priority Access Hi to Low	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
	Core Priority Access Low to Hi	1.5	0.5	23.5	2.0	1.15	2.0	SCLK
$\overline{\text{DPA}}$	DMA Priority Access Hi to Low	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
	DMA Priority Access Low to Hi	1.5	0.5	23.5	2.0	1.15	2.0	SCLK
$\overline{\text{BMS}}$	Boot Memory Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
FLAG3–0[2]	FLAG pins	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RST\_IN}}$[3,4]	Global Reset pin	1.5	0.5	—	—	—	—	SCLK
TMS	Test Mode Select (JTAG)	1.5	0.5	—	—	—	—	TCK
TDI	Test Data Input (JTAG)	1.5	0.5	—	—	—	—	TCK
TDO	Test Data Output (JTAG)	—	—	4.0	1.0	1.15	2.0	TCK
$\overline{\text{TRST}}$[3,4]	Test Reset (JTAG)	1.5	0.5	—	—	—	—	TCK

Table 22. AC Signal Specifications (all values in this table are in nanoseconds) (continued)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)	Output Hold (min)	Output Enable (min)[1]	Output Disable (max)[1]	Reference Clock
$\overline{\text{EMU}}$[5]	Emulation High to Low	—	—	3.6	2.0	1.15	2.0	TCK or SCLK
ID2–0[6]	Static pins – must be constant	—	—	—	—	—	—	—
CONTROLIMP1–0[6]	Static pins – must be constant	—	—	—	—	—	—	—
DS2–0[6]	Static pins – must be constant	—	—	—	—	—	—	—
SCLKRAT2–0[6]	Static pins – must be constant	—	—	—	—	—	—	—
ENEDREG[6]	Static pins – must be constant	—	—	—	—	—	—	—
STRAP SYS[7,8]	Strap pins	1.5	0.5	—	—	—	—	SCLK
JTAG SYS[9]	JTAG system pins	1.5	0.5	0.4	1.0	—	—	TCK

[1]The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.
[2]For input specifications on FLAG3–0 pins, see Table 17.
[3]These input pins are asynchronous and therefore do not need to be synchronized to a clock reference.
[4]For additional requirement details, see Reset and Booting on page 8.
[5]Reference clock depends on function.
[6]These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.
[7]STRAP pins include: $\overline{\text{BMS}}$, $\overline{\text{BM}}$, $\overline{\text{BUSLOCK}}$, TMR0E, $\overline{\text{L1BCMPO}}$, $\overline{\text{L2BCMPO}}$, and $\overline{\text{L3BCMPO}}$.
[8]Specifications applicable during reset only.
[9]JTAG system pins include: $\overline{\text{RST\_IN}}$, $\overline{\text{RST\_OUT}}$, $\overline{\text{POR\_IN}}$, $\overline{\text{IRQ3-0}}$, $\overline{\text{DMAR3-0}}$, $\overline{\text{HBR}}$, $\overline{\text{BOFF}}$, $\overline{\text{MS1-0}}$, $\overline{\text{MSH}}$, SDCKE, LDQM, HDQM, $\overline{\text{BMS}}$, $\overline{\text{IOWR}}$, $\overline{\text{IORD}}$, $\overline{\text{BM}}$, $\overline{\text{EMU}}$, SDA10, $\overline{\text{IOEN}}$, $\overline{\text{BUSLOCK}}$, TMR0E, DATA63-0, ADDR31-0, $\overline{\text{RD}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{BRST}}$, $\overline{\text{MSSD3-0}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{HBG}}$, $\overline{\text{BR7-0}}$, FLAG3-0, L0DATOP3-0, L0DATON3-0, L1DATOP3-0, L1DATON3-0, L2DATOP3-0, L2DATON3-0, L3DATOP3-0, L3DATON3-0, L0CLKOUTP, L0CLKOUTN, L1CLKOUTP, L1CLKOUTN, L2CLKOUTP, L2CLKOUTN, L3CLKOUTP, L3CLKOUTN, L0ACKI, L1ACKI, L2ACKI, L3ACKI, L0DATIP3-0, L0DATIN3-0, L1DATIP3-0, L1DATIN3-0, L2DATIP3-0, L2DATIN3-0, L3DATIP3-0, L3DATIN3-0, L0CLKINP, L0CLKINN, L1CLKINP, L1CLKINN, L2CLKINP, L2CLKINN, L3CLKINP, L3CLKINN, L0ACKO, L1ACKO, L2ACKO, L3ACKO, ACK, $\overline{\text{CPA}}$, $\overline{\text{DPA}}$, $\overline{\text{L0BCMPO}}$, $\overline{\text{L1BCMPO}}$, $\overline{\text{L2BCMPO}}$, $\overline{\text{L3BCMPO}}$, $\overline{\text{L0BCMPI}}$, $\overline{\text{L1BCMPI}}$, $\overline{\text{L2BCMPI}}$, $\overline{\text{L3BCMPI}}$, ID2-0, CTRL_IMPD1-0, SCLKRAT2-0, DS2-0, ENEDREG.

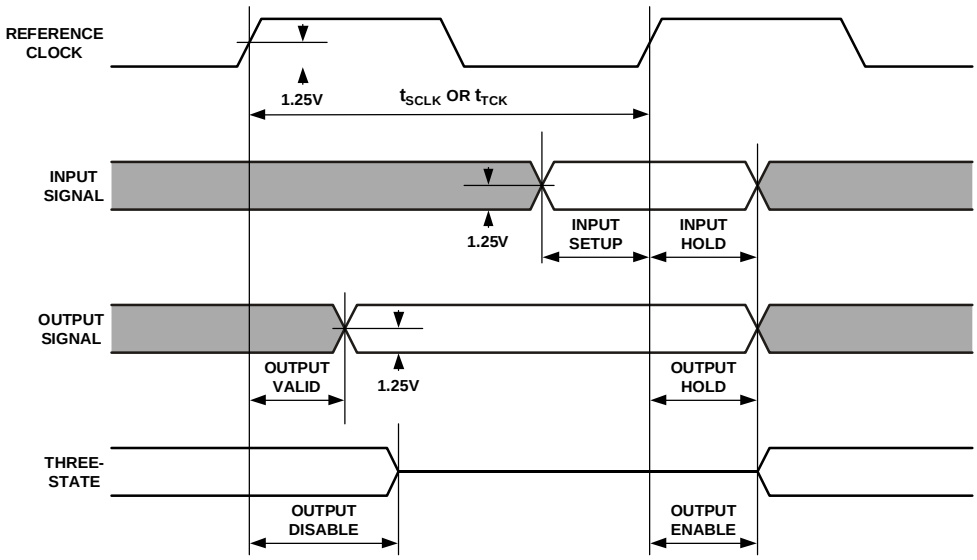


Figure 10. General AC Parameters Timing

Link Port Low-Voltage, Differential-Signal (LVDS) Electrical Characteristics and Timing

Table 23 and Table 24 with Figure 11 provide the electrical characteristics for the LVDS link ports.

The LVDS link port signal definitions represent all differential signals with a V_{OD} = 0 V level and use signal naming without N (negative) and P (positive) suffixes (see Figure 12).

Table 23. Link Port LVDS Transmit Electrical Characteristics

Parameter		Test Conditions	Min	Max	Units
V_{OH}	Output Voltage High, V_{O_P} or V_{O_N}	R_L = 100 Ω		1.58	V
V_{OL}	Output Voltage Low, V_{O_P} or V_{O_N}	R_L = 100 Ω	0.92		V
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100 Ω	150	450	mV
I_{OS}	Short-circuit Output Current	V_{O_P} or V_{O_N} = 0 V		+5/- 40	mA
		V_{OD} = 0 V		+/- 5	mA
V_{OCM}	Common Mode Output Voltage		1.13	1.38	V

Table 24. Link Port LVDS Receive Electrical Characteristics

Parameter		Test Conditions	Min	Max	Units
$\|V_{ID}\|$	Differential Input Voltage		100	600	mV
V_{ICM}	Common Mode Input Voltage		0.6	1.57	V

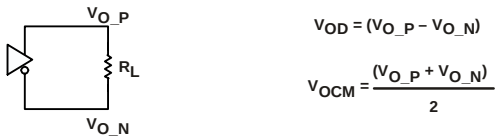


Figure 11. Link Ports—Transmit Electrical Characteristics

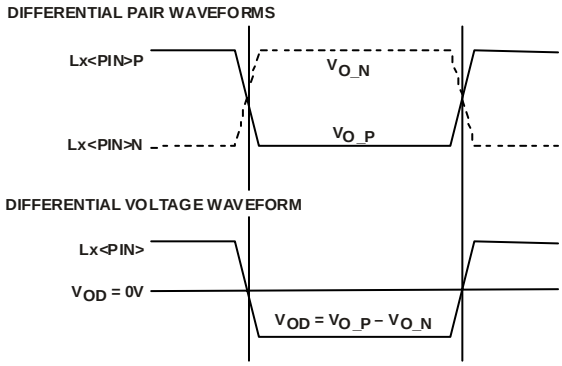


Figure 12. Link Ports—Signals Definition

Link Port—Data Out Timing

Table 25. Link Port—Data Out Timing

Parameter		Min	Max	Units
Outputs				
t_{REO}	Rising Edge (Figure 13)		200	ps
t_{FEO}	Falling Edge (Figure 13)		200	ps
t_{LCLKOP}	LxCLKOUT Period (Figure 14)	$0.9\times LCR\times t_{CCLK}$[1,2]	$1.1\times LCR\times t_{CCLK}$[1,2]	ns
t_{LCLKOH}	LxCLKOUT High (Figure 14	$0.4\times LCR\times t_{CCLK}$[1,2]	$0.6\times LCR\times t_{CCLK}$[1,2]	ns
t_{LCLKOL}	LxCLKOUT Low (Figure 14)	$0.4\times LCR\times t_{CCLK}$[1,2]	$0.6\times LCR\times t_{CCLK}$[1,2]	ns
t_{COJT}	LxCLKOUT Jitter (Figure 14)		–/+70	ps
t_{LDOS}	LxDATO Output Setup, LCR = 1 and LCR = 1.5 (Figure 15)	smaller of 2.5[3] or $0.25\times LCR\times t_{CCLK} - 0.15$[1,2,4]		ns
	LxDATO Output Setup, LCR = 2 and LCR = 4 (Figure 15)	smaller of 2.5[3] or $0.25\times LCR\times t_{CCLK} - 0.3$[1,2,4]		ns
t_{LDOH}	LxDATO Output Hold, LCR = 1 and LCR = 1.5 (Figure 15)	$0.25\times LCR\times t_{CCLK} - 0.15$[1,2,4]		ns
	LxDATO Output Hold, LCR = 2 and LCR = 4 (Figure 15)	$0.25\times LCR\times t_{CCLK} - 0.3$[1,2,4]		ns
t_{LACKID}	Delay from LxACKI rising edge to first transmission clock edge (Figure 16)		$14\times LCR\times t_{CCLK}$[1,2]	ns
t_{BCMPOV}	$\overline{\text{LxBCMPO}}$ Valid (Figure 16)		$2\times LCR\times t_{CCLK}$[1,2]	ns
t_{BCMPOH}	$\overline{\text{LxBCMPO}}$ Hold (Figure 17).	3×TSW - 0.5[1,2,5]		ns
Inputs				
t_{LACKIS}	LxACKI low setup to guarantee that the transmitter stops transmitting (Figure 17). LxACKI high setup to guarantee that the transmitter continues its transmission without any interruption (Figure 18).	$14\times LCR\times t_{CCLK}$[1,2]		ns
t_{LACKIH}	LxACKI high hold time (Figure 17).	0.5[1,2]		ns

[1] Timing is relative to the 0 differential voltage (V_{OD} = 0)
[2] LCR (Link port Clock Ratio) = 1, 1.5, 2 or 4. t_{CCLK} is the core period
[3] The 2.5 value for t_{LDOS} applies for LCLKOUT≤100 MHz.
[4] t_{LDOS} and t_{LDOH} values include LCLKOUT jitter.
[5] TSW is a short-word transmission period. For a 4-Bit Link it is $2\times LCR\times t_{CCLK}$ and for a 1-Bit Link is $8\times LCR\times t_{CCLK}$ ns

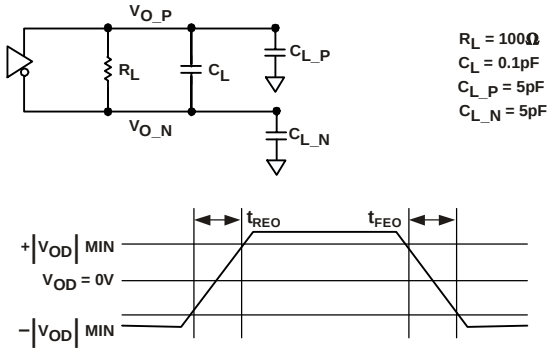


Figure 13. Link Ports—Differential Output Signals Transition Time

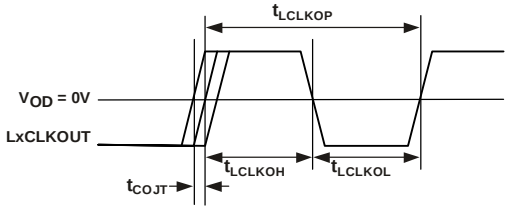


Figure 14. Link Ports—Output Clock

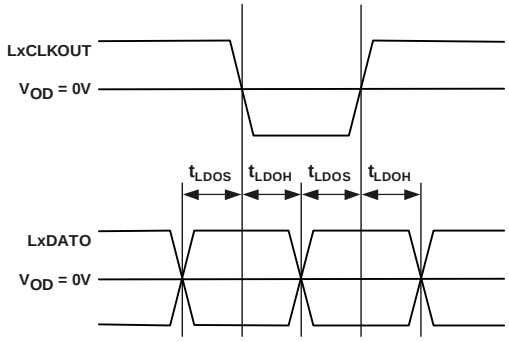


Figure 15. Link Ports—Data Output Setup and Hold[1]

[1] These parameters are valid for both clock edges

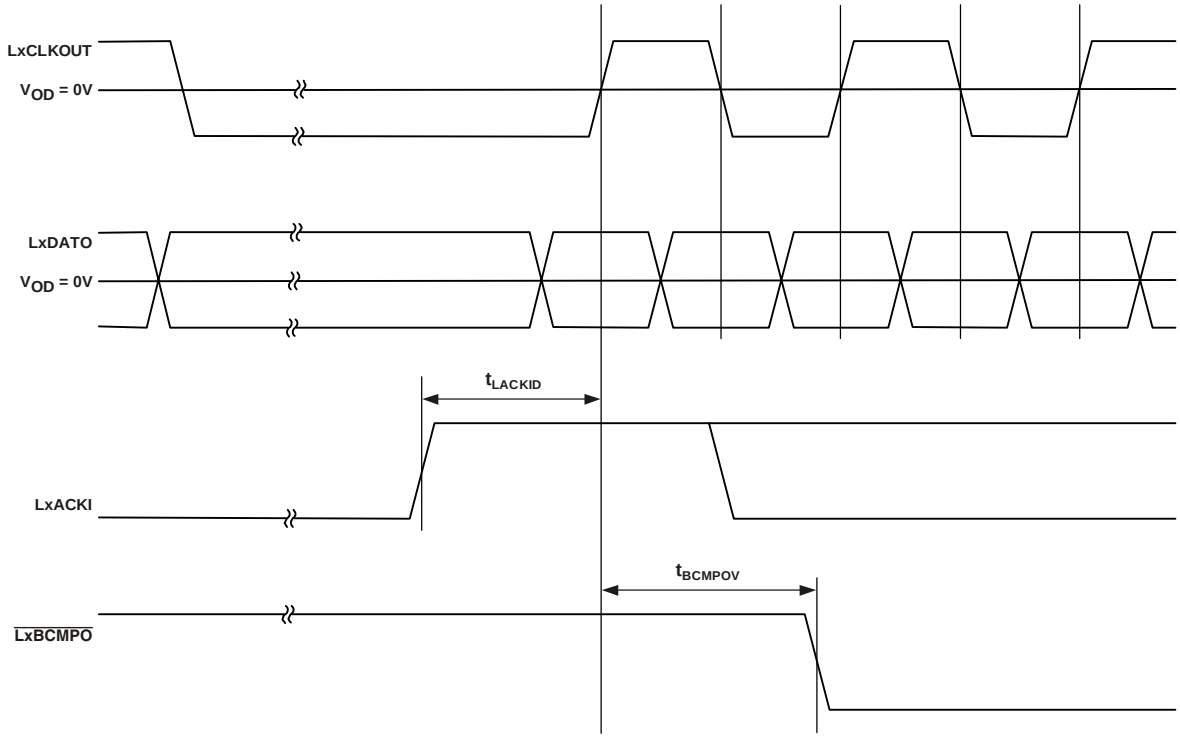


Figure 16. Link Ports—Transmission Start

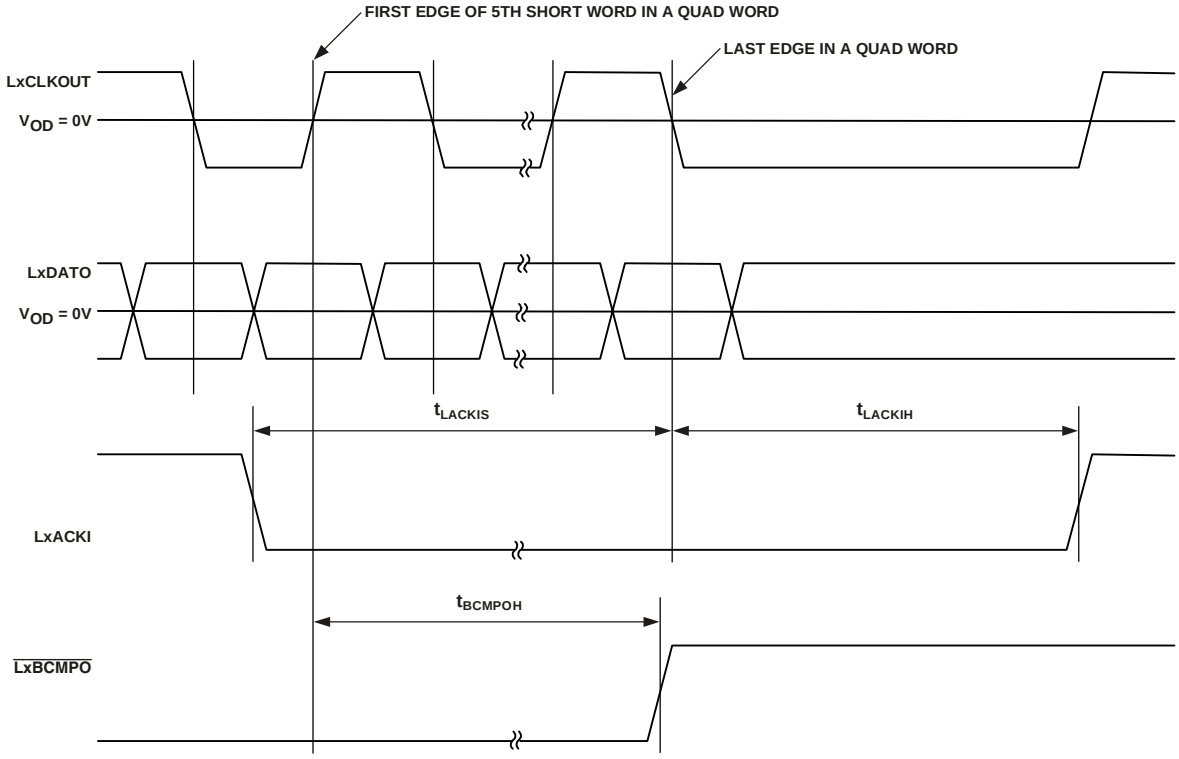


Figure 17. Link Ports—Transmission End and Stops

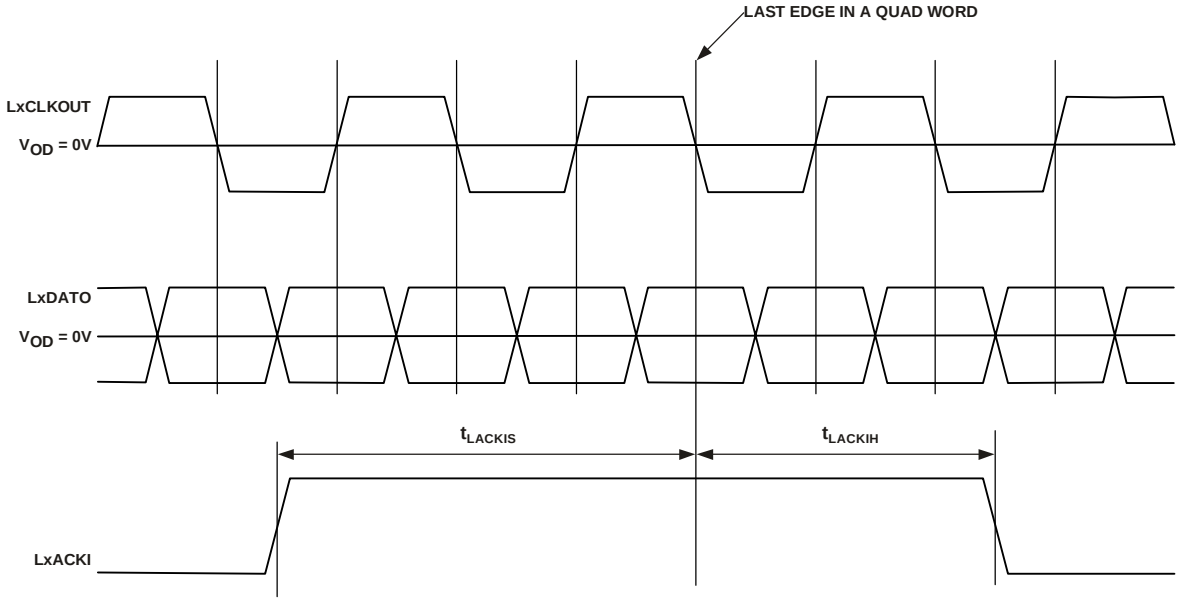


Figure 18. Link Ports—Back to Back Transmission

Link Port—Data In Timing

Table 26. Link Port—Data In Timing

Parameter		Min	Max	Units
Inputs				
t_{LCLKIP}	LxCLKIN Period (Figure 21)	$0.9 \times t_{CCLK}$[1]		ns
t_{REI}	Rising Edge (Figure 20)		400	ps
t_{FEI}	Falling Edge (Figure 20)		400	ps
t_{LDIS}	LxDATI Input Setup (Figure 21)	0.2[1]		ns
t_{LDIH}	LxDATI Input Hold (Figure 21)	0.2[1]		ns
t_{BCMPIS}	$\overline{\text{LxBCMPI}}$ Valid (Figure 19)	$2 \times LCR \times t_{CCLK}$[1,2]		ns
t_{BCMPIH}	$\overline{\text{LxBCMPI}}$ Hold (Figure 19)	$2 \times LCR \times t_{CCLK}$[1,2]		ns

[1] Timing is relative to the 0 differential voltage (V_{OD} = 0)
[2] LCR (Link port Clock Ratio) = 1, 1.5, 2 or 4. t_{CCLK} is the core period

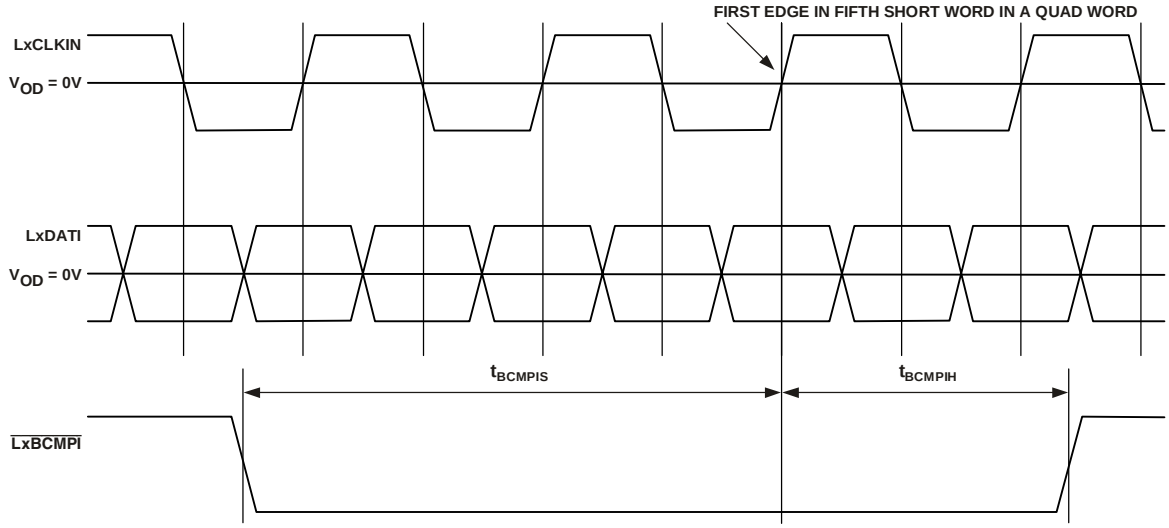


Figure 19. Link Ports—Last Received Quad Word

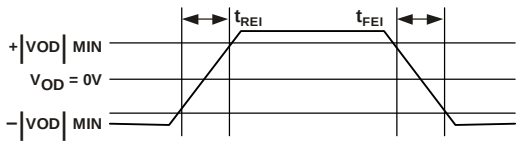


Figure 20. Link Ports—Differential Input Signals Transition Time

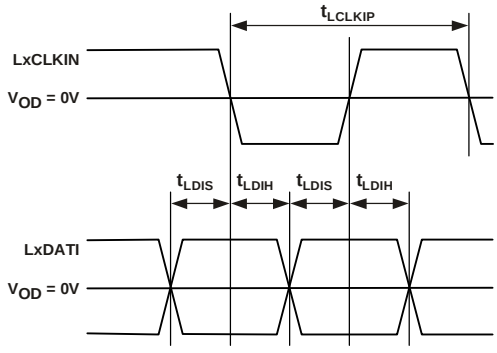


Figure 21. Link Ports—Data Input Setup and Hold[1]

[1] These parameters are valid for both clock edges

Output Drive Currents

Figure 22 through Figure 29 show typical I–V characteristics for the output drivers of the ADSP-TS201S processor. The curves in these diagrams represent the current drive capability of the output drivers as a function of output voltage over the range of drive strengths. For complete output driver characteristics, refer to the DSP's IBIS models, available on the Analog Devices website (www.analog.com).

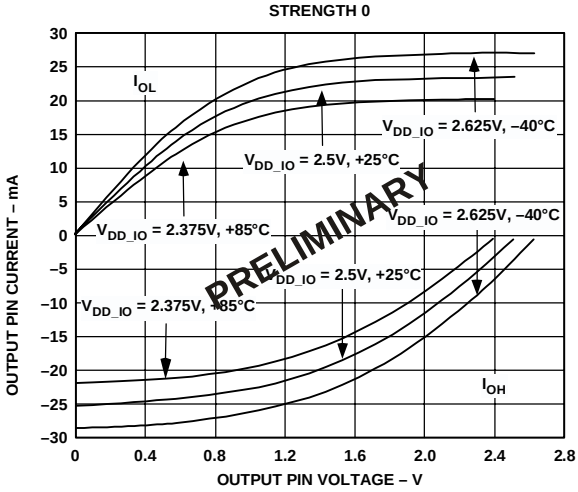


Figure 22. Typical Drive Currents at Strength 0

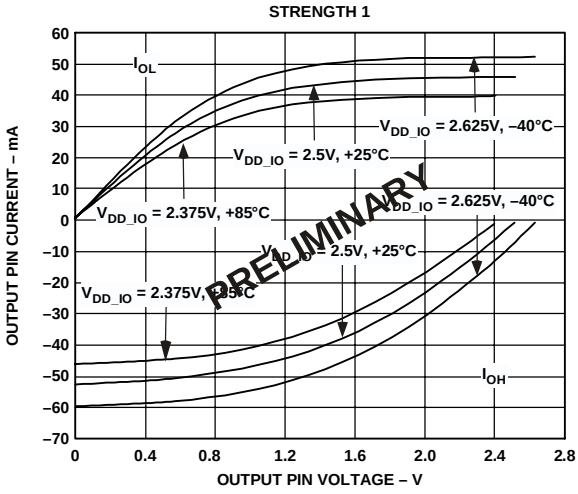


Figure 23. Typical Drive Currents at Strength 1

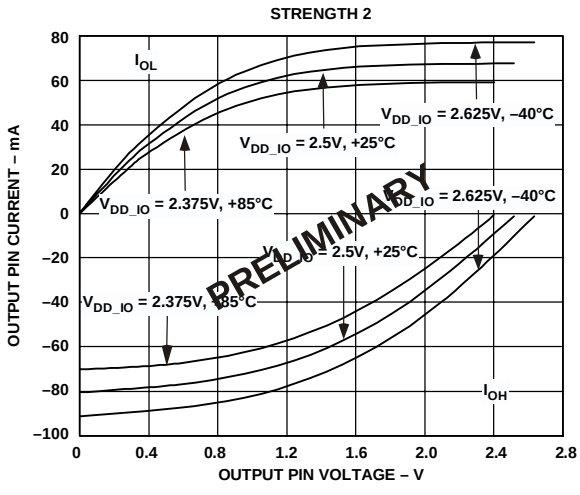


Figure 24. Typical Drive Currents at Strength 2

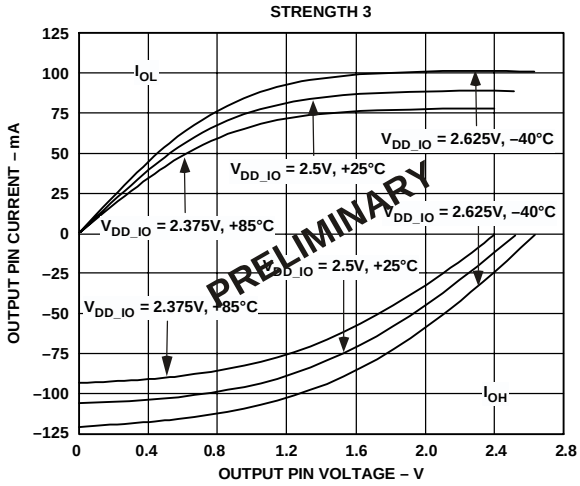


Figure 25. Typical Drive Currents at Strength 3

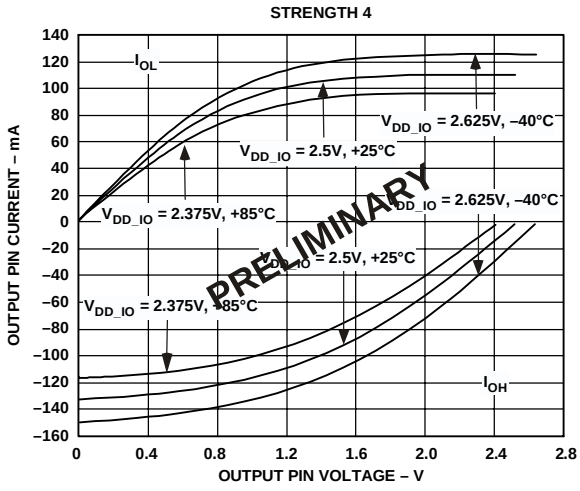


Figure 26. Typical Drive Currents at Strength 4

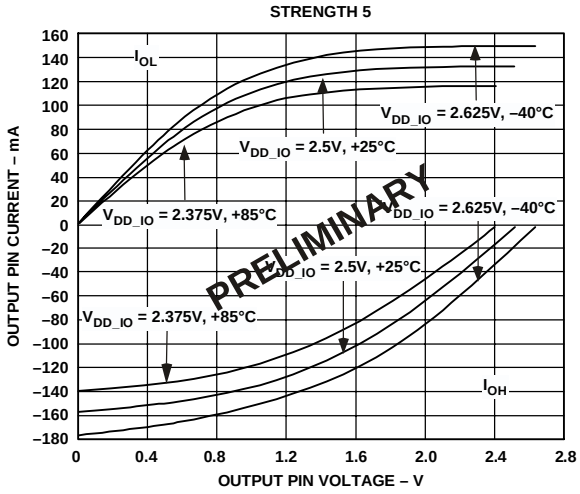


Figure 27. Typical Drive Currents at Strength 5

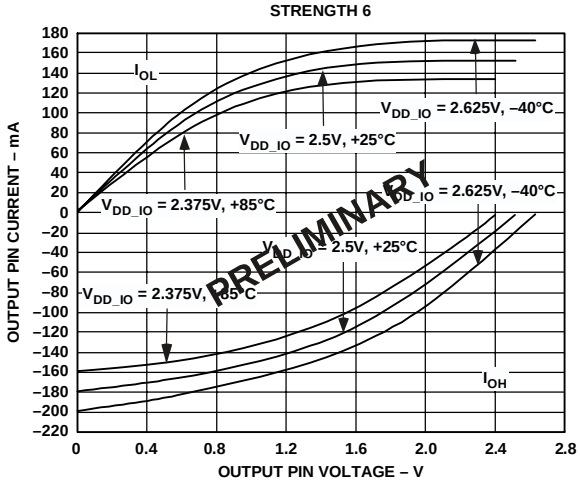


Figure 28. Typical Drive Currents at Strength 6

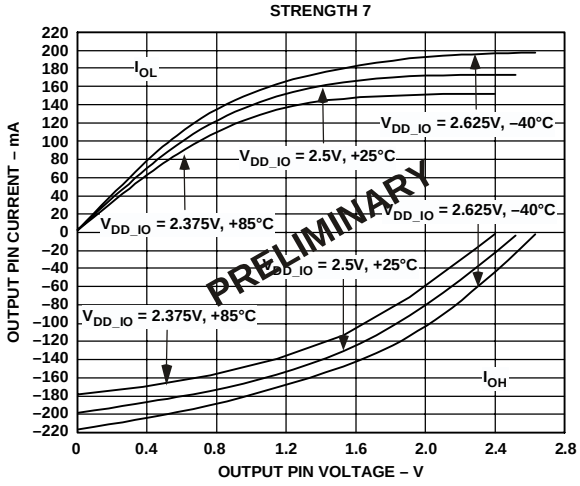


Figure 29. Typical Drive Currents at Strength 7

Test Conditions

The ac signal specifications (timing parameters) appear Table 22 on page 24. These include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 30.

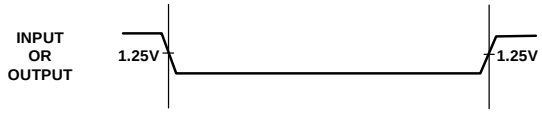


Figure 30. Voltage reference levels for AC measurements (except output enable/disable)

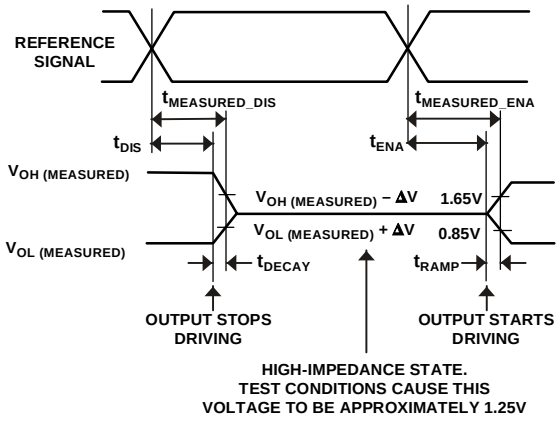


Figure 31. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED\_DIS}$ and t_{DECAY} as shown in Figure 31. The time $t_{MEASURED\_DIS}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.4 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The time for the voltage on the bus to ramp by ΔV is dependent on the capacitive load, C_L, and the drive current, I_D. This ramp time can be approximated by the following equation:

$$t_{RAMP} = (C_L \Delta V)/I_D$$

The output enable time t_{ENA} is the difference between $t_{MEASURED\_ENA}$ and t_{RAMP} as shown in Figure 31. The time $t_{MEASURED\_ENA}$ is the interval from when the reference signal switches to when the output voltage ramps ΔV from the measured three-stated output level. t_{RAMP} is calculated with test load C_L, drive current I_D, and with ΔV equal to 0.4 V.

Capacitive Loading

Output valid and hold are based on standard capacitive loads: 30 pF on all pins (see Figure 32). The delay and hold specifications given should be derated by a drive strength related factor for loads other than the nominal value of 30 pF. Figure 33 through Figure 40 show how output rise time varies with capacitance. Figure 41 graphically shows how output valid varies with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on page 32.) The graphs of Figure 33 through Figure 41 may not be linear outside the ranges shown.

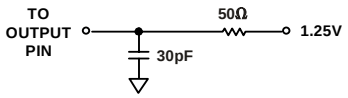


Figure 32. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

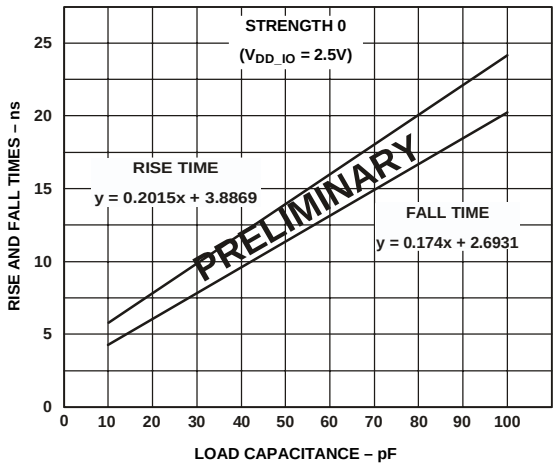


Figure 33. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 0

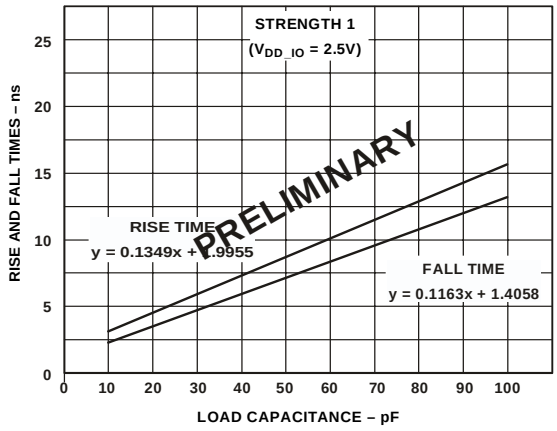


Figure 34. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 1

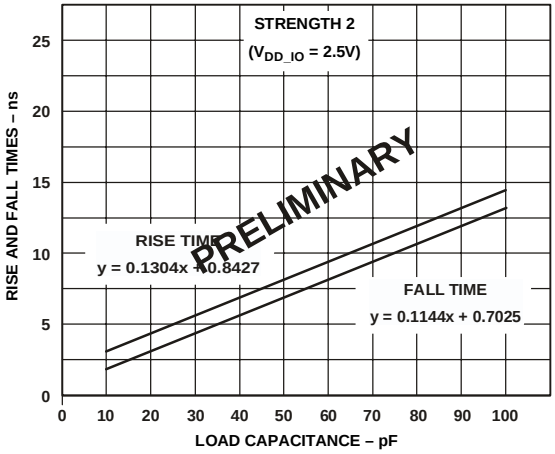


Figure 35. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 2

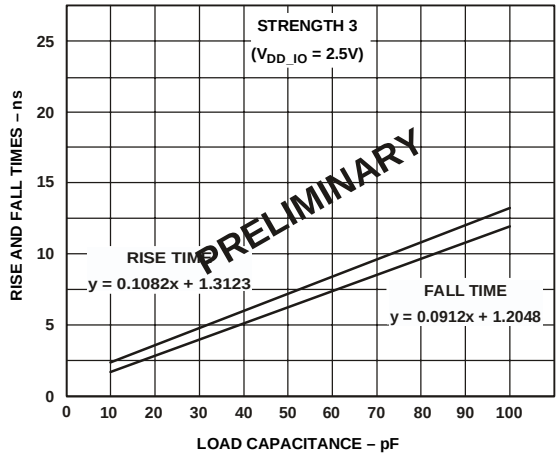


Figure 36. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 3

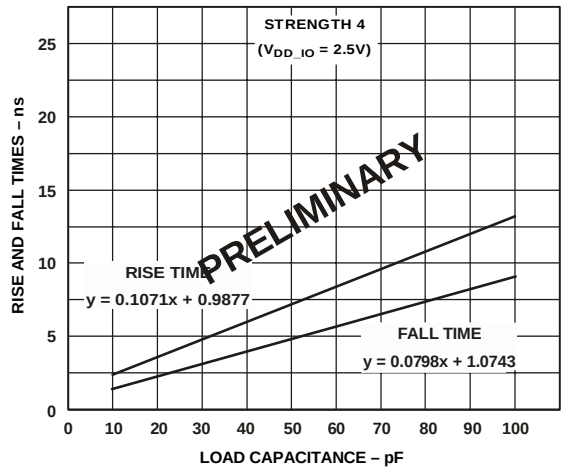


Figure 37. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 4

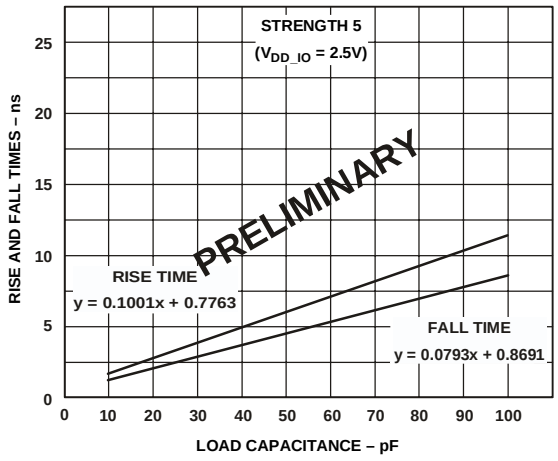


Figure 38. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 5

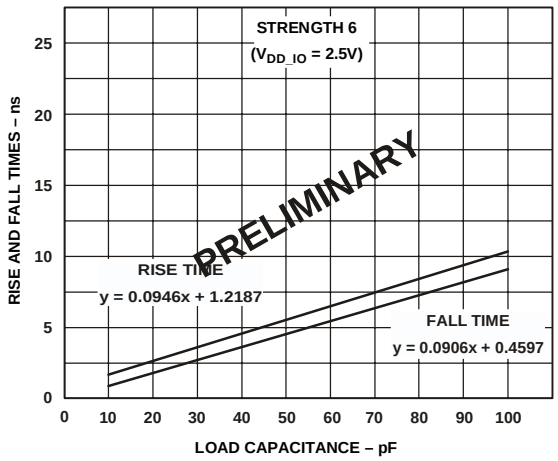


Figure 39. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 6

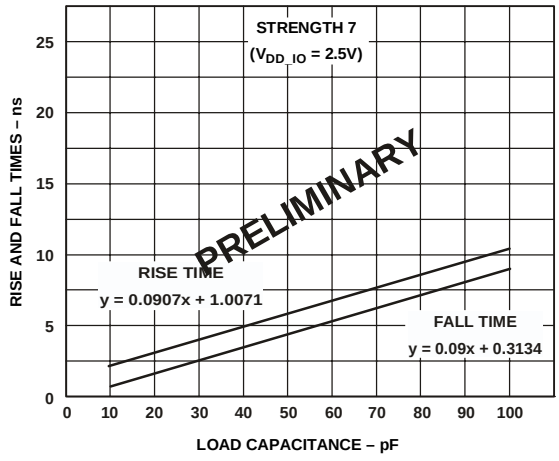


Figure 40. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 7

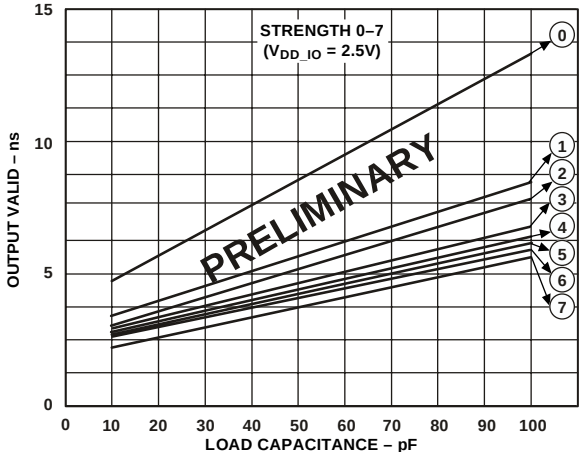


Figure 41. Typical Output Valid (V_{DD_IO} = 2.5 V) vs. Load Capacitance at Max Case Temperature and Strength 0–7[1]

[1] The line equations for the output valid versus load capacitance are:
Strength 0: y = 0.0956x + 3.5662
Strength 1: y = 0.0523x + 3.2144
Strength 2: y = 0.0433x + 3.1319
Strength 3: y = 0.0391x + 2.9675
Strength 4: y = 0.0393x + 2.7653
Strength 5: y = 0.0373x + 2.6515
Strength 6: y = 0.0379x + 2.1206
Strength 7: y = 0.0399x + 1.9080

Environmental Conditions

The ADSP-TS201S processor is rated for performance over the extended commercial temperature range, T_{CASE} = –40°C to 85°C.

Thermal Characteristics

The ADSP-TS201S processor is packaged in a 25 mm × 25 mm thermally enhanced Ball Grid Array (BGA_ED). The ADSP-TS201S processor is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used.

Table 27 shows the thermal characteristics of the 25 mm × 25 mm BGA_ED package.

Table 27. Thermal Characteristics for 25 mm × 25 mm Package

Parameter	Condition	Typical	Units
θ_{JA}	Airflow = 0 m/s	19.6	°C/W
	Airflow = 1 m/s	15.4	°C/W
	Airflow = 2 m/s	13.7	°C/W
θ_{JC}	–	0.7	°C/W
θ_{JB}	–	8.3	°C/W

576-BALL BGA_ED PIN CONFIGURATIONS

Table 28. 576-Ball (25 mm × 25 mm) BGA_ED Pin Assignments

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
A1	V_{SS}	B1	DATA53	C1	V_{SS}	D1	DATA55
A2	DATA51	B2	V_{SS}	C2	V_{SS}	D2	DATA56
A3	V_{SS}	B3	V_{SS}	C3	V_{SS}	D3	DATA54
A4	DATA49	B4	DATA50	C4	DATA52	D4	V_{SS}
A5	DATA43	B5	DATA44	C5	DATA47	D5	DATA48
A6	DATA41	B6	DATA42	C6	DATA45	D6	DATA46
A7	DATA37	B7	DATA38	C7	DATA39	D7	DATA40
A8	DATA33	B8	DATA34	C8	DATA35	D8	DATA36
A9	DATA29	B9	DATA30	C9	DATA31	D9	DATA32
A10	DATA25	B10	DATA26	C10	DATA27	D10	DATA28
A11	DATA23	B11	DATA24	C11	DATA21	D11	DATA22
A12	DATA19	B12	DATA20	C12	DATA17	D12	DATA18
A13	DATA15	B13	DATA16	C13	V_{SS}	D13	V_{SS}
A14	DATA11	B14	DATA12	C14	DATA13	D14	DATA14
A15	DATA9	B15	DATA10	C15	DATA7	D15	DATA8
A16	DATA5	B16	DATA6	C16	DATA3	D16	DATA4
A17	DATA1	B17	DATA2	C17	ACK	D17	DATA0
A18	$\overline{WRL}$	B18	$\overline{WRH}$	C18	$\overline{RD}$	D18	$\overline{BRST}$
A19	ADDR30	B19	ADDR31	C19	ADDR26	D19	ADDR27
A20	ADDR28	B20	ADDR29	C20	ADDR24	D20	ADDR25
A21	ADDR22	B21	ADDR23	C21	ADDR20	D21	V_{SS}
A22	V_{SS}	B22	V_{SS}	C22	V_{SS}	D22	ADDR19
A23	ADDR21	B23	V_{SS}	C23	V_{DD_IO}	D23	ADDR17
A24	V_{SS}	B24	ADDR18	C24	V_{DD_IO}	D24	ADDR16
E1	DATA61	F1	DATA63	G1	$\overline{MSSD1}$	H1	V_{SS}
E2	DATA62	F2	$\overline{MS1}$	G2	V_{SS}	H2	$\overline{MSH}$
E3	DATA57	F3	DATA59	G3	$\overline{MS0}$	H3	$\overline{MSSD3}$
E4	DATA58	F4	DATA60	G4	$\overline{BMS}$	H4	SCLKRAT0
E5	V_{SS}	F5	V_{DD_IO}	G5	V_{SS}	H5	V_{DD_IO}
E6	V_{DD_IO}	F6	V_{DD}	G6	V_{DD}	H6	V_{DD}
E7	V_{SS}	F7	V_{DD}	G7	V_{DD}	H7	V_{DD}
E8	V_{DD_IO}	F8	V_{DD}	G8	V_{DD}	H8	V_{SS}
E9	V_{SS}	F9	V_{DD}	G9	V_{DD}	H9	V_{SS}
E10	V_{DD_IO}	F10	V_{DD}	G10	V_{DD}	H10	V_{SS}
E11	V_{DD_IO}	F11	V_{DD_DRAM}	G11	V_{DD_DRAM}	H11	V_{SS}
E12	V_{DD_IO}	F12	V_{DD_DRAM}	G12	V_{DD_DRAM}	H12	V_{SS}
E13	V_{DD_IO}	F13	V_{DD}	G13	V_{DD}	H13	V_{SS}
E14	V_{DD_IO}	F14	V_{DD}	G14	V_{DD}	H14	V_{SS}
E15	V_{DD_IO}	F15	V_{DD_DRAM}	G15	V_{DD_DRAM}	H15	V_{SS}
E16	V_{SS}	F16	V_{DD_DRAM}	G16	V_{DD_DRAM}	H16	V_{SS}
E17	V_{DD_IO}	F17	V_{DD}	G17	V_{DD}	H17	V_{SS}
E18	V_{SS}	F18	V_{DD}	G18	V_{DD}	H18	V_{DD}
E19	V_{DD_IO}	F19	V_{DD}	G19	V_{DD}	H19	V_{DD}
E20	V_{SS}	F20	V_{DD_IO}	G20	V_{DD_IO}	H20	V_{DD_IO}
E21	ADDR15	F21	ADDR13	G21	ADDR7	H21	ADDR3
E22	ADDR14	F22	ADDR12	G22	ADDR6	H22	ADDR2
E23	ADDR11	F23	ADDR9	G23	ADDR5	H23	ADDR1
E24	ADDR10	F24	ADDR8	G24	ADDR4	H24	ADDR0

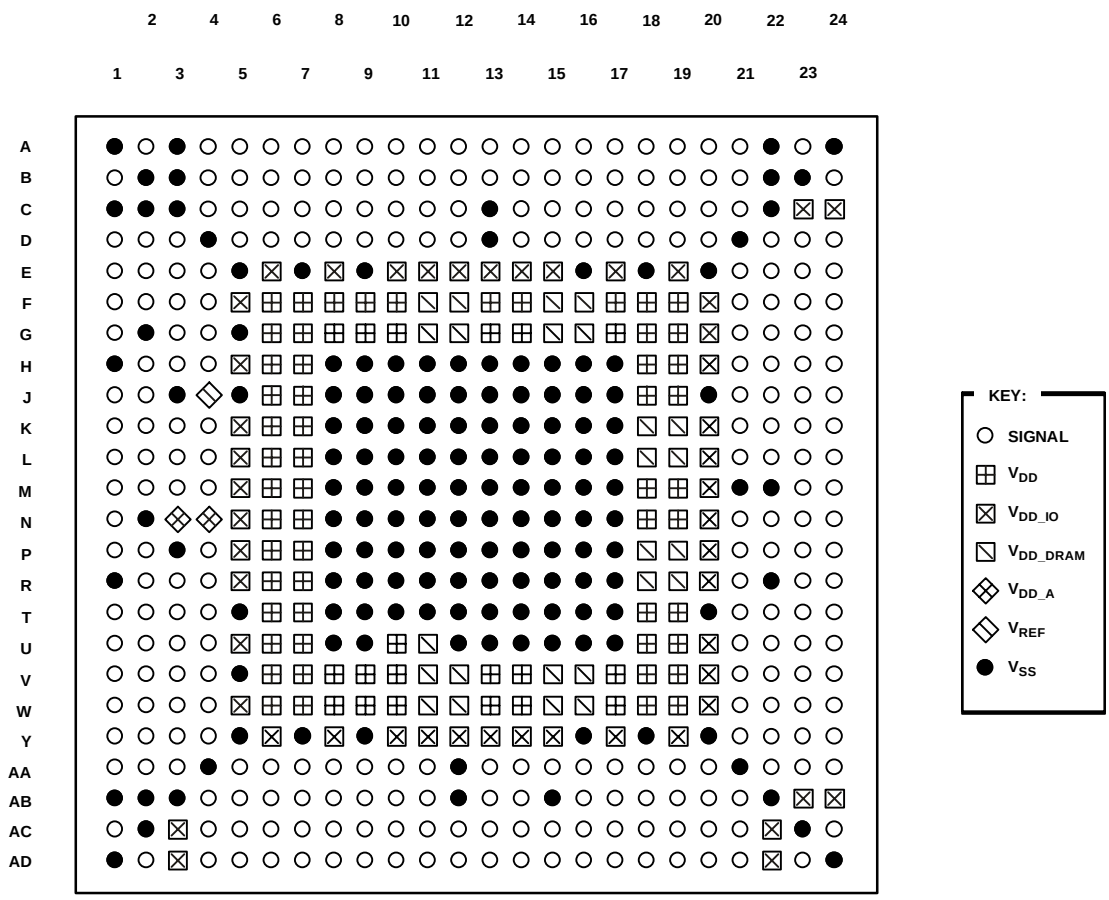
Table 28. 576-Ball (25 mm × 25 mm) BGA_ED Pin Assignments (continued)

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
J1	$\overline{RAS}$	K1	SDA10	L1	$\overline{SDWE}$	M1	$\overline{BR3}$
J2	$\overline{CAS}$	K2	SDCKE	L2	$\overline{BR0}$	M2	SCLKRAT1
J3	V_{SS}	K3	LDQM	L3	$\overline{BR1}$	M3	$\overline{BR5}$
J4	V_{REF}	K4	HDQM	L4	$\overline{BR2}$	M4	$\overline{BR6}$
J5	V_{SS}	K5	V_{DD_IO}	L5	V_{DD_IO}	M5	V_{DD_IO}
J6	V_{DD}	K6	V_{DD}	L6	V_{DD}	M6	V_{DD}
J7	V_{DD}	K7	V_{DD}	L7	V_{DD}	M7	V_{DD}
J8	V_{SS}	K8	V_{SS}	L8	V_{SS}	M8	V_{SS}
J9	V_{SS}	K9	V_{SS}	L9	V_{SS}	M9	V_{SS}
J10	V_{SS}	K10	V_{SS}	L10	V_{SS}	M10	V_{SS}
J11	V_{SS}	K11	V_{SS}	L11	V_{SS}	M11	V_{SS}
J12	V_{SS}	K12	V_{SS}	L12	V_{SS}	M12	V_{SS}
J13	V_{SS}	K13	V_{SS}	L13	V_{SS}	M13	V_{SS}
J14	V_{SS}	K14	V_{SS}	L14	V_{SS}	M14	V_{SS}
J15	V_{SS}	K15	V_{SS}	L15	V_{SS}	M15	V_{SS}
J16	V_{SS}	K16	V_{SS}	L16	V_{SS}	M16	V_{SS}
J17	V_{SS}	K17	V_{SS}	L17	V_{SS}	M17	V_{SS}
J18	V_{DD}	K18	V_{DD_DRAM}	L18	V_{DD_DRAM}	M18	V_{DD}
J19	V_{DD}	K19	V_{DD_DRAM}	L19	V_{DD_DRAM}	M19	V_{DD}
J20	V_{SS}	K20	V_{DD_IO}	L20	V_{DD_IO}	M20	V_{DD_IO}
J21	L0ACKO	K21	L0DATI1_N	L21	L0DATI3_N	M21	V_{SS}
J22	$\overline{L0BCMPI}$	K22	L0DATI1_P	L22	L0DATI3_P	M22	V_{SS}
J23	L0DATI0_N	K23	L0CLKINN	L23	L0DATI2_N	M23	L0DATO3_N
J24	L0DATI0_P	K24	L0CLKINP	L24	L0DATI2_P	M24	L0DATO3_P
N1	ID0	P1	SCLK	R1	V_{SS}	T1	$\overline{RST\_IN}$
N2	V_{SS}	P2	SCLK_VREF	R2	SCLK	T2	SCLKRAT2
N3	V_{DD_A}	P3	V_{SS}	R3	SCLK_VREF	T3	$\overline{BR4}$
N4	V_{DD_A}	P4	$\overline{BM}$	R4	$\overline{BR7}$	T4	DS0
N5	V_{DD_IO}	P5	V_{DD_IO}	R5	V_{DD_IO}	T5	V_{SS}
N6	V_{DD}	P6	V_{DD}	R6	V_{DD}	T6	V_{DD}
N7	V_{DD}	P7	V_{DD}	R7	V_{DD}	T7	V_{DD}
N8	V_{SS}	P8	V_{SS}	R8	V_{SS}	T8	V_{SS}
N9	V_{SS}	P9	V_{SS}	R9	V_{SS}	T9	V_{SS}
N10	V_{SS}	P10	V_{SS}	R10	V_{SS}	T10	V_{SS}
N11	V_{SS}	P11	V_{SS}	R11	V_{SS}	T11	V_{SS}
N12	V_{SS}	P12	V_{SS}	R12	V_{SS}	T12	V_{SS}
N13	V_{SS}	P13	V_{SS}	R13	V_{SS}	T13	V_{SS}
N14	V_{SS}	P14	V_{SS}	R14	V_{SS}	T14	V_{SS}
N15	V_{SS}	P15	V_{SS}	R15	V_{SS}	T15	V_{SS}
N16	V_{SS}	P16	V_{SS}	R16	V_{SS}	T16	V_{SS}
N17	V_{SS}	P17	V_{SS}	R17	V_{SS}	T17	V_{SS}
N18	V_{DD}	P18	V_{DD_DRAM}	R18	V_{DD_DRAM}	T18	V_{DD}
N19	V_{DD}	P19	V_{DD_DRAM}	R19	V_{DD_DRAM}	T19	V_{DD}
N20	V_{DD_IO}	P20	V_{DD_IO}	R20	V_{DD_IO}	T20	V_{SS}
N21	L0DATO2_N	P21	L0DATO1_N	R21	NC	T21	L1DATI0_N
N22	L0DATO2_P	P22	L0DATO1_P	R22	V_{SS}	T22	L1DATI0_P
N23	L0CLKON	P23	L0DATO0_N	R23	$\overline{L0BCMPO}$	T23	L1ACKO
N24	L0CLKOP	P24	L0DATO0_P	R24	L0ACKI	T24	$\overline{L1BCMPI}$

Table 28. 576-Ball (25 mm × 25 mm) BGA_ED Pin Assignments (continued)

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
U1	$\overline{\text{MSSD0}}$	V1	$\overline{\text{MSSD2}}$	W1	CONTROLIMP0	Y1	$\overline{\text{EMU}}$
U2	$\overline{\text{RST\_OUT}}$	V2	DS2	W2	ENEDREG	Y2	TCK
U3	ID2	V3	$\overline{\text{POR\_IN}}$	W3	TDI	Y3	TMR0E
U4	DS1	V4	CONTROLIMP1	W4	TDO	Y4	FLAG3
U5	V_{DD_IO}	V5	V_{SS}	W5	V_{DD_IO}	Y5	V_{SS}
U6	V_{DD}	V6	V_{DD}	W6	V_{DD}	Y6	V_{DD_IO}
U7	V_{DD}	V7	V_{DD}	W7	V_{DD}	Y7	V_{SS}
U8	V_{SS}	V8	V_{DD}	W8	V_{DD}	Y8	V_{DD_IO}
U9	V_{SS}	V9	V_{DD}	W9	V_{DD}	Y9	V_{SS}
U10	V_{DD}	V10	V_{DD}	W10	V_{DD}	Y10	V_{DD_IO}
U11	V_{DD_DRAM}	V11	V_{DD_DRAM}	W11	V_{DD_DRAM}	Y11	V_{DD_IO}
U12	V_{SS}	V12	V_{DD_DRAM}	W12	V_{DD_DRAM}	Y12	V_{DD_IO}
U13	V_{SS}	V13	V_{DD}	W13	V_{DD}	Y13	V_{DD_IO}
U14	V_{SS}	V14	V_{DD}	W14	V_{DD}	Y14	V_{DD_IO}
U15	V_{SS}	V15	V_{DD_DRAM}	W15	V_{DD_DRAM}	Y15	V_{DD_IO}
U16	V_{SS}	V16	V_{DD_DRAM}	W16	V_{DD_DRAM}	Y16	V_{SS}
U17	V_{SS}	V17	V_{DD}	W17	V_{DD}	Y17	V_{DD_IO}
U18	V_{DD}	V18	V_{DD}	W18	V_{DD}	Y18	V_{SS}
U19	V_{DD}	V19	V_{DD}	W19	V_{DD}	Y19	V_{DD_IO}
U20	V_{DD_IO}	V20	V_{DD_IO}	W20	V_{DD_IO}	Y20	V_{SS}
U21	L1CLKINN	V21	L1DATI3_N	W21	L1CLKON	Y21	L1DATO1_N
U22	L1CLKINP	V22	L1DATI3_P	W22	L1CLKOP	Y22	L1DATO1_P
U23	L1DATI1_N	V23	L1DATI2_N	W23	L1DATO3_N	Y23	L1DATO2_N
U24	L1DATI1_P	V24	L1DATI2_P	W24	L1DATO3_P	Y24	L1DATO2_P
AA1	FLAG2	AB1	V_{SS}	AC1	FLAG0	AD1	V_{SS}
AA2	FLAG1	AB2	V_{SS}	AC2	V_{SS}	AD2	ID1
AA3	$\overline{\text{IRQ3}}$	AB3	V_{SS}	AC3	V_{DD_IO}	AD3	V_{DD_IO}
AA4	V_{SS}	AB4	NC	AC4	TMS	AD4	$\overline{\text{TRST}}$
AA5	$\overline{\text{IRQ0}}$	AB5	$\overline{\text{IRQ2}}$	AC5	$\overline{\text{IOWR}}$	AD5	$\overline{\text{IORD}}$
AA6	$\overline{\text{IOEN}}$	AB6	$\overline{\text{IRQ1}}$	AC6	$\overline{\text{DMAR2}}$	AD6	$\overline{\text{DMAR3}}$
AA7	$\overline{\text{DMAR0}}$	AB7	$\overline{\text{DMAR1}}$	AC7	$\overline{\text{CPA}}$	AD7	$\overline{\text{DPA}}$
AA8	$\overline{\text{HBR}}$	AB8	$\overline{\text{HBG}}$	AC8	$\overline{\text{BOFF}}$	AD8	$\overline{\text{BUSLOCK}}$
AA9	$\overline{\text{L3BCMPO}}$	AB9	L3ACKI	AC9	L3DATO0_N	AD9	L3DATO0_P
AA10	L3DATO1_N	AB10	L3DATO1_P	AC10	L3CLKON	AD10	L3CLKOP
AA11	L3DATO3_N	AB11	L3DATO3_P	AC11	L3DATO2_N	AD11	L3DATO2_P
AA12	V_{SS}	AB12	V_{SS}	AC12	L3DATI3_N	AD12	L3DATI3_P
AA13	L3DATI2_N	AB13	L3DATI2_P	AC13	L3CLKINN	AD13	L3CLKINP
AA14	L3DATI1_N	AB14	L3DATI1_P	AC14	L3DATI0_N	AD14	L3DATI0_P
AA15	NC	AB15	V_{SS}	AC15	$\overline{\text{L3ACKO}}$	AD15	$\overline{\text{L3BCMPI}}$
AA16	L2DATO0_N	AB16	L2DATO0_P	AC16	$\overline{\text{L2BCMPO}}$	AD16	L2ACKI
AA17	L2CLKON	AB17	L2CLKOP	AC17	L2DATO1_N	AD17	L2DATO1_P
AA18	L2DATO3_N	AB18	L2DATO3_P	AC18	L2DATO2_N	AD18	L2DATO2_P
AA19	L2CLKINN	AB19	L2CLKINP	AC19	L2DATI3_N	AD19	L2DATI3_P
AA20	L2DATI1_N	AB20	L2DATI1_P	AC20	L2DATI2_N	AD20	L2DATI2_P
AA21	V_{SS}	AB21	L2ACKO	AC21	L2DATI0_N	AD21	L2DATI0_P
AA22	$\overline{\text{L1BCMPO}}$	AB22	V_{SS}	AC22	V_{DD_IO}	AD22	V_{DD_IO}
AA23	L1DATO0_N	AB23	V_{DD_IO}	AC23	V_{SS}	AD23	$\overline{\text{L2BCMPI}}$
AA24	L1DATO0_P	AB24	V_{DD_IO}	AC24	L1ACKI	AD24	V_{SS}

576-BALL BGA_ED PIN CONFIGURATIONS[1] (TOP VIEW, SUMMARY)



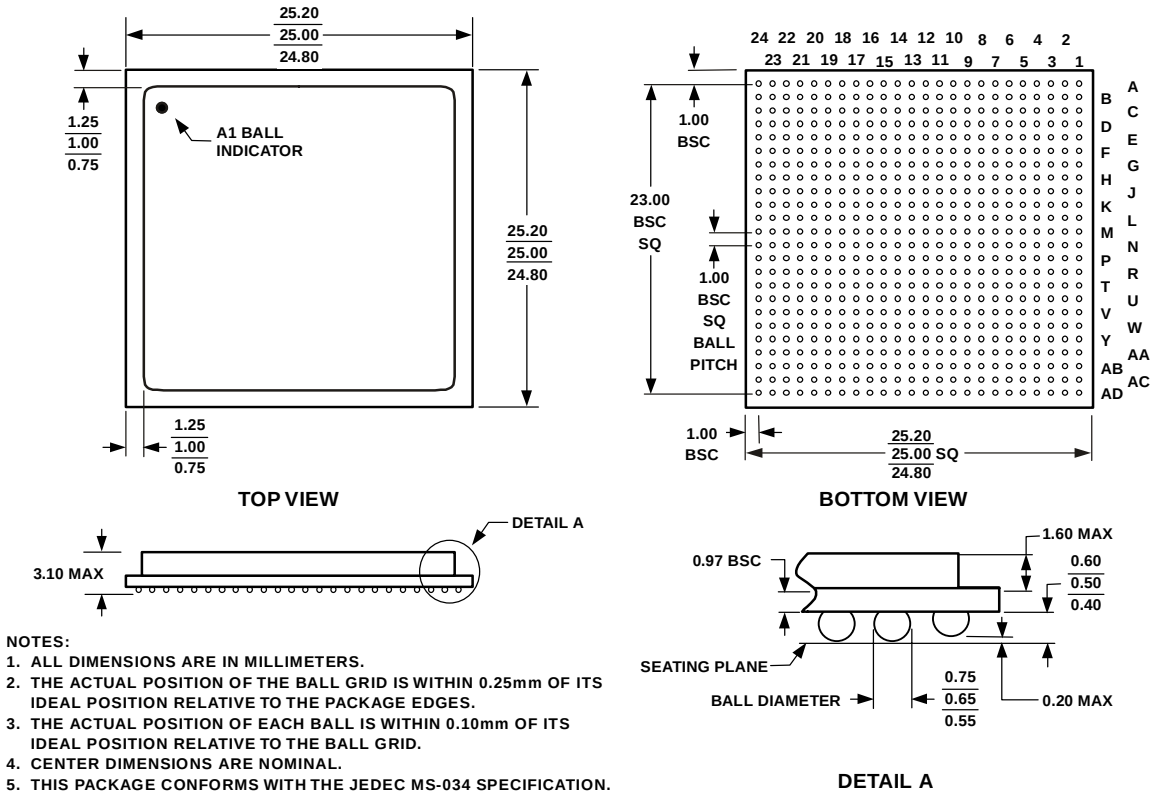
TOP VIEW

[1]For a more detailed pin summary diagram, see the *EE-179: ADSP-TS201S System Design Guidelines* on the Analog Devices website (www.analog.com)

OUTLINE DIMENSIONS

The ADSP-TS201S processor is available in a 25 mm × 25 mm, 576-ball metric thermally enhanced Ball Grid Array (BGA_ED) package with 24 rows of balls (BP-576).

576-BALL BGA_ED (BP-576)



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. THE ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.25mm OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
3. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.10mm OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
4. CENTER DIMENSIONS ARE NOMINAL.
5. THIS PACKAGE CONFORMS WITH THE JEDEC MS-034 SPECIFICATION.

ORDERING GUIDE

Table 29.

Part Number[1,2,3,4]	Case Temperature Range	Instruction Rate[5]	On-chip DRAM	Operating Voltage	Package
ADSP-TS201SABP-ENG	–40°C to 85°C	500 MHz	24Mbit	1.0 V_{DD} 2.5 V_{DD_IO} 1.5 V_{DD_DRAM}	(BP-576)[6]

[1] S indicates 1.0/2.5 V supplies.
[2] A indicates –40°C to 85°C temperature.
[3] BP indicated thermally enhanced Ball Grid Array (BGA_ED) package.
[4] -ENG indicates engineering grade product.
[5] The instruction rate is the same as the internal DSP clock (CCLK) rate.
[6] The BP-576 package measures 25mm × 25mm.