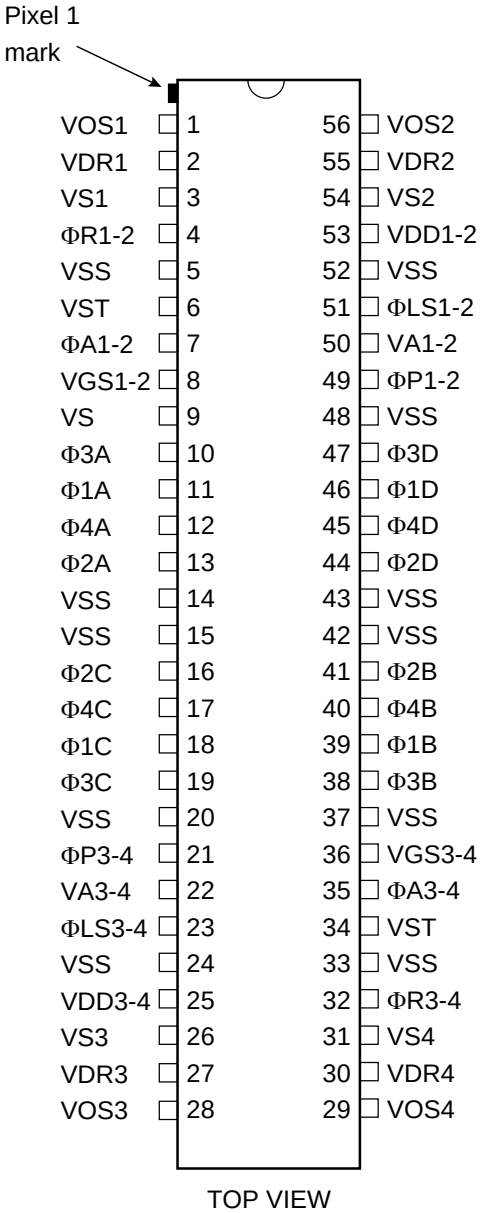
Features

- **6.5 µm x 6.5 µm Photodiode Pixel, at 6.5 µm Pitch**
- **2 x 2 Outputs**
- **High Output Data Rate: 4 x 5 MHz**
- **High Dynamic Range: 10000: 1**
- **Antiblooming and Exposure Time Control**
- **Very Low Lag**
- **56 lead 0.6" DIL Package**

Description

Atmel's TH7834C is a linear sensor based on charge-coupled device (CCD) technology. It can be used in a wide range of applications thanks to operating mode flexibility, very high definition and high dynamic range (document scanning, digital photography, Art, Industrial and Scientific Applications).



TOP VIEW

Very High-resolution Linear CCD Image Sensor (12000 Pixels)

TH7834C

Rev. 1997A–IMAGE–05/02

Pin Description

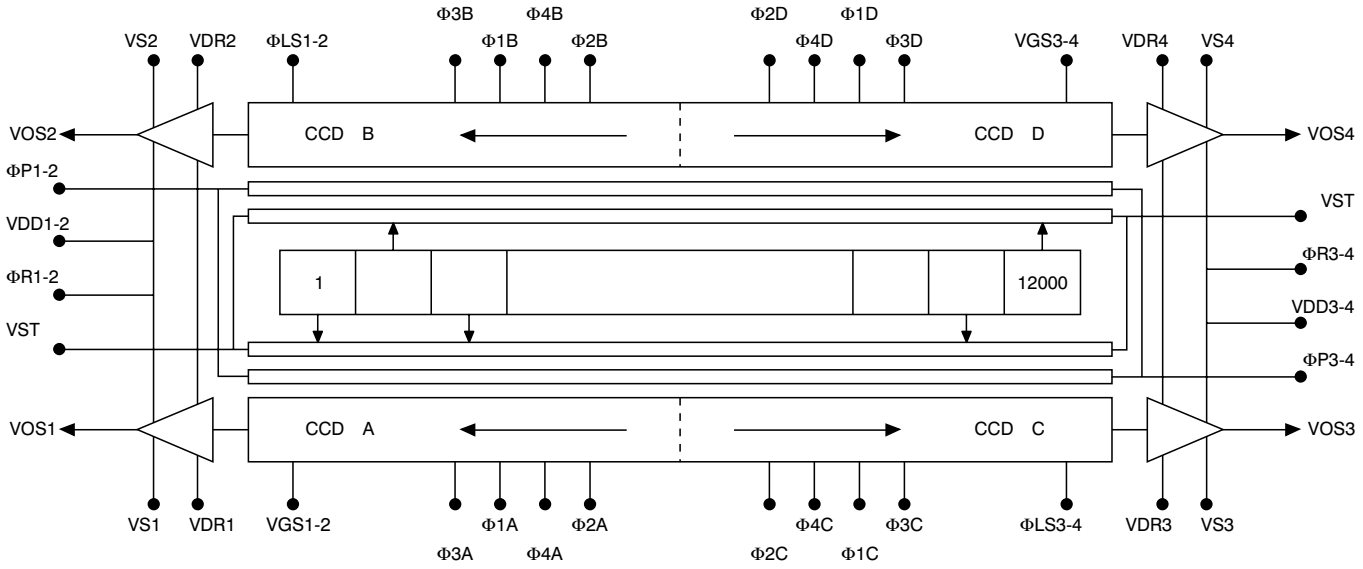
Pin Number	Symbol	Designation
1	V_{OS1}	Output 1 (Odd Pixels)
2	V_{DR1}	Reset DC Bias (Output 1)
3	V_{S1}	Amplifier Source Bias (Output 1)
4	Φ_{R1-2}	Reset Clock (Outputs 1 and 2)
5, 9, 14, 15, 20, 24, 33, 37, 42, 43, 48, 52	V_{SS}	Substrate Bias (Ground)
6, 34	VST	Pixel Storage Gate DC Bias
7	Φ_{A1-2}	Antiblooming and/or Exposure Time Control
8	V_{GS1-2}	Output Gate DC Bias
10	Φ_{3A}	Register Main Transport Clock
11	Φ_{1A}	Register Main Transport Clock
12	Φ_{4A}	Register Main Transport Clock
13	Φ_{2A}	Register Main Transport Clock
16	Φ_{2C}	Register Main Transport Clock
17	Φ_{4C}	Register Main Transport Clock
18	Φ_{1C}	Register Main Transport Clock
19	Φ_{3C}	Register Main Transport Clock
21	Φ_{P3-4}	Transfer Clock
22	VA_{3-4}	Antiblooming Diode Bias
23	Φ_{LS3-4}	Register End Transport Clock
25	V_{DD3-4}	Amplifier Drain Supplies (Outputs 3, 4)
26	V_{S3}	Amplifier Source Bias (Output 3)
27	V_{DR3}	Reset DC Bias (Output 3)
28	V_{OS3}	Output 3 (Odd Pixels)
29	V_{OS4}	Output 4 (Even Pixels)
30	V_{DR4}	Reset DC Bias (Output 4)
31	V_{S4}	Amplifier Source Bias (Output 4)
32	Φ_{R3-4}	Reset Clock (Outputs 3 and 4)
35	Φ_{A3-4}	Antiblooming and/or Exposure Time Control
36	V_{GS3-4}	Output Gate DC Bias
38	Φ_{3D}	Register Main Transport Clock
39	Φ_{1D}	Register Main Transport Clock
40	Φ_{4D}	Register Main Transport Clock
41	Φ_{2D}	Register Main Transport Clock
44	Φ_{2B}	Register Main Transport Clock
45	Φ_{4B}	Register Main Transport Clock

Pin Description (Continued)

Pin Number	Symbol	Designation
46	Φ_{1B}	Register Main Transport Clock
47	Φ_{3B}	Register Main Transport Clock
49	Φ_{P1-2}	Transfer Clock
50	VA_{1-2}	Antiblooming Diode Bias
51	Φ_{LS1-2}	Register End Transport Clock
53	V_{DD1-2}	Amplifier Drain Supplies (Outputs 1, 2)
54	V_{S2}	Amplifier Source Bias (Output 2)
55	V_{DR2}	Reset DC Bias (Output 2)
56	V_{OS2}	Output 2 (Even Pixels)

Notes: 1. Pins Φ_{A1-2}, V_{GS1-2}, Φ_{P1-2}, VA_{1-2}, Φ_{LS1-2}, V_{DD1-2}, Φ_{R1-2} and respectively, Φ_{A3-4}, V_{GS3-4}, Φ_{P3-4}, $VA_{3-4,}$ Φ_{LS3-4}, V_{DD3-4}, Φ_{R3-4} are not connected together inside the package.
2. Two Pins V_{ST} connected together inside the package.

Figure 1. TH7834 Block Diagram



Description

TH7834C high resolution linear array consists of 12000 useful pixel photosensitive line, associated with four CCD shift registers and four output amplifiers. Transfer gates on both sides of the photosensitive line enable delivery of charges, respectively:

- on one side, charge accumulated by odd pixels (1, 3, 5… 11999), to CCD shift registers A and C,
- on the other side, charge accumulated by even pixels (2, 4, 6… 12000), to CCD shift registers B and D.

Shift registers 1 and 2 collect charges generated by one half of the photosensitive line (pixel 1 to 6000), whereas shift registers 3 and 4 collect charges generated by the second half of the photosensitive line (pixels 12000 to 6001).

The four CCD shift registers have separated clocks. The output signal can be, then, delivered simultaneously or sequentially on the four outputs.

The four CCD shift registers are designed with 4 separated gates. According to the gate connection, the signal can be read through 2 or 4 output amplifiers.

According to gate connection, 2 or 4 output operating mode can be chosen. In the 4 output operating mode, signals associated to the end pixels of the array (either pixels number 1, 2 or pixels number 11999, 12000) are delivered first in time and signals corresponding to the center of the line (pixels number 5999, 6000 and 6001, 6002) are delivered last in time. Thus, external circuitry and processing are needed to combine the four video outputs and to restore the normal order of the pixels in accordance with their spatial distribution on the photosensitive line.

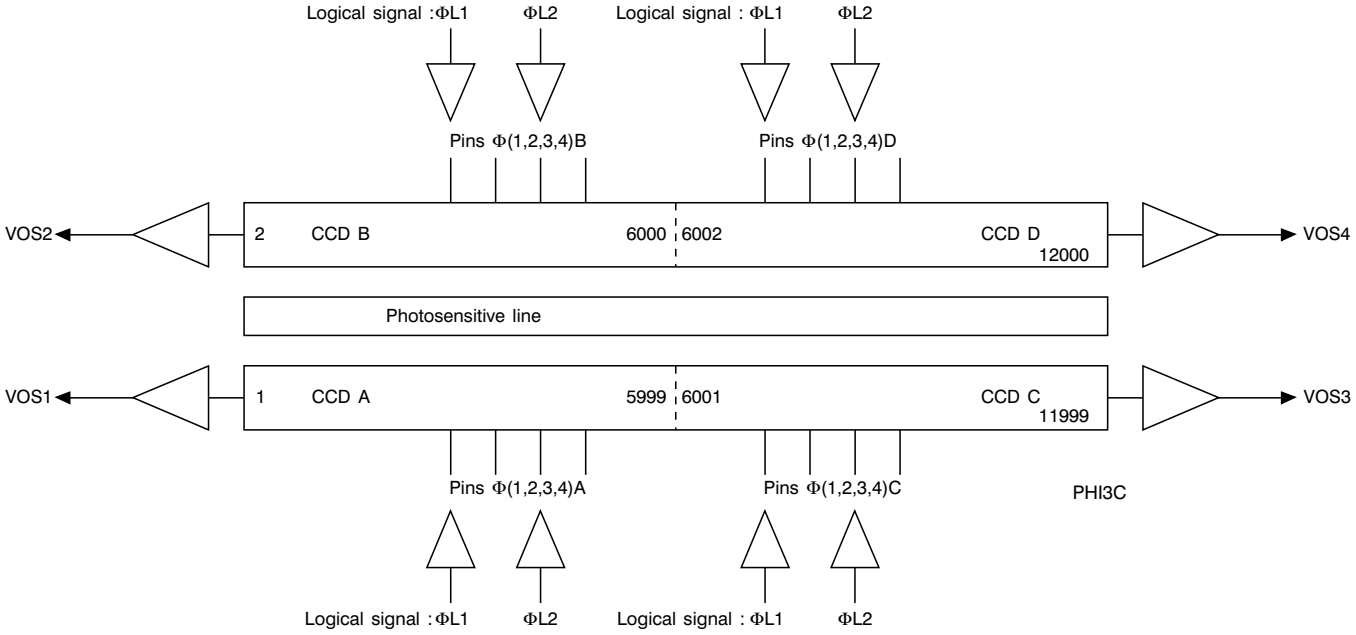
Terminal stages for every CCD shift register have separate clock control inputs in order to speed up the final charge to voltage conversion and reduce the video output settling time.

Antiblooming and exposure time control functions are provided.

Symmetrical TH7834 package PIN OUT allow to inverted pin 1 and 56 positions without damage.

To obtain optimal operating mode, separated driving circuits are recommended for each readout shift register (at least ΦLS and ΦR).

Figure 2. Driving Schematic



Readout Shift Register Clocking

All gates of the 4 CCD shift registers are separated, enabling two or four output readout modes.

To select 2 or 4 outputs operating mode, register main transport gates must be connected as described here after:

- 4 outputs mode:

  V_{OS1}: $\Phi_{L1} = \Phi_{2A} + \Phi_{3A}$; $\Phi_{L2} = \Phi_{1A} + \Phi_{4A}$

  V_{OS2}: $\Phi_{L1} = \Phi_{2B} + \Phi_{3B}$; $\Phi_{L2} = \Phi_{1B} + \Phi_{4B}$

  V_{OS3}: $\Phi_{L1} = \Phi_{2C} + \Phi_{3C}$; $\Phi_{L2} = \Phi_{1C} + \Phi_{4C}$

  V_{OS4}: $\Phi_{L1} = \Phi_{2D} + \Phi_{3D}$; $\Phi_{L2} = \Phi_{1D} + \Phi_{4D}$

- 2 output mode: $V_{OS}1$ and V_{OS2}:

  V_{OS1}: $\Phi_{L1} = \Phi_{2A} + \Phi_{3A} + \Phi_{1C} + \Phi_{2C}$

  $\Phi_{L2} = \Phi_{1A} + \Phi_{4A} + \Phi_{3C} + \Phi_{4C}$

  V_{OS2}: $\Phi_{L1} = \Phi_{2B} + \Phi_{3B} + \Phi_{1D} + \Phi_{2D}$

  $\Phi_{L2} = \Phi_{1B} + \Phi_{4B} + \Phi_{3D} + \Phi_{4D}$

- 2 output mode: V_{OS3} and V_{OS4}:

  V_{OS3}: $\Phi_{L1} = \Phi_{1A} + \Phi_{2A} + \Phi_{2C} + \Phi_{3C}$

  $\Phi_{L2} = \Phi_{3A} + \Phi_{4A} + \Phi_{1C} + \Phi_{4C}$

  V_{OS4}: $\Phi_{L1} = \Phi_{1B} + \Phi_{2B} + \Phi_{2D} + \Phi_{3D}$

  $\Phi_{L2} = \Phi_{3B} + \Phi 4B + \Phi_{1D} + \Phi_{4D}$

Note: In 2 output mode, the unused outputs can be connected as following:
- $\Phi_{LS} = \Phi_R = V_{GS} = 0V$
- $10V < V_{DR} < 15V$
- $V_{DD} = 15V$
- V_S not connected in order to cancel unused output amplifiers power consumption.

Absolute Maximum Ratings*

Storage Temperature	-55°C to + 150°C
Operating Temperature	0°C to + 70°C
Thermal Cycling	15°C/mm
Maximum Voltage:	
• Pins: 4, 6, 7, 8, 10, 11, 12, 13, 16, 17, 18, 19, 21, 23, 32, 34, 35, 36, 38, 39, 40, 41, 44, 45, 46, 47, 49, 51	-0.3V to + 15V
• Pins: 2, 3, 22, 25, 26, 27, 30, 31, 50, 53, 54, 55	-0.3V to + 15.5V
• Pins: 5, 9, 14, 15, 20, 24, 33, 37, 42, 43, 48, 52	Ground 0V

*NOTICE: Stresses above those listed under absolute maximum ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

Operating Range

Operating range defines the temperature limits between which the functionality is guaranteed: 0°C to 70°C.

Operating Precautions

Shorting the video outputs to VSS or VDD, even temporarily, can permanently damage the output amplifiers.

Operating Conditions (T = 25°C)

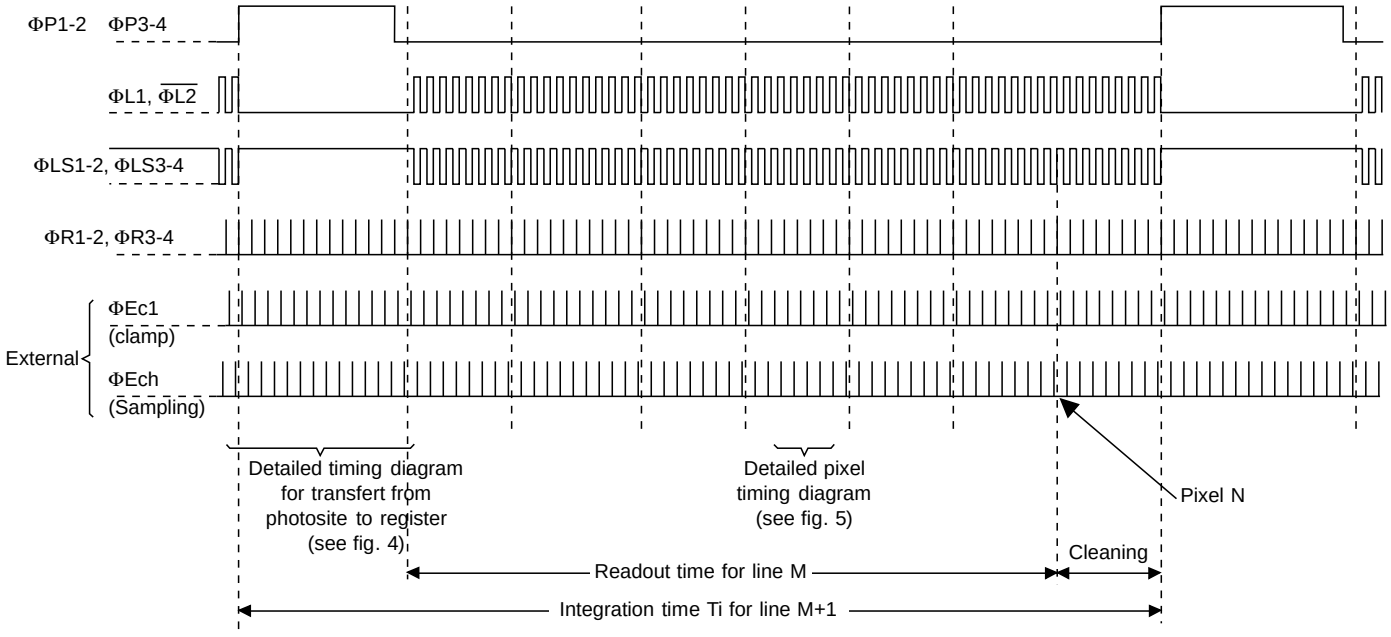
Table 1. DC Characteristics

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Output Amplifier Drain Supply	V_{DD1-2}, V_{DD3-4}	14.5	15	15.5	V
Substrate Voltage	V_{SS}	0	0		V
Reset DC Bias	V_{DR1}, V_{DR2}, V_{DR3}, V_{DR4}		V_{DD} - 0.5		V
Output Amplifier Source Bias	V_{S1}, V_{S2}, V_{S3}, V_{S4}		0		V
Output Gate DC Bias	V_{GS1-2}, V_{GS3-4}	2.2	2.4	2.6	V
Photosensitive Zone DC Bias	V_{ST}	3.5	4	4.5	V
Antiblooming Diode Bias	VA_{1-2}, VA_{3-4}	14	14.5	15	V

Note: If no exposure time control is required, Φ_{A1-2} and Φ_{A3-4} must be connected to an adjustable DC bias (see Figure 7).
Typical current in V_{DR}, V_A < 10 µA; in V_{GS}, V_{ST} < 1 µA.

Timing Diagram

Figure 3. Line Timing Diagram



- Minimum exposure time: Ti min = readout time.
  For data rate of 5 MHz: Ti min = $\frac{3043}{5\ \text{MHz}}$ = 608.6 µs.

Note: It is better to clean the shift registers (with running clocks) and not to stop clocking them after readout time.

- Each video line in four output operating mode consists in:
  - 30 inactive pre-scan, (not connected to pixels),
  - 6 dark references,
  - 4 isolation elements, (inactive, not connected to pixels),
  - 3 non-useful pixels,
  - 3 000 useful pixels of the line.

N = number of pixel periods (T_p) during readout period (see Figure 5).

Four output operating mode: N ≥ 3043.

Two output operating mode: N ≥ 6086.

(Φ_{LS} can be clocked during the line blancking).

Figure 4. Detailed Timing Diagram For Transfer From Photosite To Register

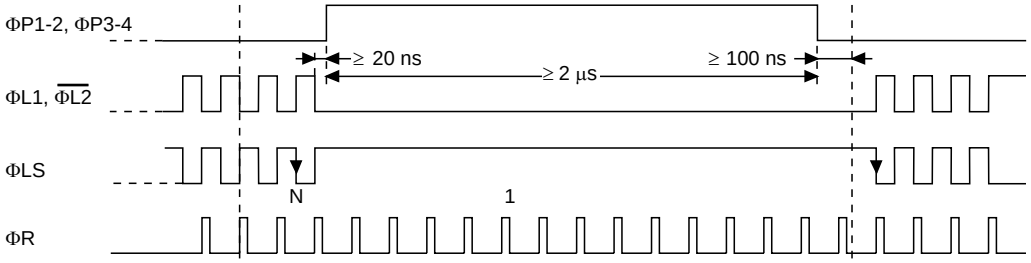
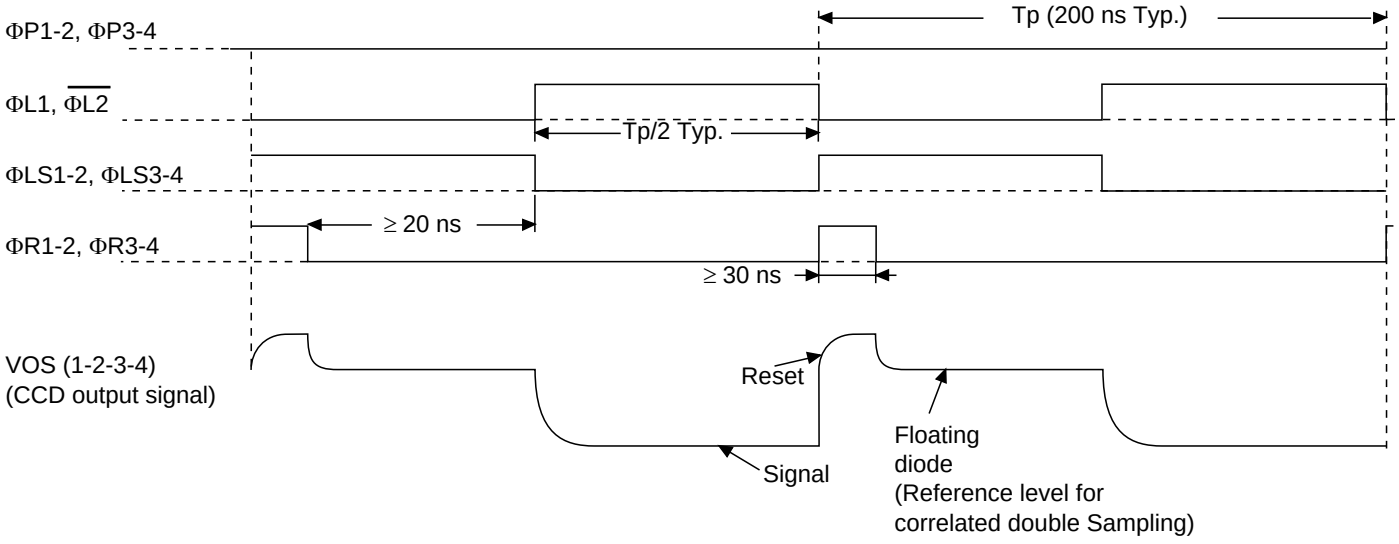


Figure 5. Detailed Pixel Timing Diagram



T_P = Pixel period

Rise and fall time:

Φ_{R1-2}, Φ_{R3-4}: 5% of T_P (min. 5 ns),
Φ_{LS1-2}, Φ_{LS3-4}: 5% of T_P (min. 5 ns),
Φ_{L1}, Φ_{L2}: 25% of TP (min. 30 ns),
Φ_{P1-2}, Φ_{P3-4}: 100 ns (min 20 ns).

Cross over of complementary clocks (Φ_{L1} and Φ_{L2}) preferably at 50% of their amplitude.

Note: Generally, the difference between the floating diode level and signal level is the sum of several signals:
- Register clock feedthrough
- Average CCD register dark signal proportional to CCD clock period, mode, temperature
- Pixel dark signal (depending upon temperature and exposure time)
- Pixel signal under illumination

Table 2.

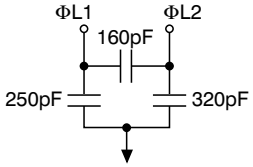
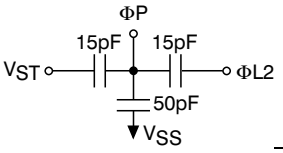
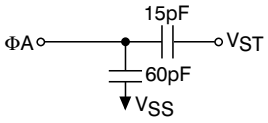
Elements / Signals	Inactive Prescan	Dark References	Isolation Elements	Non Useful Pixels	Useful Pixels
Register Clock Feedthrough	X	X	X	X	X
Average CCD Register Dark Signal	X	X	X	X	X
Pixel Dark Signal		X		X	X
Pixel Signal Under Illumination				X	X

Table 3. Drive Clock Voltage Swings

Parameter	Symbol	Logic	Value			Unit
			Min.	Typ.	Max.	
Register Main Transport Clock(1)	Φ_{L1}, Φ_{L2}	High	8.5	9	11	V
		Low	0	0.4	0.6	V
Register End Transport Clock(1)	Φ_{LS1-2}, Φ_{LS3-4}	High	8.5	9	11	V
		Low	0	0.2	0.4	V
Antiblooming (Low Level) And Exposure Time Control (High Level)(1)	Φ_{A1-2}, Φ_{A3-4}	High	9.5	10	10.5	V
		Low	0	To be adjusted		V
Reset Clock(1)	Φ_{R1-2}, Φ_{R3-4}	High	10.5	11	12.5	V
		Low	0	1.5	2	V
Transfer Clock(1)	Φ_{P1-2}, Φ_{P3-4}	High	10.5	11	11.5	V
		Low	0	0.4	0.6	V

Note: 1. Transients under 0.0V in the clock pulses will lead to charge injection, causing a localized increase of the dark signal. If such spurious negative transients are present, they can be removed by inserting a serial resistor of appropriate value (typically 20 Ω to 100 Ω) at the relevant driver output.

Table 4. Drive Clock Capacitances Operating Frequencies(1)

Symbol	Function/Clock	Capacitive Network	Total	Max. Frequency
Φ_{L1}, Φ_{L2}	Register Main Transport Clock		Φ_{L1}: 570 pF Φ_{L2}: 640 pF for one CCD(1)	10 MHz
Φ_{LS1-2}, Φ_{LS3-4}	Register End Transfer Clock		≤ 50 pF per phase	10 MHz
Φ_{P1-2}, Φ_{P3-4}	Transfer Clock		80 pF per phase	Pulse duration ≥ 2 µs Period: ≥ 608.6 µs (4 outputs mode)
Φ_{A1-2}, Φ_{A3-4}	Antiblooming And Exposure Time Control		100 pF per phase	
Φ_{R1-2}, Φ_{R3-4}	Reset Clock		≤ 50 pF per phase	10 MHz

Note: 1. For ¼ of total CCD register.

Table 5. Static and Dynamic Electrical Characteristics

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
DC Output Level (Pins: 1, 28, 29, 56)	V_{ref}		10		V	
Output Impedance (Pins: 1, 28, 29, 56)	Z_S		400	600	Ω	
Maximum Data Output Frequency Per Channel	F_S max		5	10	MHz	(Note:)
Input Current On Active Pins 4, 6, 7, 8, 10, 11, 12, 13, 16, 17, 18, 19, 21, 23, 32, 34, 35, 36, 38, 39, 40, 41, 44, 45, 46, 47, 49, 51	I_e		<< 1	2	µA	V_{in} = 15V with all other pins = 0V
Amplifier Drain Supply Current (Per V_{DD})	I_{DD1-2}, I_{DD3-4}		10	16	mA	V_{DD} = 15V
Static Power Dissipation (Per V_{DD})	P_{D1-2}, P_{D3-4}		165	240	mW	

Note: The maximum clock frequency is limited by the dark signal increase. Full performance for 5 MHz.

Electro-optical Performance

- General measurement conditions: Tc = 25°C; Ti = 1 ms; $F\Phi_{LA}$, $F\Phi_{LB}$, $F\Phi_{LC}$, $F\Phi_{LD}$ = 5 MHz, readout through 4 outputs.
- Light source: tungsten filament lamp (2,854 K) + BG 38 filter (2 mm thick) + F/3.5 aperture. The BG 38 filter limits the spectrum to 700 nm. In these conditions, 1 µJ/cm^2 corresponds to 3.5 lux.s.
- Typical operating conditions (see Table 1, 2, 3 and 4). First and last pixels of the photosensitive line, as well as reference elements, are excluded from the specification.
- Test without antiblooming, except for AE max.

Table 6. Electro-optical Performance

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Saturation Output Voltage With Antiblooming OFF	V_{SAT}	2	3		V	(1)(2)(3)
Saturation Exposure	E_{SAT}		0.6		µJ/cm^2	
Responsitivity	R	3.5	5		V/µJ/cm^2	
Photo Response Non-uniformity Excluding Single Defects	PRNU		± 6	± 10	% $\overline{VOS}$	$\overline{VOS}$ = 1.0V(4)
Contrast Transfer Function At Nyquist Frequency (77 lp/mm)						
at 500 nm	CTF		75		%	VOS = 1.5V
at 600 nm			62		%	For white level
at 700 nm			47		%	
Temporal Noise In Darkness (rms)			300		µV	(5)
Dynamic Range (Relative to rms Noise)	D_R		10000			
Pixel Average Dark Signal	V_{DS}		110	250	µV/ms	(6)
Dark Signal Non-uniformity	DSNU		90	400	µV/ms	Peak to peak(6)
Register Single Stage Transfer Efficiency	1 - ε	0.99998	0.999998			$\overline{VOS}$ = 1V
Lag (Vertical Charge Transfer Efficiency)	VCTE		0.1	0.5	%	(7)
Antiblooming Efficiency	AE max		<1	15	mV	(8)

Notes:
1. Value measured with respect to zero reference level.
2. Conversion factor is typically: 6 µV/e-.
3. Without antiblooming: $\Phi_{A1-2} = \Phi_{A3-4}$ = 0V.
4. $\overline{VOS}$ = average output voltage; PRNU for each output, in 4 output operating mode.
5. Measured in Correlated Double Sampling (C.D.S.) mode.
6. V_{DS} and DSNU vary with temperature.
7. Residual signal after line readout, at $\overline{VOS}$= 1V.
8. Line acquisition with Phi-A at high level. AE max = maximum signal along the line (to test all the antiblooming sites).

Figure 6. Typical Spectral Responsitivity

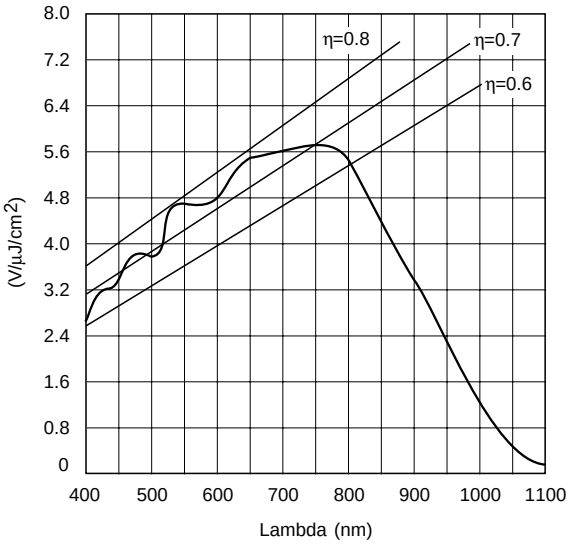
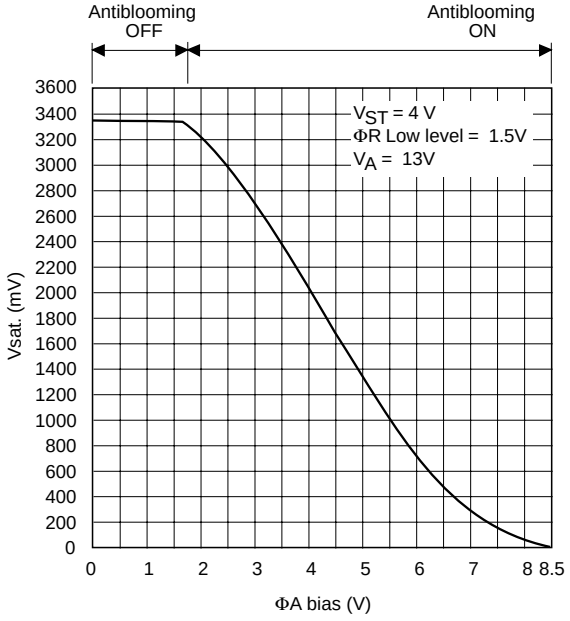


Figure 7. V_{SAT} versus Φ_A Low Level Typical Curve



Exposure Time Reduction (See Figure 8)

TH7834 allows a reduction in the exposure time without changing the readout time. It thus provides a function which is equivalent to an optical iris.

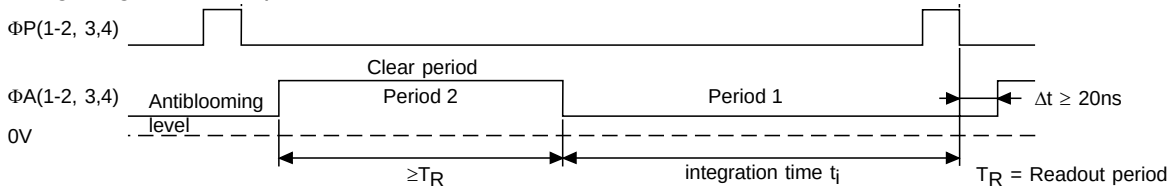
The exposure time reduction consists in increasing the Φ_A gate bias in order to remove continuously, during period 2, the photoelectrons from the pixel and to inject them into the antiblooming diode V_A. When Φ_A returns to the normal bias, electrons are integrated in the pixel.

Only excess electrons are evacuated into V_A (blooming control). Thus, the actual integration time is ti instead of T_i, without any change in the readout sequence. Register transfer and reset clocks (Φ_L, Φ_{LS} and Φ_R) must be pulsed during the T_i integration time.

Table 7. Exposure Time Reduction Conditions

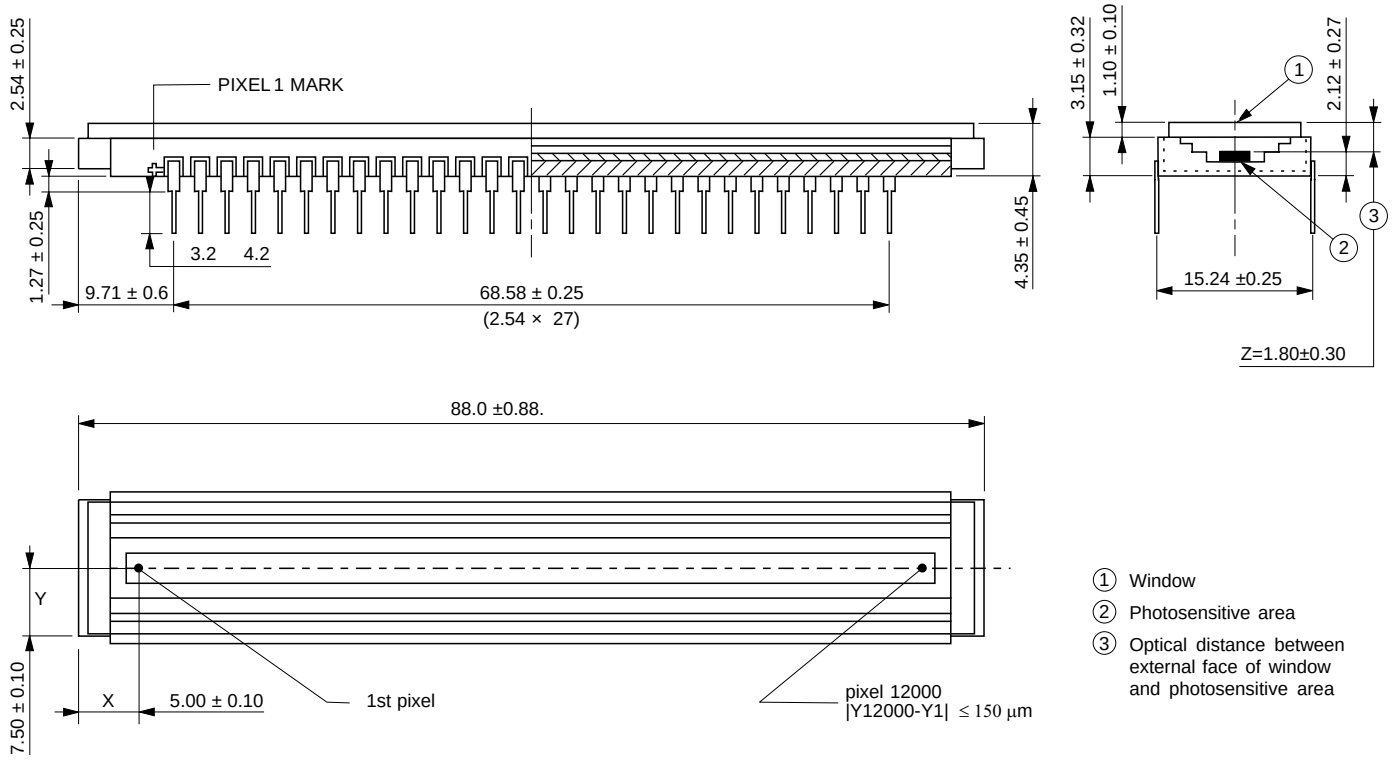
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Antiblooming Diode Bias	VA_{1-2}. VA_{3-4}	14	15.5	15	V
Antiblooming And Expose Time Control Period 1	Φ_{A1-2}, Φ_{A3-4}		to be adjusted		V
Period 2		9.5	10	10.5	V

Figure 8. Timing Diagram For Exposure Time Control



Note: It is better to have Φ_A falling/rising edge outside the useful readout period.

Outline Drawing



Note: Antireflective window: reflection.
Less than 1% per side over 400 - 700 nm wavelength range.
All dimensions are in mm (except otherwise specified).

Ordering Code

The ordering code is TH7834CCC-RB

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