MJE16106

Designer's™ Data Sheet

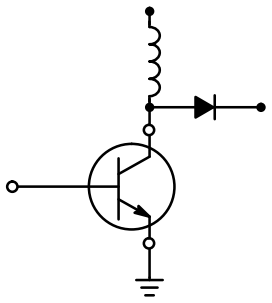
NPN Silicon Power Transistor

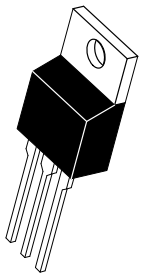
Switchmode Bridge Series

POWER TRANSISTORS
8 AMPERES
400 VOLTS
100 AND 125 WATTS

. . . specifically designed for use in half bridge and full bridge off line converters.

- Excellent Dynamic Saturation Characteristics
- Rugged RBSOA Capability
- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ — 400 V
- Collector–Emitter Breakdown — $V_{(BR)CES}$ — 650 V
- State–of–Art Bipolar Power Transistor Design
- Fast Inductive Switching:
  - t_{fi} = 30 ns (Typ) @ 100°C
  - t_c = 65 ns (Typ) @ 100°C
  - t_{sv} = 1.3 μs (Typ) @ 100°C
- Ultrafast FBSOA Specified
- 100°C Performance Specified for:
  - RBSOA
  - Inductive Load Switching
  - Saturation Voltages
  - Leakages





CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	650	Vdc
Emitter–Base Voltage	V_{EBO}	6	Vdc
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	8 16	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	6 12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above 25°C	P_D	100 40 0.8	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 20 mAdc, I_B = 0)			$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = 650 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 650 Vdc, $V_{BE(off)}$ = 1.5 V, T_C = 100°C)			I_{CEV}	 — —	 — —	 100 1000	μAdc
Collector Cutoff Current (V_{CE} = 650 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	1000	μAdc
Emitter–Base Leakage (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (1)							
Collector–Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 0.25 Adc) (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — — —	 0.2 0.4 0.2 0.3	 0.9 2.0 1.0 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{BE(sat)}$	 — —	 0.9 0.8	 1.5 1.5	Vdc
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	6	13	22	—
DYNAMIC CHARACTERISTICS							
Dynamic Saturation			$V_{CE(dsat)}$	See Figures 11, 12, and 13			V
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	300	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage	I_C = 5.0 A, I_{B1} = 0.5 A, $V_{BE(off)}$ = 5 V, $V_{CE(pk)}$ = 250 V	T_J = 25°C	t_{sv}	—	950	2000	ns
Crossover			t_c	—	45	150	
Fall Time			t_{fi}	—	20	75	
Storage		T_J = 100°C	t_{sv}	—	1300	2600	
Crossover			t_c	—	65	200	
Fall Time			t_{fi}	—	30	125	
Resistive Load (Table 2)							
Delay Time	I_C = 5.0 A, I_{B1} = 0.5 A, V_{CC} = 250 V, PW = 30 μs, Duty Cycle = ≤ 2.0%	I_{B2} = 1.0 A	t_d	—	30	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	1800	—	
Fall Time			t_f	—	100	—	
Storage Time		$V_{BE(off)}$ = 5 V	t_s	—	1200	—	
Fall Time			t_f	—	70	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL STATIC CHARACTERISTICS

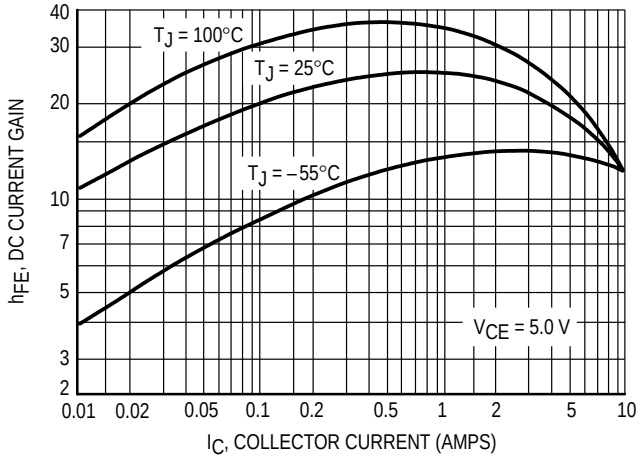


Figure 1. DC Current Gain

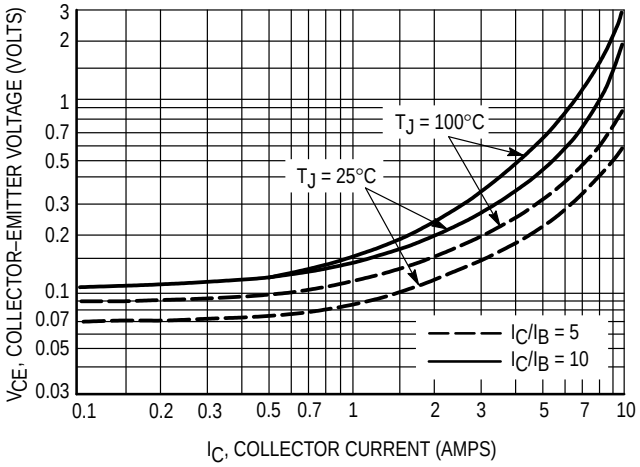


Figure 2. Collector–Emitter Saturation Voltage

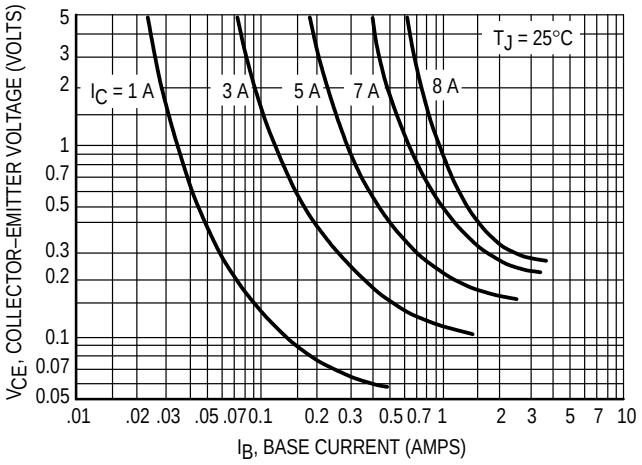


Figure 3. Collector–Emitter Saturation Region

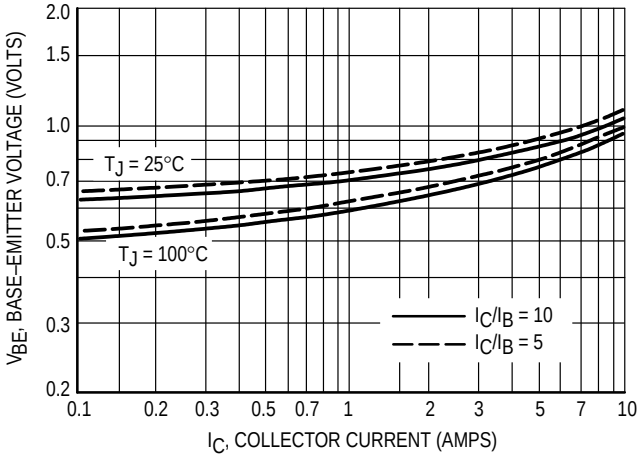


Figure 4. Base–Emitter Saturation Region

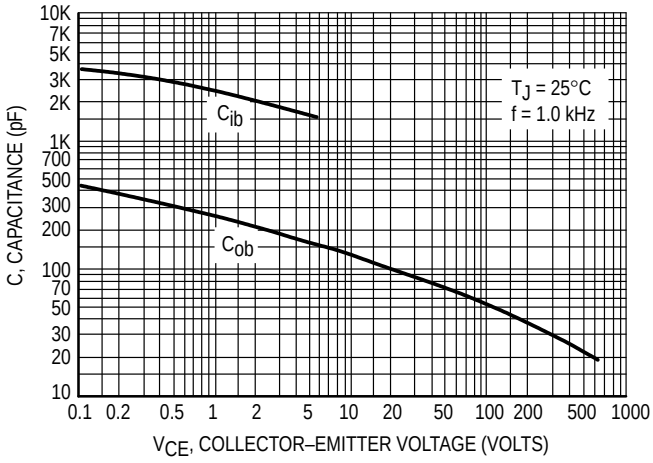


Figure 5. Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS
I_C/I_B = 10, T_C = 100°C, $V_{CE(pk)}$ = 250 V

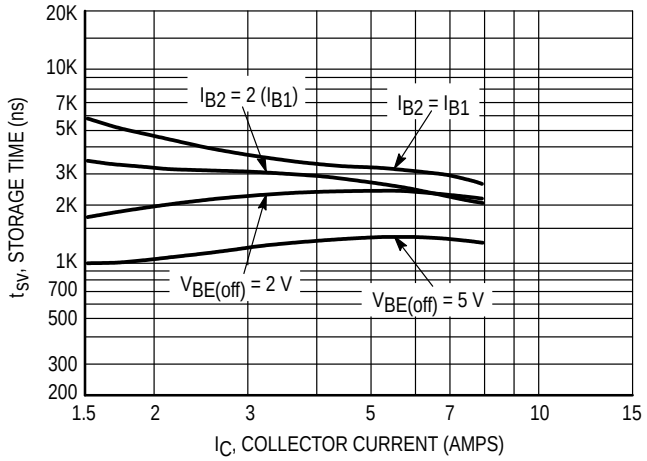


Figure 6. Inductive Storage Time

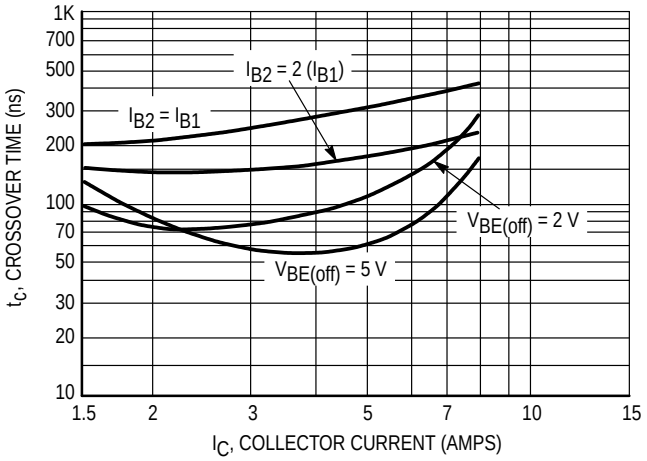


Figure 7. Crossover Time

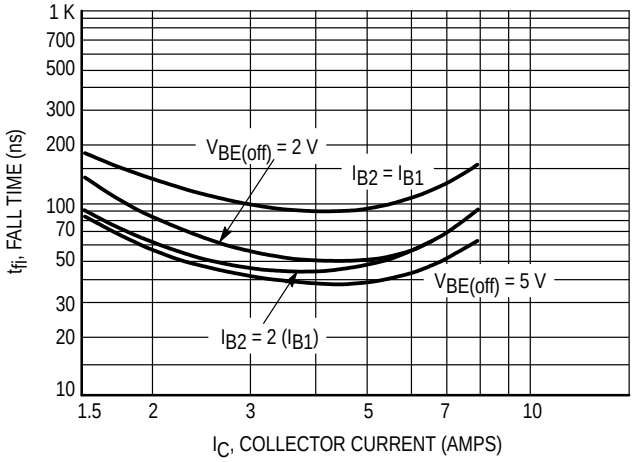


Figure 8. Collector Current Fall Time

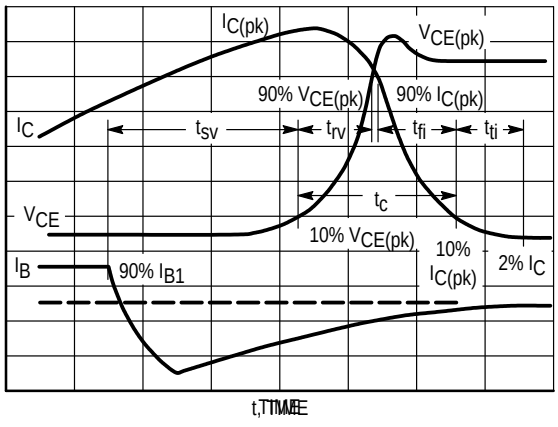


Figure 9. Inductive Switching Measurements

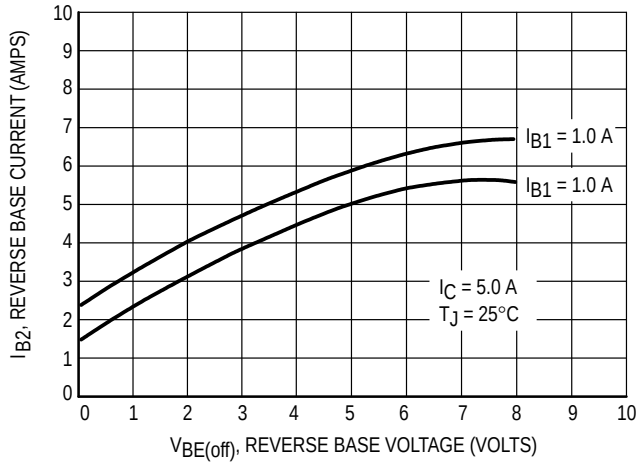
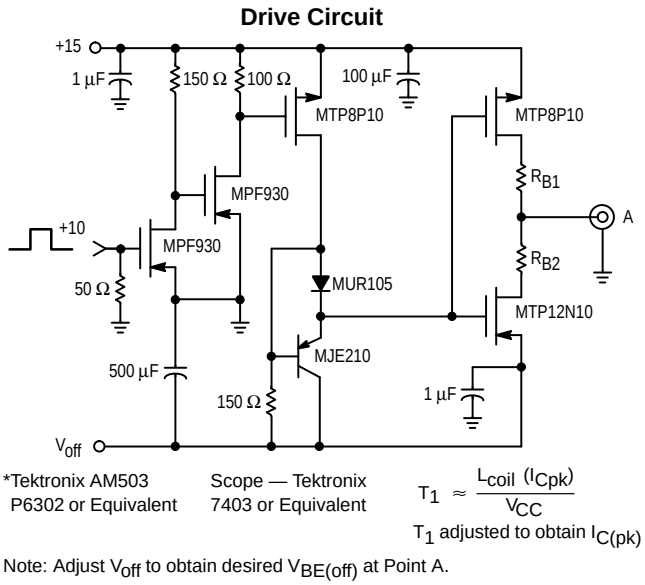


Figure 10. Peak Reverse Base Current

Table 1. Inductive Load Switching



Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts
$I_{C(pk)}$ = 20 mA

Inductive Switching
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

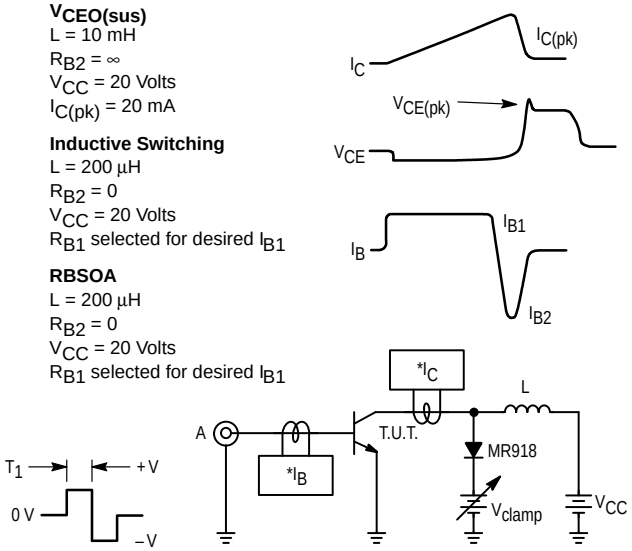
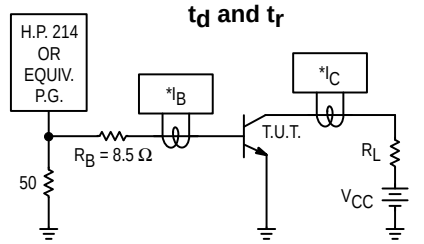
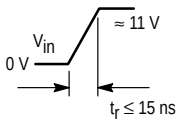


Table 2. Resistive Load Switching

t_d and t_r



V_{CC}	250 Vdc
R_L	25 Ω
I_C	5 A
I_B	0.5 A

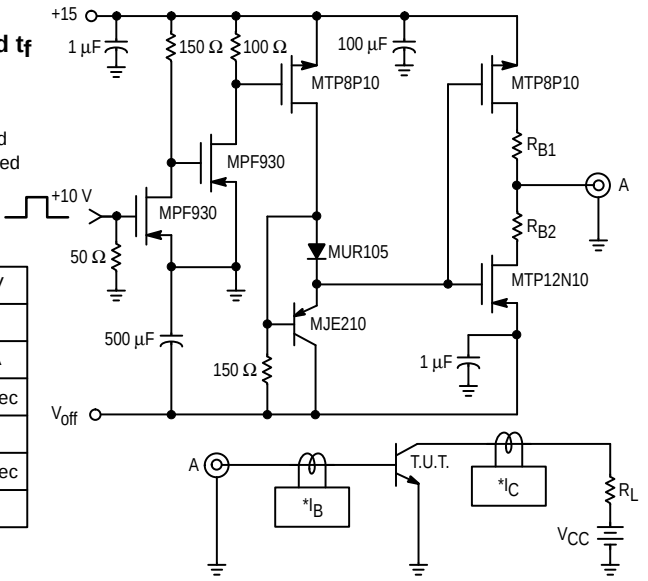


*Tektronix AM503
P6302 or Equivalent

t_s and t_f

$V_{(off)}$ adjusted to give specified off drive

V_{CC}	250 V
I_C	5 A
I_{B1}	0.5 A
I_{B2}	Per Spec
R_{B1}	30 Ω
R_{B2}	Per Spec
R_L	25 Ω



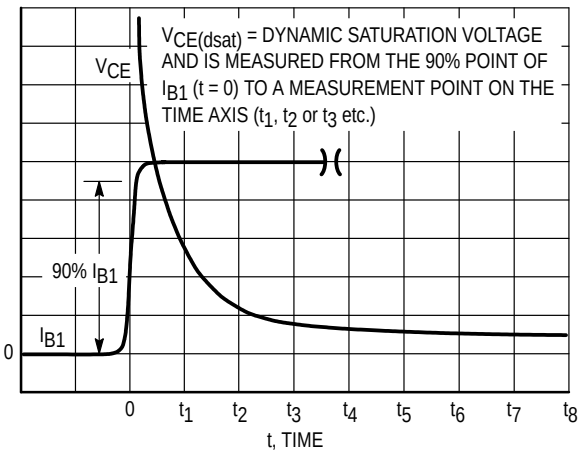


Figure 11. Definition of Dynamic Saturation Measurement

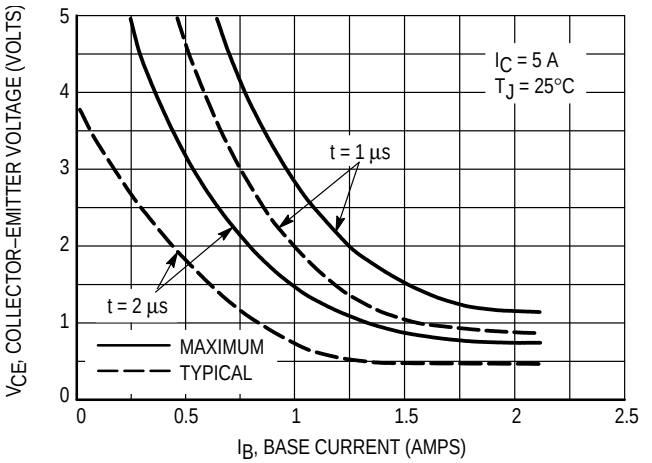


Figure 12. Dynamic Saturation Voltage

DYNAMIC SATURATION VOLTAGE

For bipolar power transistors low DC saturation voltages are achieved by conductivity modulating the collector region. Since conductivity modulation takes a finite amount of time, DC saturation voltages are not achieved instantly at turn–on. In bridge circuits, two transistor forward converters, and two transistor flyback converters dynamic saturation characteristics are responsible for the bulk of dynamic losses. The MJE16106 has been designed specifically to minimize these losses. Performance is roughly four times better than the original version of MJ16006.

From a measurement point of view, dynamic saturation voltage is defined as collector–emitter voltage at a specific point in time after I_{B1} has been applied, where t = 0 is the 90% point on the I_{B1} rise time waveform. This definition is illustrated in Figure 11. Performance data was taken in the circuit that is shown in Figure 13. The 24 volt rail allows a Tektronix 2445 or equivalent scope to operate at 1 volt per division without input amplifier saturation.

Dynamic saturation performance is illustrated in Figure 12. The MJE16106 reaches DC saturation levels in approximately 2 μs, provided that sufficient base drive is provided. The dependence of dynamic saturation voltage upon base drive suggests a spike of I_{B1} at turn–on to minimize dynamic saturation losses, and also avoid overdrive at turn–off. However, in order to simulate worst case conditions the guaranteed dynamic saturation limits in this data sheet are specified with a constant level of I_{B1}.

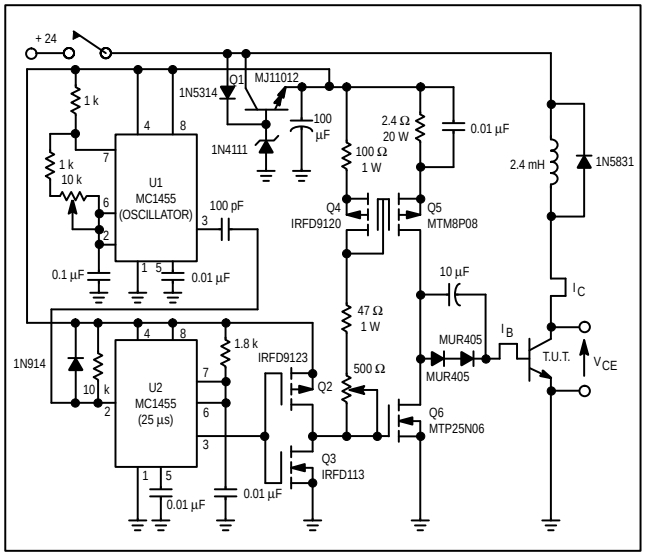


Figure 13. Dynamic Saturation Test Circuit

GUARANTEED SAFE OPERATING AREA INFORMATION

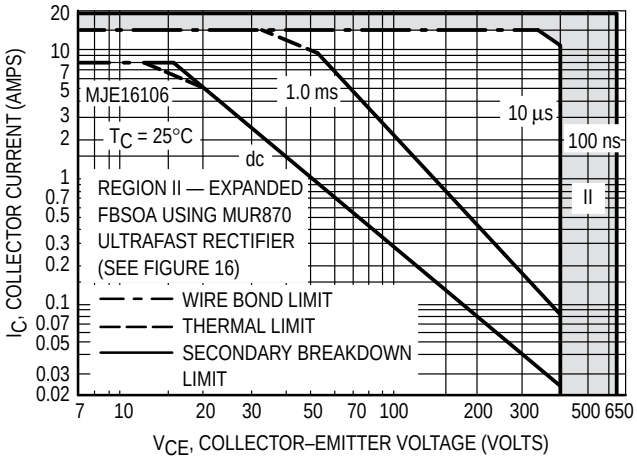


Figure 14. Maximum Rated Forward Bias Safe Operating Area

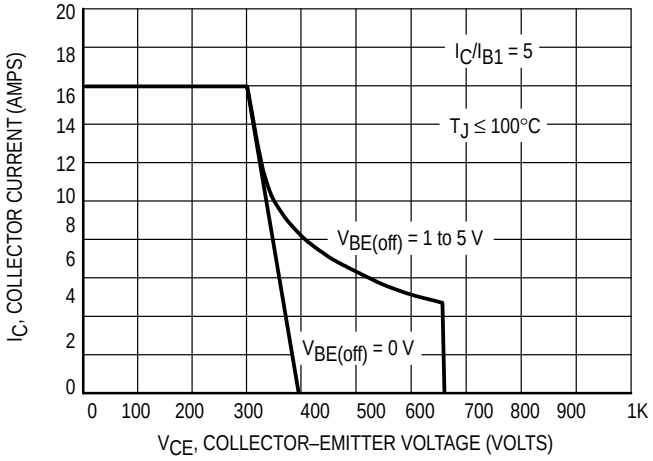


Figure 15. Maximum Rated Reverse Bias Safe Operating Area

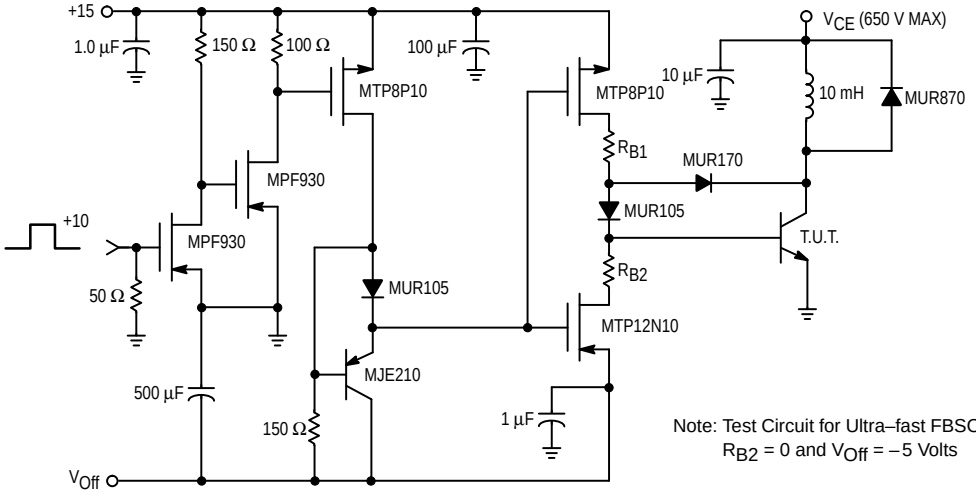


Figure 16. Switching Safe Operating Area

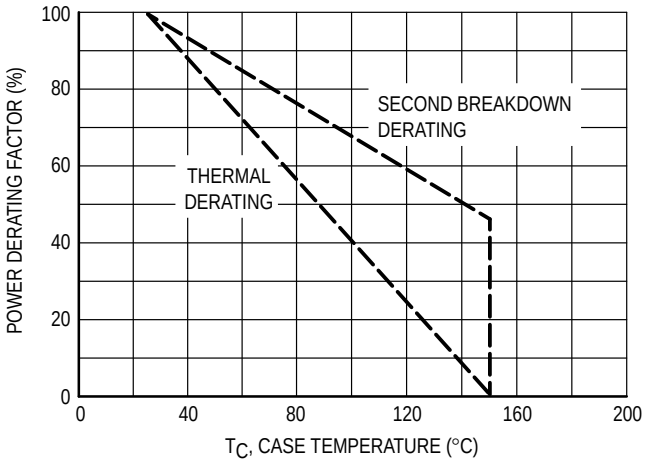


Figure 17. Power Derating

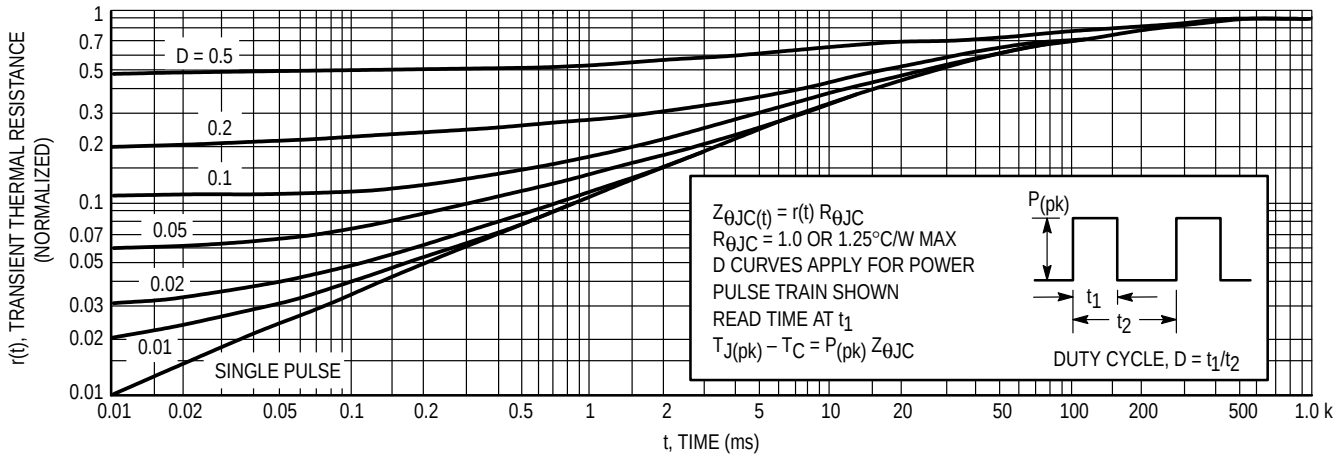


Figure 18. Typical Thermal Response [$Z_{\theta JC}(t)$]

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data in Figure 14 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

FBSOA

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector–emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{(BR)CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

TURN–ON

Safe turn–on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra–fast recovery rectifiers, and are valid for turn–on crossover times less than 100 ns (AN952).

At voltages above 75% of $V_{(BR)CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn–on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

TURN–OFF

A bipolar transistor's ability to withstand turn–off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

OPERATION ABOVE $V_{(BR)CEO(sus)}$

When bipolars are operated above collector–emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn–on, as is a stiff negative bias needed for safe turn–off. Any hiccup in the base–drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

RBSOA

Reversed Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

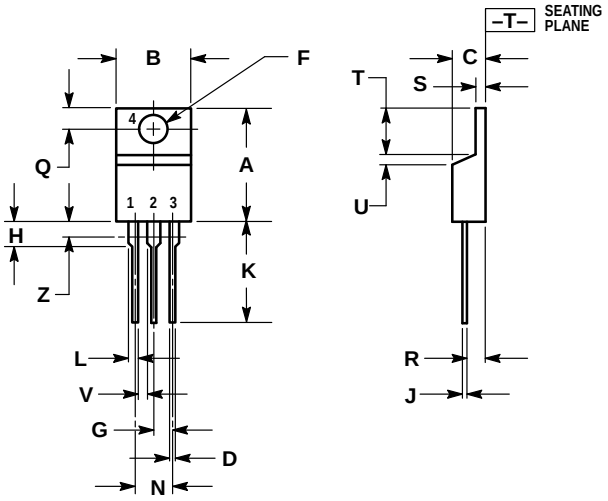
DESIGN SAMPLES

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

BAKER CLAMPS

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR170 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR470 types are well–suited for higher drive requirements (see Article Reprint AR131).

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y

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