

SANYO

No.3256

LC7938C

a-Si Contact Type
Image Sensor-Use Driver

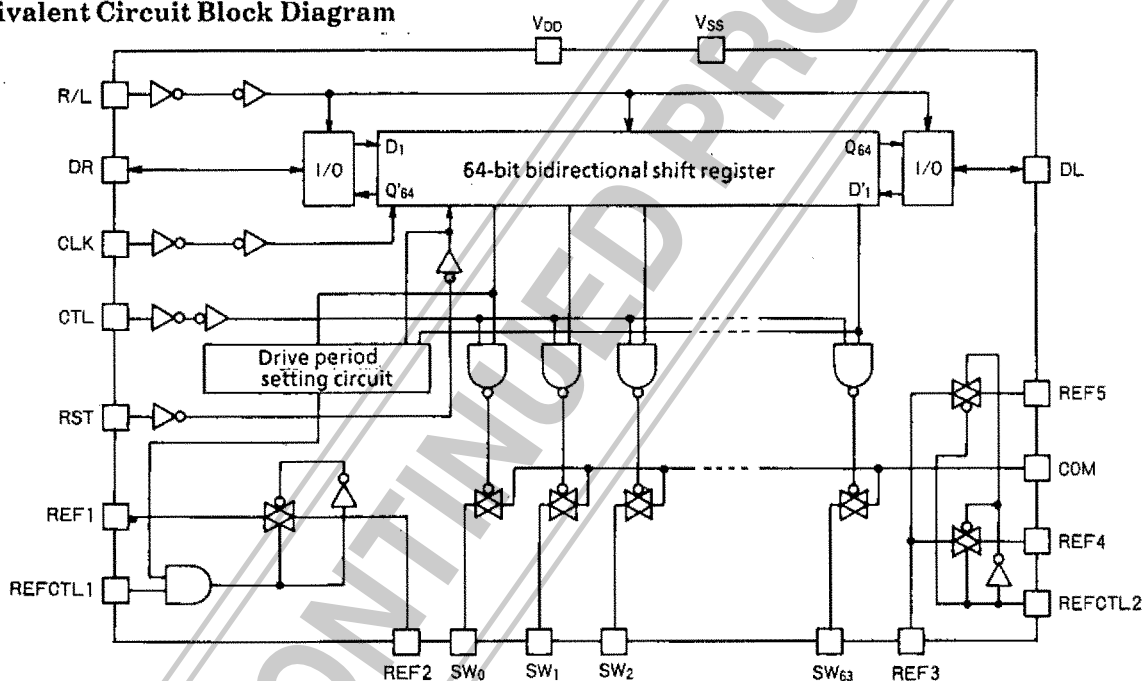
Features

- High-speed silicon gate CMOS device
- On-chip high-speed shiftable (5MHz max.) 64-bit bidirectional shift register, 64-bit sensor driver analog switch
- On-chip CTL signal (CTL) to turn OFF 64-bit sensor driver analog switch
- On-chip noise cancel analog switch

Package

Available in chip form, Chip size : 1.67mm×6.63mm, Number of pads : 80

Equivalent Circuit Block Diagram



Electrical Characteristics

The Electrical Characteristics shown below are for the LC7938C placed in our standard ceramic package.

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Limits	unit
Maximum Supply Voltage	V _{CC} max		-0.3 to +7.0	V
Input Voltage	V _{IN}		-0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT}		-0.3 to V _{DD} + 0.3	V
Operating Temperature	T _{opr}	(Junction temperature)	-25 to +85	°C
Storage Temperature	T _{stg}		-40 to +125	°C

Note) The die bond temperature and other parameters are listed in the common specification for quality assurance prepared separately.

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LC7938C

Allowable Operating Conditions at Ta = 25 ± 2°C, VSS = 0V

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Supply Voltage	VDD			4.5	5.0	5.5	V
Input 'H'-Level Voltage	VIH	CLK, DR, DL, RST, R/L, CTR,		0.7VDD		VDD	V
Input 'L'-Level Voltage	VIL	REFCTL1, REFCTL2		0		0.3VDD	V
Operating Frequency	fCLK	CLK	Duty = 1/2 ± 10%			5.0	MHz
Clock Pulse Width	f _{φWH}	CLK		100			ns
Data Setup Time	t _{DS}	CLK, DR, DL		50			ns
Data Hold Time	t _{DH}			50			ns
Reset Pulse Width	f _{RW}	RST		125			ns
Reset OFF Time	t _{RS}	RST, CLK		125			ns
Maximum Clock Rise/Fall Time	t _r , t _f	CLK	Duty = 1/2 ± 10%			150	ns

Electrical Characteristics at Ta = 25 ± 2°C, VDD = 4.5 to 5.5V, VSS = 0V

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Output 'H'-Level Voltage	VOH	DR, DL	I _{OH} = -0.3mA	VDD - 0.3		VDD	V
Output 'L'-Level Voltage	VOL		I _{OL} = 0.3mA	0		0.3	V
Analog SW ON Resistance	R _{ON(1)}	SW ₀ to SW ₆₃ to COM	COM = 0V, VDD = 5V, SW ₀ to SW ₆₃ = 0.2V		1.0		kΩ
	R _{ON(2)}		COM = 0.2V, VDD = 5V, SW ₀ to SW ₆₃ = 0V		1.0		kΩ
	R _{ON(3)}	REF1 to REF2	REF1 = 0V, VDD = 5V, REF2 = 0.2V		1.0		kΩ
	R _{ON(4)}		REF1 = 0.2V, VDD = 5V, REF2 = 0V		1.0		kΩ
	R _{ON(5)}	REF3 to REF4	REF3 = 0V, VDD = 5V, REF4 = 0.2V		200		Ω
	R _{ON(6)}		REF3 = 0.2V, VDD = 5V, REF4 = 0V		200		Ω
	R _{ON(7)}	REF3 to REF5	REF3 = 0V, VDD = 5V, REF5 = 0.2V		200		Ω
	R _{ON(8)}		REF3 = 0.2V, VDD = 5V, REF5 = 0V		200		Ω

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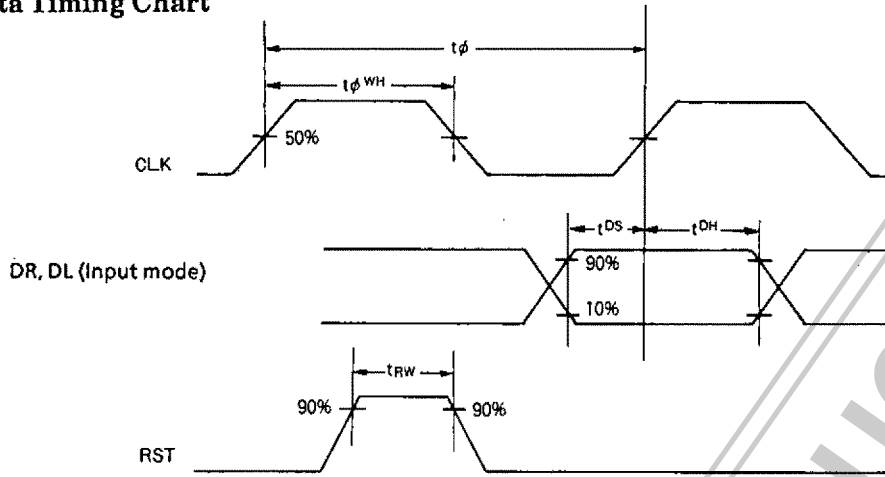
Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Input/Output OFF Leakage Current	I _{OFF(1)}	SW ₀ to SW ₆₃ COM	Analog SW OFF, COM = 0V, SW ₀ to SW ₆₃ = V _{DD} , sum of individual pole leakage currents V _{DD} = 5V, T _a = 60°C			1.0	μA
	I _{OFF(2)}					1.0	μA
Input Capacitance	C1	SW ₀ to SW ₆₃			(1.5)		pF
	C2	COM				(150)	pF
Operating Current Dissipation	I _{DD}	V _{DD}	All outputs open, f = 1MHz			1	mA

(): "Design to" value

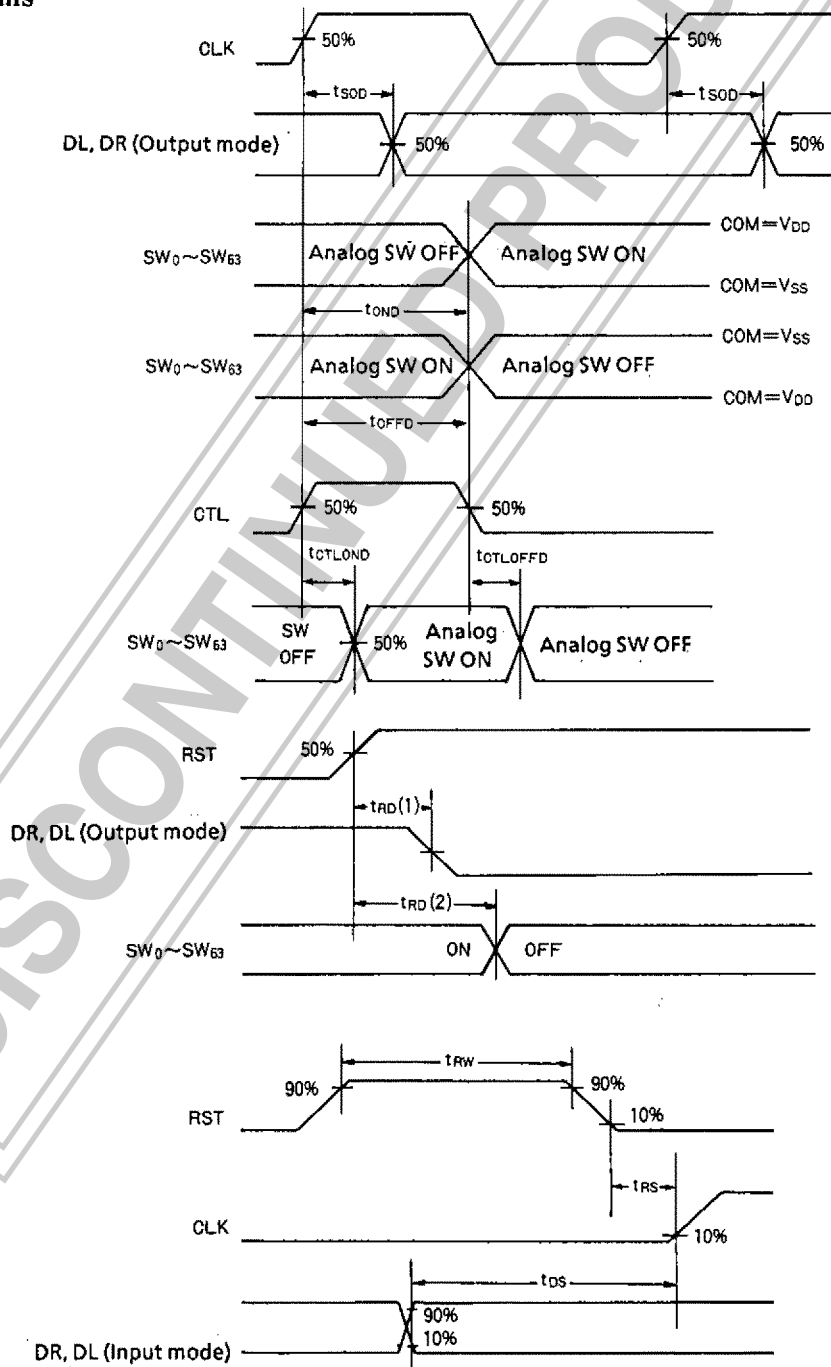
Switching Characteristics at T_a = 25 ± 2°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Analog SW Turn-ON Delay Time	t _{OND}	CLK → SW ₀ to SW ₆₃	CTL = V _{DD} , RST = V _{SS} ,			150	ns
Analog SW Turn-OFF Delay Time	t _{OFFD}	CLK → SW ₀ to SW ₆₃	C _L = 20pF, R _L = 1kΩ			150	ns
Data Output Delay Time	t _{SOD}	CLK → DR, DL	C _L = 20pF			200	ns
Reset Signal Delay Time	t _{RD(1)}	RST → DR, DL	C _L = 20pF			200	ns
	t _{RD(2)}	RST → SW ₀ to SW ₆₃	CTL = V _{DD} , C _L = 20pF, R _L = 1kΩ			200	ns
Control Signal Delay Time	t _{CTL-OND(1)}	CTL → SW ₀ to SW ₆₃	C _L = 20pF, R _L = 1kΩ			120	ns
	t _{CTL-OND(2)}	REFCTL1 → REF1 (REF2)				120	ns
	t _{CTL-OND(3)}	REFCTL2 → REF3 (REF4) (REF5)	C _L = 20pF, R _L = 200Ω			120	ns
	t _{CTL-OFFD(1)}	CTL → SW ₀ to SW ₆₃	C _L = 20pF, R _L = 1kΩ			120	ns
	t _{CTL-OFFD(2)}	REFCTL1 → REF1 (REF2)				120	ns
	t _{CTL-OFFD(3)}	REFCTL2 → REF3 (REF4) (REF5)	C _L = 20pF, R _L = 200Ω			120	ns
Maximum Clock Rise/Fall Time	t _r , t _f	CLK	Duty = 1/2 ± 10%	150			ns

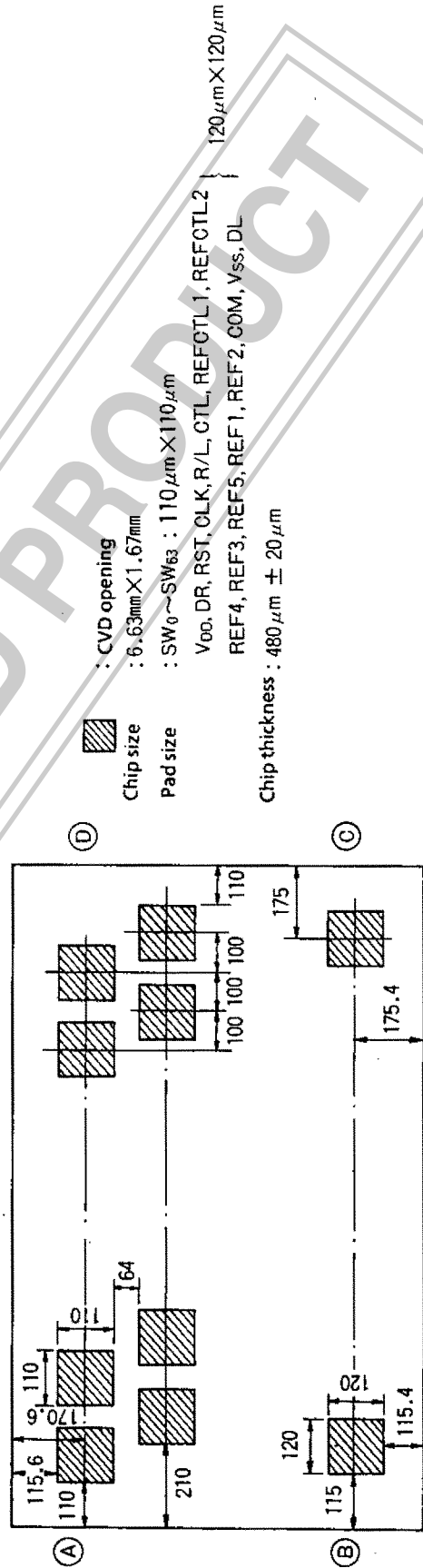
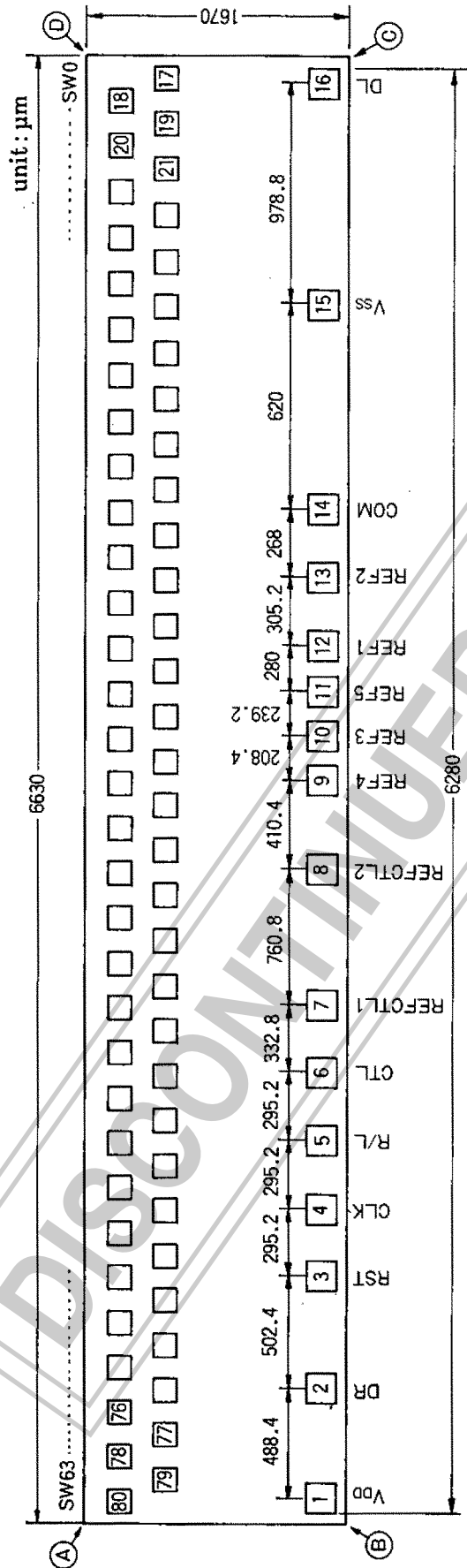
Input Data Timing Chart



Switching Waveforms



Pad Layout



LC7938C Pad Coordinates

Pad No.	Signal Name	X Coordinate μm	Y Coordinate μm	Pad No.	Signal Name	X Coordinate μm	Y Coordinate μm
1	VDD	-659.6	3140	41	SW39	490.4	-750
2	DR	-659.6	2651.6	42	38	664.4	-650
3	RST	-659.6	2149.2	43	37	490.4	-550
4	CLK	-659.6	1854	44	36	664.4	-450
5	R/L	-659.6	1558.8	45	35	490.4	-350
6	CTL	-659.6	1263.6	46	34	664.4	-250
7	REFCTL1	-659.6	930.8	47	33	490.4	-150
8	REFCTL2	-659.6	170	48	32	664.4	-50
9	REF4	-659.6	-240.4	49	31	490.4	50
10	REF3	-659.6	-448.8	50	30	664.4	150
11	REF5	-659.6	-688	51	29	490.4	250
12	REF1	-659.6	-968	52	28	664.4	350
13	REF2	-659.6	-1273.2	53	27	490.4	450
14	COM	-659.6	-1541.2	54	26	664.4	550
15	Vss	-659.6	-2161.2	55	25	490.4	650
16	DL	-659.6	-3140	56	24	664.4	750
17	SW63	490.4	-3150	57	23	490.4	850
18	62	664.4	-3050	58	22	664.4	950
19	61	490.4	-2950	59	21	490.4	1050
20	60	664.4	-2850	60	20	664.4	1150
21	59	490.4	-2750	61	19	490.4	1250
22	58	664.4	-2650	62	18	664.4	1350
23	57	490.4	-2550	63	17	490.4	1450
24	56	664.4	-2450	64	16	664.4	1550
25	55	490.4	-2350	65	15	490.4	1650
26	54	664.4	-2250	66	14	664.4	1750
27	53	490.4	-2150	67	13	490.4	1850
28	52	664.4	-2050	68	12	664.4	1950
29	51	490.4	-1950	69	11	490.4	2050
30	50	664.4	-1850	70	10	664.4	2150
31	49	490.4	-1750	71	9	490.4	2250
32	48	664.4	-1650	72	8	664.4	2350
33	47	490.4	-1550	73	7	490.4	2450
34	46	664.4	-1450	74	6	664.4	2550
35	45	490.4	-1350	75	5	490.4	2650
36	44	664.4	-1250	76	4	664.4	2750
37	43	490.4	-1150	77	3	490.4	2850
38	42	664.4	-1050	78	2	664.4	2950
39	41	490.4	-950	79	1	490.4	3050
40	40	664.4	-850	80	0	664.4	3150

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