3-in-1 ACPI Regulator/Controller for Dual Channel DDR and DDR2 Memory Systems

The ISL6532A provides a complete ACPI compliant power solution for dual channel DDR/DDR2 Memory systems. Included are both a synchronous buck controller and integrated LDO to supply VDDQ with high current during S0/S1 (Run) states and standby current during S3 (suspend-to-RAM = STR) state. During Run mode, a fully integrated sink-source regulator generates an accurate (VDDQ/2) high current VTT voltage without the need for a negative supply. A buffered version of the VDDQ/2 reference is provided as V_{REF}.

The VDDQ PWM controller drives two N-Channel MOSFETs in a synchronous-rectified buck converter topology. The synchronous buck converter incorporates simple, single feedback loop, voltage-mode control with fast transient response. Both the switching regulator and standby LDO provide a maximum static regulation tolerance of ±2% over line, load, and temperature ranges. VDDQ is user-adjustable by means of external resistors down to 0.8V.

Switching VDDQ power control between the PWM regulator and the standby LDO during state transitions is accomplished smoothly via the ISL6532A's ACPI control circuitry. The NCH signal provides synchronized switching of a backfeed blocking switch during the transitions.

An integrated soft-start feature brings VDDQ into regulation in a controlled manner when returning to Run mode from S4/S5 (suspend-to-disk = STR) or mechanical off states. During S0 the PGOOD signal indicates that all supplies are within spec and operational.

Each output is monitored via the FB pins for under and over-voltage events. Current limiting is included on the VTT and VDDQ standby regulators. Thermal shutdown is integrated.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
ISL6532ACR	0 to 70	6X6mm 28ld QFN	L28.6X6

Applications

- Single and Dual Channel DDR Memory Power Systems in ACPI compliant PCs
- Graphics cards - GPU and memory supplies
- ASIC power supplies
- Embedded processor and I/O supplies
- DSP supplies

Features

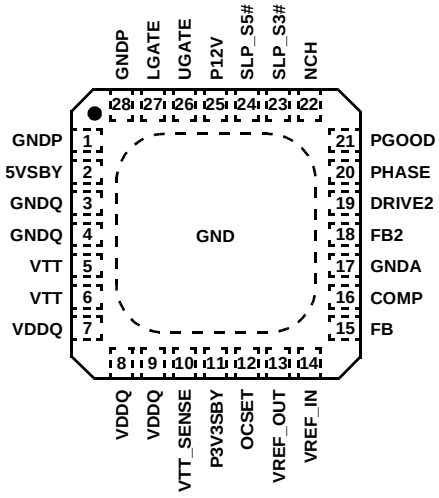
- Generates 3 Regulated Voltages
  - Synchronous Buck PWM Controller with Standby LDO
  - 1.8A Integrated Sink/Source Linear Regulator with accurate VDDQ/2 divider reference.
  - LDO regulator for 1.5V Video and Core voltage
- ACPI compliant sleep state control
- Glitch-free transitioning during state changes
- Integrated V_{REF} Buffer
- PWM Controller Drives Low Cost N-Channel MOSFETs
- 12Volt Direct Drive Saves External Components
- 250kHz Constant Frequency Operation
- Excellent Output Voltage Regulation
  - Both Outputs: ±2% Over Temperature
- 5V or 3.3V Down Conversion
- Fully-Adjustable Outputs with Wide Voltage Range: Down to 0.8V supports DDR and DDR2 Specifications
- Simple Single-Loop Voltage-Mode PWM Control Design
- Fast PWM Converter Transient Response
- Under and Over-voltage Monitoring of VDDQ and VTT Outputs
- Current Limited VTT regulator
- Integrated Thermal Shutdown Protection

Related Literature

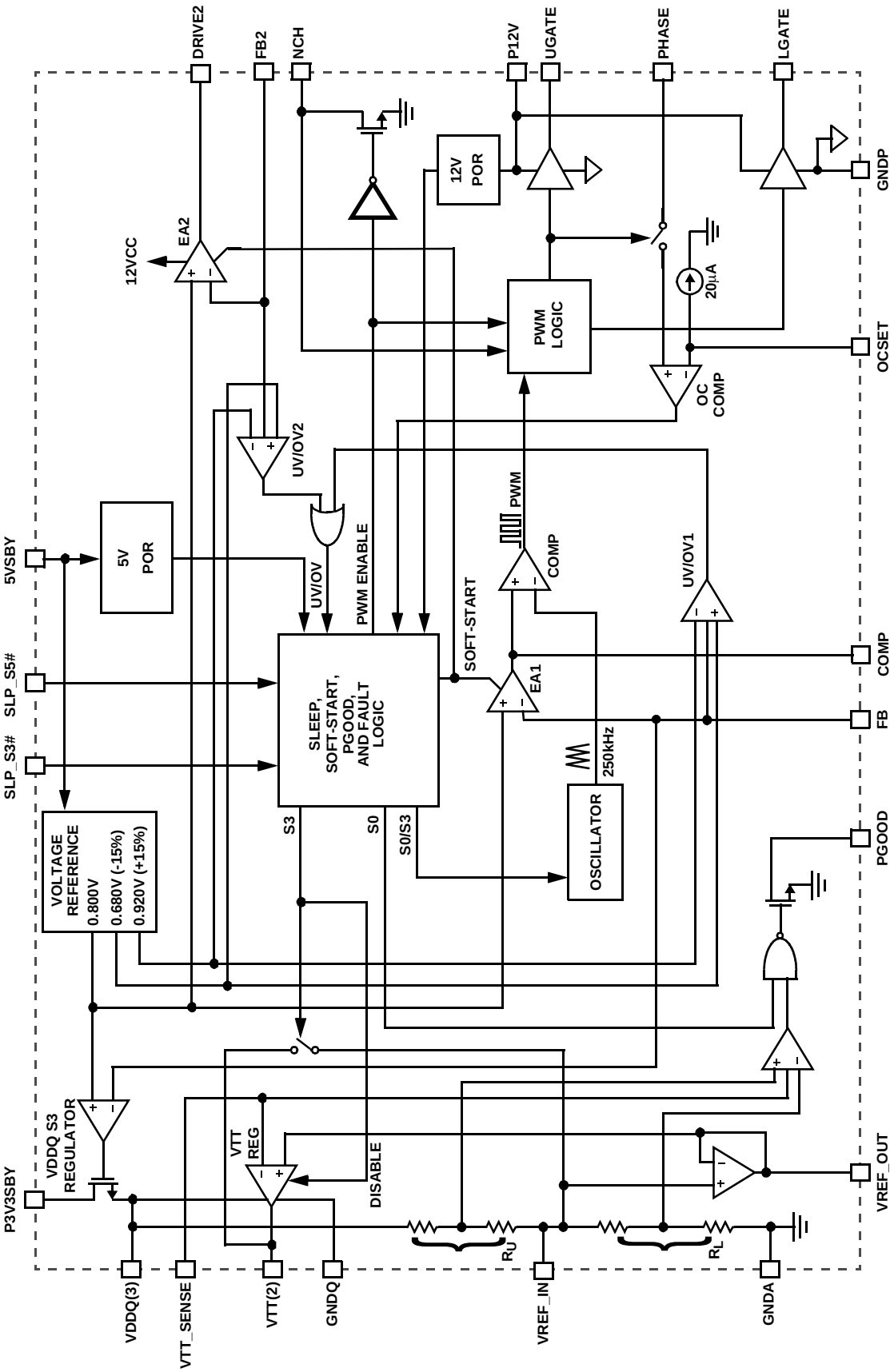
- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Pinout

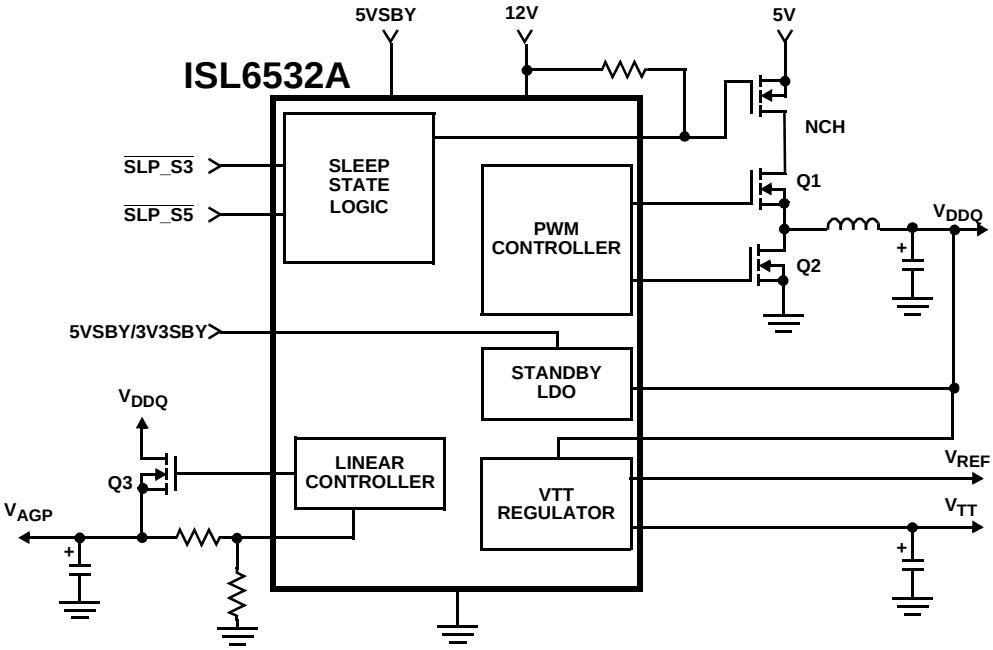
ISL6532A (QFN)
TOP VIEW



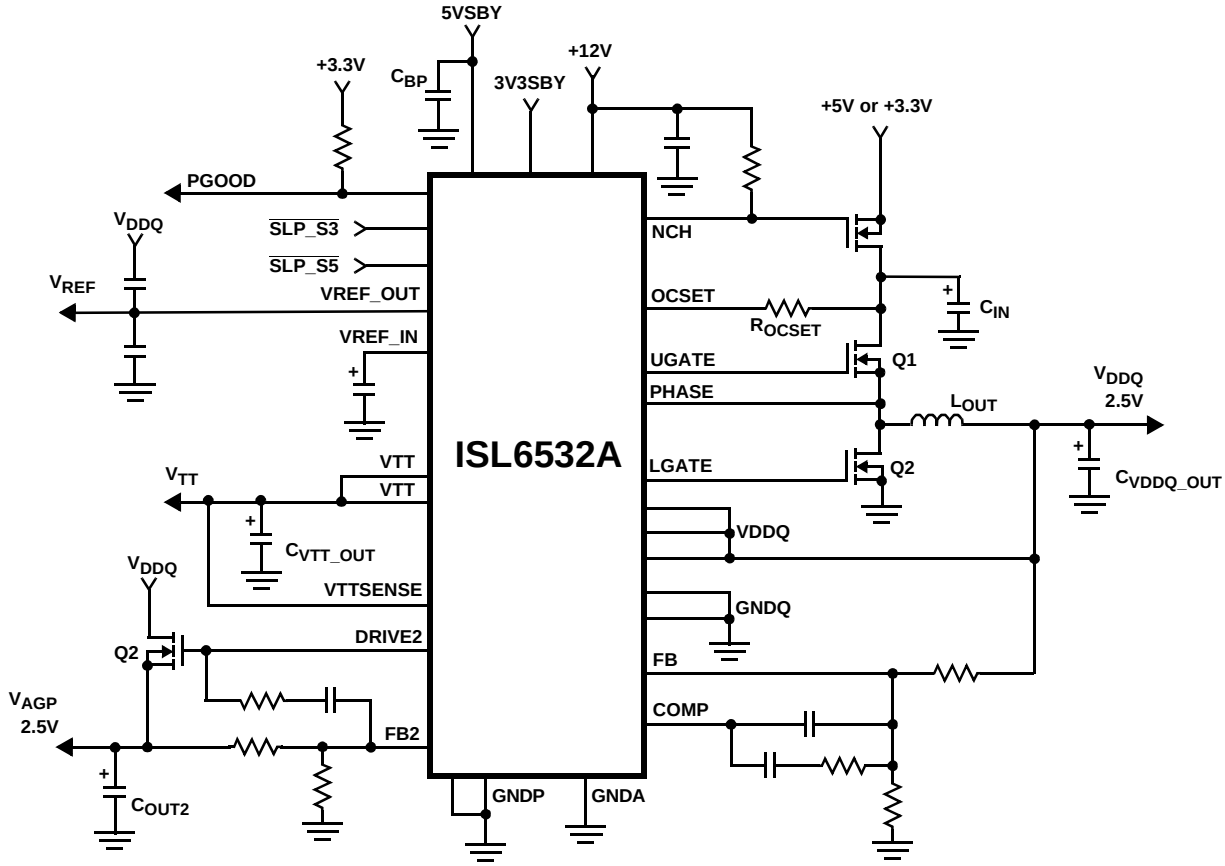
Block Diagram



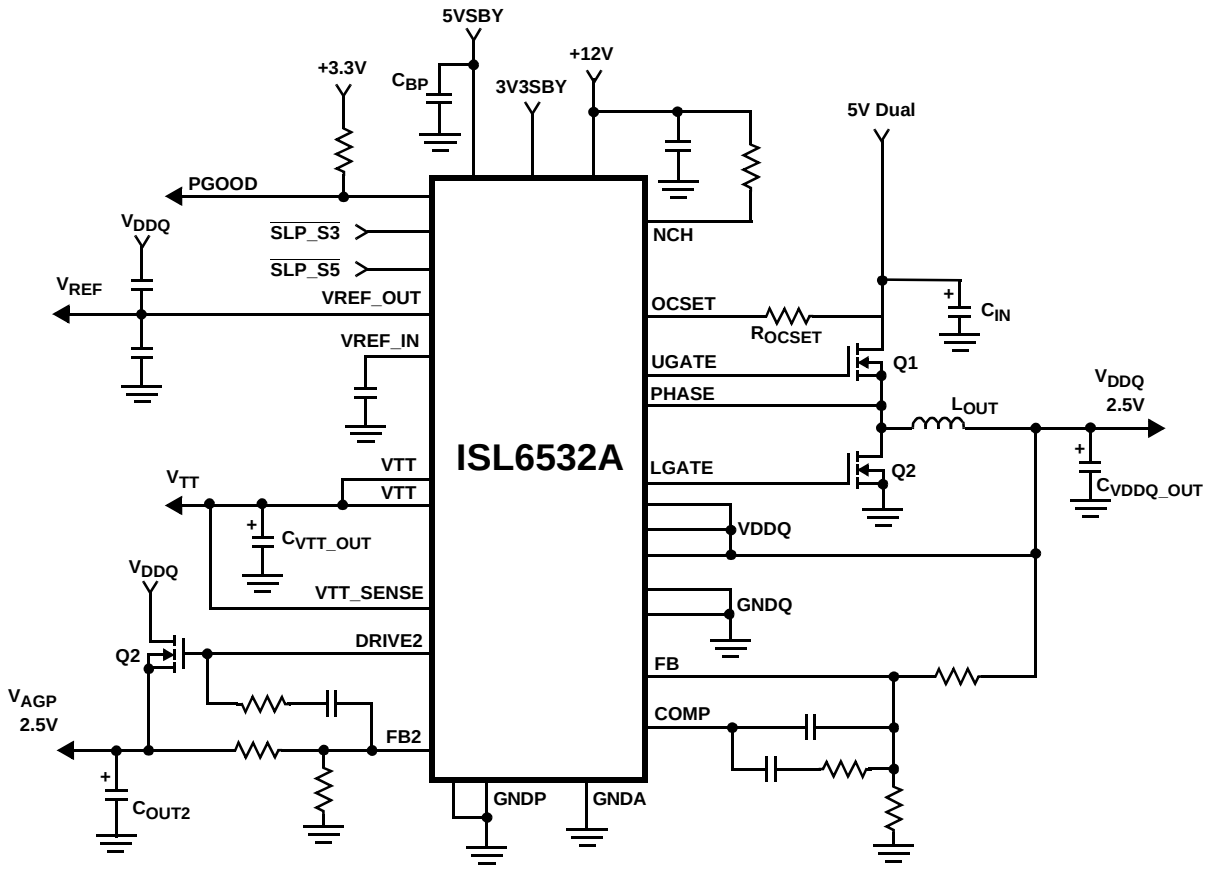
Simplified Power System Diagram



Typical Application - V_{DDQ} From 5 or 3.3V



Typical Application - V_{DDQ} From 5V Dual



Absolute Maximum Ratings

5VSBY . . . . . GND - 0.3V to +7V
P12V . . . . . GND - 0.3V to +14V
UGATE, LGATE, NCH . . . . . GND - 0.3V to P12V + 0.3V
All other Pins . . . . . GND - 0.3V to 5VCC + 0.3V
ESD Classification . . . . . TBD

Recommended Operating Conditions

Supply Voltage on 5VSBY . . . . . +5V ±10%
Supply Voltage on P12V . . . . . +12V ±10%
Supply Voltage on 3V3SBY . . . . . +3.3V ±10%
Ambient Temperature Range . . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
QFN Package	32

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
For Recommended Soldering Conditions, See Intersil Tech Brief TB334.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams and Typical Application Schematics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{CC0}	S0	-	5	-	mA
	I_{CC3}	S3	-	TBD	-	
	I_{CC5}	S5	-	800	-	µA
POWER-ON RESET						
Rising 5VSBY POR Threshold			-	TBD	-	V
Falling 5VSBY POR Threshold			-	TBD	-	
Rising P12V POR Threshold			-	TBD	-	
Falling P12V POR Threshold			-	TBD	-	
OSCILLATOR AND SOFT-START						
PWM Frequency	f_{OSC}		225	250	275	kHz
Ramp Amplitude	ΔV_{OSC}		-	1.5	-	V
Error Amp Reset Time	t_{RESET}	Mechanical Off/S5 to S0	3.73	4.14	4.55	ms
VDDQ Soft-Start Interval	t_{SS}	Mechanical Off/S5 to S0	3.73	4.14	4.55	ms
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}		0.792	0.800	0.808	V
System Accuracy			-2.0	-	+2.0	%
PWM CONTROLLER ERROR AMPLIFIER						
DC Gain		Guaranteed By Design	-	80	-	dB
Gain-Bandwidth Product	GBWP		15	-	-	MHz
Slew Rate	SR		-	6	-	V/µs
PWM CONTROLLER GATE DRIVERS						
UGATE and LGATE Source	I_{GATE}		-	-1	-	A
UGATE and LGATE Sink	I_{GATE}		-	1	-	A

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams and Typical Application Schematics **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
NCH BACKFEED CONTROL						
NCH Current Sink	I_{NCH}	NCH = 0.8V	-	-	8	mA
NCH Trip Level	V_{NCH}		8.55	9.0	9.45	V
VDDQ STANDBY LDO						
Output Drive Current		3V3SBY > 3.0V	-	-	450	mA
VTT REGULATOR						
Sink/Source Current		5VSBY > 4.5V	-	1.8	-	A
Current Limit	I_{LIMIT}		2.2	-	2.4	A
Upper Divider Impedance	R_U		-	2.5	-	kΩ
Lower Divider Impedance	R_L		-	2.5	-	kΩ
Divider Impedance Matching	R_U/R_L		-	TBD	-	%
VREF_OUT Buffer Source Current	I_{VREF_OUT}		-	-	5	mA
LINEAR REGULATOR						
DC GAIN		Guaranteed By Design	-	80	-	dB
Gain Bandwidth Product	GBWP		15	-	-	MHz
Slew Rate	SR		-	6	-	V/µs
DRIVE2 High Output Voltage			9.5	10.3	-	V
DRIVE2 Low Output Voltage			-	0.1	1.0	V
DRIVE2 High Output Source Current			-.7	-1.4	-	mA
DRIVE2 Low Output Sink Current			.85	1.2	-	mA
PGOOD						
PGOOD Rising Threshold	V_{VTT_SENSE}/V_{VDDQ}	S0		57.5		%
PGOOD Falling Threshold	V_{VTT_SENSE}/V_{VDDQ}	S0		45.0		%
PGOOD Threshold Hysteresis				TBD		%
PROTECTION						
OCSET Current Source	I_{OCSET}		-	20	-	µA
VDDQ OV Level	V_{FB}/V_{REF}	S0	-	115	-	%
VDDQ UV Level	V_{FB}/V_{REF}	S0	-	85	-	%
Linear Regulator OV Level	V_{FB2}/V_{REF}	S0	-	115	-	%
Linear Regulator UV Level	V_{FB2}/V_{REF}	S0	-	85	-	%
Thermal Shutdown Limit	T_{SD}		-	140	-	°C

Functional Pin Description

This section provides a description of each of the 28 pins of the ISL6532A as shown in Figure1.

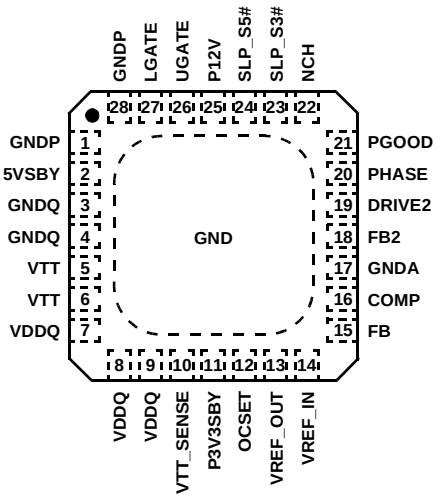


FIGURE 1. 28 LEAD QFN TERMINAL ASSIGNMENTS

5VSBY (5 Volt Standby)

5VSBY is the primary supply to the state and control logic and to the analog references and blocks of the ISL6532A. It is typically connected to the 5V standby rail of an ATX power supply. During S5 sleep states the ISL6532A enters a reduced power mode and draws less than 1mA (I_{CC5}) from the 5VSBY supply. The supply to 5VSBY should be locally bypassed at the pin

P12V (12V Power)

P12V provides the gate drive to the upper (control) and lower (synchronous) FETs of the PWM power stage. The VTT regulation circuit and the Linear Driver are also powered by P12V. P12V is not required except during S0/S1 operation. P12V is typically connected to the +12V rail of an ATX power supply.

P3V3SBY (3.3V or 5V Standby)

The VDDQ standby regulator supply is fed from the P3V3SBY pin. The regulator is capable of providing standby VDDQ power from either a 3.3V or 5V source.

GNDA, GNDP, GNDQ (Ground)

The GND terminals of the ISL6532A provide the return path for all power supplies. High ground currents are conducted directly through the exposed paddle of the MLFP package which must be electrically connected to the ground plane through a path as low in inductance as possible. GNDA is the Analog ground pin, GNDQ is the return for the VTT regulator and GNDP is the return for the upper and lower gate drives.

UGATE (Upper FET Gate Drive)

UGATE drives the upper (control) FET of the VDDQ synchronous buck switching regulator. UGATE is driven between GND and P12V.

LGATE (Lower FET Gate Drive)

LGATE drives the lower (synchronous) FET of the VDDQ synchronous buck switching regulator. LGATE is driven between GND and P12V.

FB (Feedback) and COMP (Compensation)

The VDDQ switching regulator employs a single voltage control loop. FB is the negative input to the voltage loop error amplifier. The positive input of the error amplifier is connected to a precision 0.8V reference and the output of the error amplifier is connected to the COMP pin. The VDDQ output voltage is set by an external resistor divider connected to FB. With a properly selected divider, VDDQ can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference. Loop compensation is achieved by connecting an AC network across COMP and FB.

The FB pin is also monitored for under- and over-voltage events.

PHASE

Connect this pin to the upper MOSFET's source. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection.

OCSET

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 20µA current source (I_{OCSET}), and the upper MOSFET on-resistance ($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} x R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

VDDQ

The VDDQ pins should be connect externally together to the regulated VDDQ output. During S0/S1 (Run) states, the VDDQ pins serve as inputs to the VTT regulator and to the VTT Reference precision divider. During S3 (Suspend to RAM) state, the VDDQ pins serve as an output from the integrated standby LDO.

VTT

The VTT pins should be connect externally together. During S0/S1 states, the VTT pins serve as the outputs of the VTT linear regulator. During S3 state, the VTT regulator is disabled.

VTT_SENSE

VTT_SENSE is used as the feedback for control of the VTT linear regulator. Connect this pin to the VTT output at the physical point of desired regulation.

VREF_OUT

VREF_OUT is a buffered version of VTT and also acts as the reference voltage for the VTT linear regulator. It is recommended that a minimum capacitance of 0.1µF is connected between VDDQ and VREF_OUT and also between VREF_OUT and GND for proper operation.

VREF_IN

A capacitor, C_{SS}, connected between VREF_IN and Ground is required. This capacitor, in combination with the Upper Divider Impedance (R_U), sets the time constant for the start up ramp when transitioning from S3 to S0.

The minimum value for C_{SS} can be found through the following equation:

$$C_{SS} > \frac{C_{VTTOUT} \cdot V_{DDQ}}{20 \cdot R_U}$$

NCH (Blocking N-FET Driver)

NCH is an open-drain output that controls the MOSFET that blocks backfeed from VDDQ to the 3V or 5V rail during S3 state. When the VDDQ PWM regulator is inhibited NCH will be held low.

If NCH is not actively utilized, it still must be tied to the 12V rail

PGOOD (Power Good)

Power Good is an open-drain logic output that changes to a logic low if any of the three regulators are out of regulation in S0 state. PGOOD will always be low in any state other than S0.

SLP_S5# (S5 Sleep Signal)

This is an input signalling the S5 state.

SLP_S3# (S3 Sleep Signal)

This is an input signalling the S3 state.

FB2

Connect the ouput of the external linear regulator to this pin through a properly sized resistor divider. The voltage at this pin is regulated to 0.8V. This pin is monitored for under- and over-voltage events.

DRIVE2

Connect this pin to the gate terminal of an external N-Channel MOSFET transistor. This pin provides the gate voltage for the linear regulator pass transistor. It also provides a means of compensating the error amplifier for applications requiring the transient response of the linear regulator to be optimized.

Functional Description

Overview

The ISL6532 contains complete control, drive, protection and ACPI compliance for powering DDR memory systems. It is designed for microprocessor computer applications with 5VATX, 12VATX, 5VSBY, and optionally 3.3VSBY from an ATX power supply. A 250kHz Sychronous Buck Regulator with a precision 0.8V reference provides the proper V_{DDQ} voltage to the DDR system. An internal LDO regulator with the ability to both sink and source current and an externally available buffered reference that tracks the V_{DDQ} output by 50% provides the V_{TT} termination voltage to the DDR system.

ACPI compliance is realized through the SLP_S3 and SLP_S5 sleep signals and through monitoring of the 12V ATX bus.

Initialization

The ISL6532 automatically initializes upon receipt of input power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input bias supply voltage. The POR monitors the bias voltage at the 5VSBY and P12V pins. The POR function initiates soft-start operation after the bias supply voltages exceed their POR thresholds.

State Transitions

Cold Start (Mechanical Start or S5 to S0 Transition)

At the onset of a mechanical start, the ISL6532 receives it's bias voltage from the 5V Standby bus (5VSBY). As soon as the SLP_S3 and SLP_S5 have transitioned HIGH, the ISL6532 starts an internal counter. Following a cold start or any subsequent S5 state, state transitions are ignored until the system enters S0/S1. None of the regulators will begin the soft start procedure until the 5V Standby bus has exceeded POR, the 12V bus has exceeded POR and V_{NCH} has exceeded the trip level.

Once all of these conditions are met, the PWM error amplifier will first be reset by internally shorting the COMP pin to the FB pin. This reset lasts for 2048 clock cycles, which is typically 8.2ms. The digital soft start sequence will then begin.

The PWM error amplifier reference input is clamped to a level proportional to the soft-start voltage. As the soft-start voltage slews up, the PWM comparator generates PHASE pulses of increasing width that charge the output capacitor(s). The internal V_{TT} LDO will also soft start through the reference that tracks the output of the PWM regulator. The soft start lasts for 2048 clock cycles, which is typically 8.2ms. This method provides a rapid and controlled output voltage rise.

Figure 2 shows the soft start sequence for a typical cold start. Due to the soft start capacitance, C_{SS}, on the

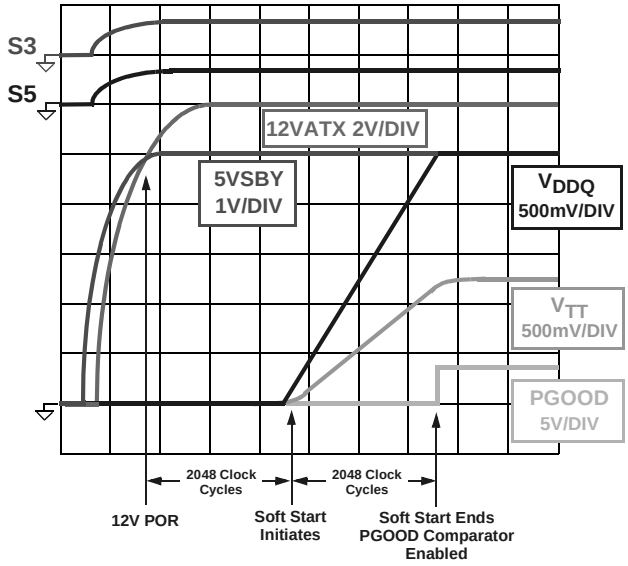


FIGURE 2. TYPICAL COLD START

VREF_IN pin, the S5 to S0 transition profile of the V_{TT} rail will have a more rounded features at the start and end of the soft start whereas the V_{DDQ} profile has distinct starting and ending points to the ramp up.

By directly monitoring 12VATX and the SLP_S3 and SLP_S5 signals the ISL6532 can achieve PGOOD status significantly faster than other devices that depend on Latched_Backfeed_Cut for timing.

Active to Sleep (S0 to S3 Transition)

When SLP_S3 goes LOW with SLP_S5 still HIGH, the ISL6532 will disable the V_{TT} linear regulator, enable the V_{DDQ} standby regulator and disable the V_{DDQ} switching regulator. NCH is pulled low to disable the backfeed blocking MOSFET. PGOOD will also transition LOW. When V_{TT} is disabled, the internal reference for the V_{TT} regulator is internally shorted to the V_{TT} rail. This allows the V_{TT} rail to float. When floating, the voltage on the V_{TT} rail will depend on the leakage characteristics of the memory and MCH I/O pins.

The V_{DDQ} rail will be supported in the S3 state through the standby V_{DDQ} LDO. When S3 transitions LOW, the Standby regulator is immediately enabled. The switching regulator is disabled synchronous to the switching waveform. The shut off time will range between 4 and 8us. The standby LDO is capable of supporting up to 450mA of load. The standby LDO receives it's input from either the 3.3V Standby rail or the 5V Standby rail through the P3V3SBY pin. It is recommended that the 3.3V Standby rail be used as the power dissipation will be minimized.

Sleep to Active (S3 to S0 Transition)

When SLP_S3 transitions from LOW to HIGH with SLP_S5 still HIGH and after the 12V rail exceeds POR, the ISL6532 will enable the V_{DDQ} switching regulator, disable the V_{DDQ} standby regulator, enable the V_{TT} LDO and force the NCH pin to a high impedance state turning on the blocking MOSFET. The internal short between the V_{TT} reference and the V_{TT} rail is released. Upon release of the short, the capacitor on VREF_IN is then charged up through the internal resistor divider network. The V_{TT} output will follow this capacitor charge up and acts as the S3 to S0 transition soft start for the V_{TT} rail. The PGOOD comparator is enabled only after 2048 clock cycles, or typically 8.2ms, have passed following the S3 transition to a HIGH state. Figure 3 illustrates a typical state transition from S3 to S0.

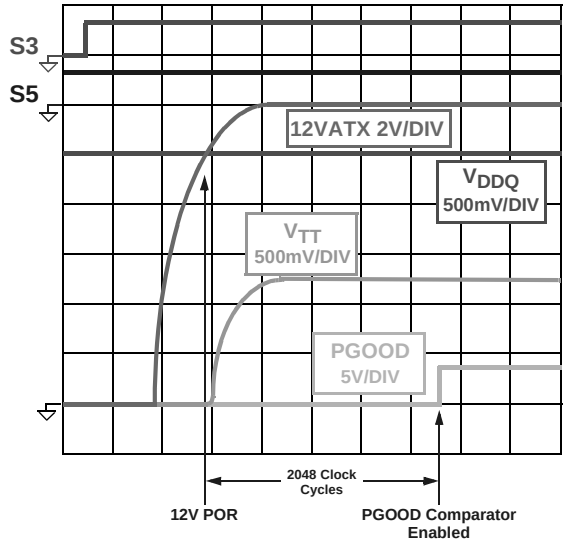


FIGURE 3. TYPICAL S3 to S0 STATE TRANSITION

Active to Shutdown (S0 to S5 Transition)

When the system transitions from active, S0, state to shutdown, S5, state, the ISL6532 IC disables all regulators and forces the PGOOD pin and the NCH pin LOW.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

Figure 4 shows the critical power components of the converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of a ground or power plane in a printed circuit board. The components shown in Figure 4 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O may each represent numerous physical capacitors. Locate the ISL6532 within 3 inches of the MOSFETs, Q_1 and Q_2. The circuit traces

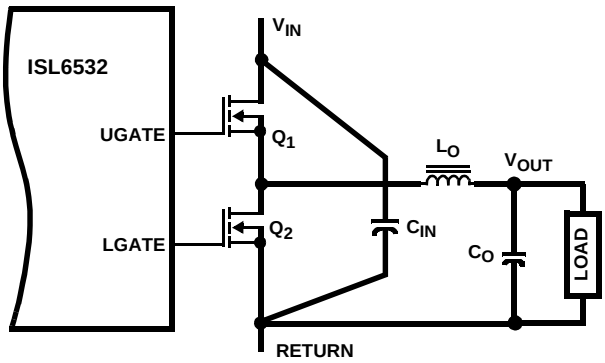


FIGURE 4. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

for the MOSFETs' gate and source connections from the ISL6532 must be sized to handle up to 1A peak current.

Feedback Compensation

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

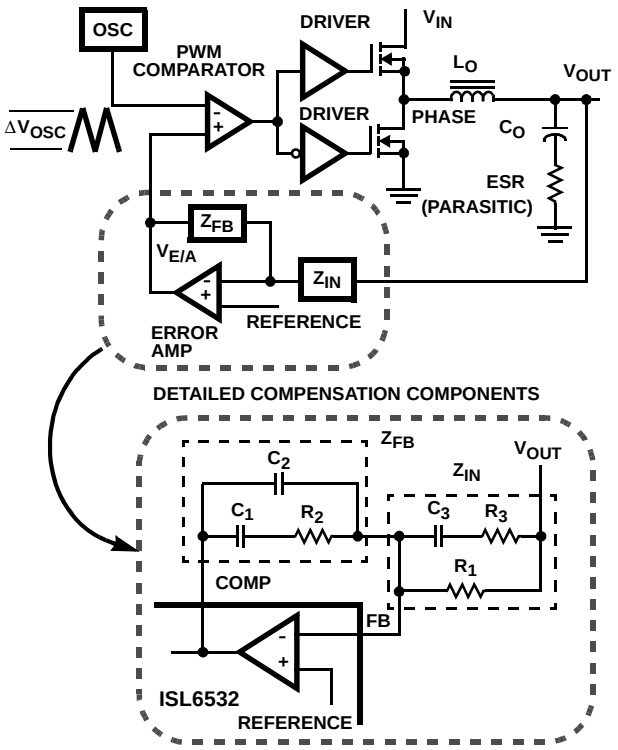


FIGURE 5. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier (internal to the ISL6532ISL6532) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 5. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for desired converter bandwidth.
2. Place 1^{ST} Zero Below Filter's Double Pole (~75% F_{LC}).
3. Place 2^{ND} Zero at Filter's Double Pole.
4. Place 1^{ST} Pole at the ESR Zero.
5. Place 2^{ND} Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

Figure 6 shows an asymptotic plot of the DC-DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 6. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

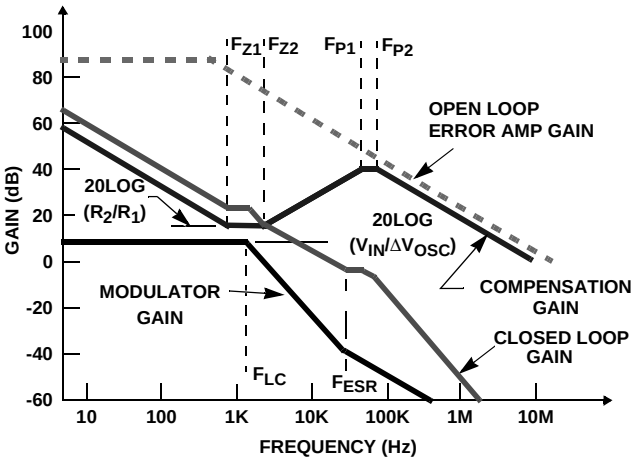


FIGURE 6. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

DDR memory systems are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6532 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of upper MOSFET and the source of lower MOSFET.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a

conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be closely approximated through the following equation:

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left({I_{OUT_{MAX}}}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_s} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \right)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection/Considerations

The ISL6532 requires 2 N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see the equations below). These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6532 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

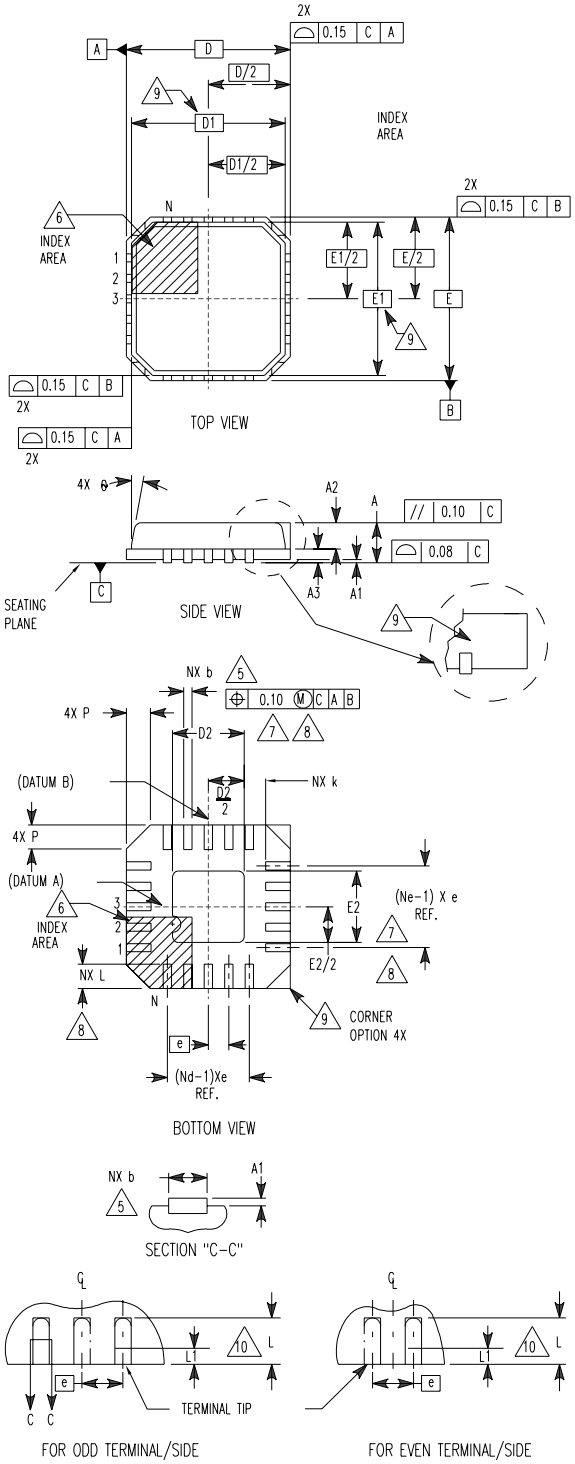
MOSFET Losses

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Where: D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the combined switch ON and OFF time, and
F_S is the switching frequency.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L28.6x6

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		28		2
Nd		7		3
Ne		7		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.