Gigabit Ethernet: 1.25 GBd 1300 nm Laser Transceiver in Low Cost 1 x 9 Package Style

Preliminary Technical Data

HFCT-5305

Features

- **Compliant with Proposed Specifications for IEEE-802-3 Gigabit Ethernet**
- **1300 nm Trenched BH Laser Source Technology**
- **Industry Standard 1 x 9 Package Style with Integral Duplex SC Connector**
- **Class 1 Laser Safety (Certification Pending)**
- **3 km Links in 8/125 μm SMF Cables**
- **550 m Links in 62.5/125 μm MMF Cables**
- **Single +5 V Power Supply Operation and PECL Logic Interfaces**
- **Wave Solder and Aqueous Wash Process Compatible**
- **Designed and Manufactured in an ISO 9000 Certified Facility**

Applications

- **Host to Host Interface**

Description

General Transmitter Section

The transmitter section consists of a 1300 nm Laser in an eye safe optical subassembly, (ELSA), which mates to the fiber cable. The ELSA is driven by a custom silicon bipolar IC which converts differential PECL logic signals, ECL referenced to a +5 V supply, into an analog Laser Diode drive current.

Eye Safety Design

The ELSA is designed to be eye safe under a single fault condition. To be eye-safe, only one of two results can occur in the event of a single fault. The transmitter must either maintain a safe level of output power or the transmitter should be disabled.

The ELSA contains a patented optical fiber stub which restricts the level of light emerging from the connector port under all conditions. Overdriving the laser (even to destruction) cannot produce enough light to violate the IEC safe level. As a result the HFCT-5305 is intrinsically eye safe.

Receiver Section

The receiver includes an InP PIN photodiode mounted together with a custom silicon bipolar transimpedance preamplifier IC in an optical subassembly, OSA. This OSA is mated to a custom silicon bipolar circuit providing post-amplification and quantization.

The custom silicon bipolar circuit also includes a Signal Detect circuit which provides a PECL logic high output upon detection of a usable input optical signal level. This single-ended low-power PECL output is designed to drive a standard PECL input

through a 10 Ω load instead of the normal 50 Ω ECL load.

Regulatory Compliance

See the Regulatory Compliance Table for the targeted typical and measured performance for these transceivers. As the product design is completed, full characterization testing will be done to determine the actual performance of the final design.

The overall equipment design will determine the level it is able to be certified to. These transceiver performance targets are offered as a figure of merit to assist the designer in considering their use in equipment designs.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The targeted performance has been shown to provide adequate performance typical industry production environments.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever system level ESD test criteria that the equipment is intended to meet. The targeted performance is more robust than typical industry equipment practices today.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

These transceivers, with their shielded design, are targeted to perform to the limits listed to assist the designer in the management of the overall equipment EMI performance.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments.

Regulatory Compliance

Feature	Test Method	Targeted Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 1 (>500 V)
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 801-2	Products of this type will typically withstand at least 25 kV without damage when the Duplex SC Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class A CENELEC EN55022 Class A (CISPR 22A) VCCI Class I	Typically provide a TBD dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 3 V/m field swept from 10 to 450 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	FDA CDRH 21-CFR 1040 Class 1 IEC 825 Issue 1 1993: 11 Class 1 CENELEC EN60825 Class 1	Compliant per Hewlett-Packard Testing for all three requirements under normal operating conditions. Fault condition testing pending completion of product development.

These transceivers have an immunity to such fields due to their shielded design.

Eye Safety

These 1300 nm Laser-based transceivers are intended to provide Class 1 eye safety by design. Hewlett-Packard has tested the current transceiver design for compliance with the requirements listed below under normal operating conditions and will test for compliance under fault conditions when the product design is completed. HP will obtain certification from outside sources for eye safety.

This performance will enable the transceivers to be used without concern for eye safety in the same way that LED-based transceivers are used today.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	–40		+100	°C	
Ambient Operating Temperature	T_A	–10		+80	°C	
Supply Voltage	V_{CC}	–0.5		7	V	
Data Input Voltage	V_I	–0.5		V_{CC}	V	
Transmitter Differential Input Voltage	V_D	See Table Below		1.4	V	1

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		+70	°C	
Relative Humidity	RH	5		95	%	
Supply Voltage	V_{CC}	4.75		5.25	V	
Power Supply Ripple				TBD	Hz/V_{pp}	
Power Supply Rejection				TBD	Hz/V_{pp}	
Transmitter Data Input Voltage - Low	V_{IL}-V_{CC}	–1.810		–1.475	V	2
Transmitter Data Input Voltage - High	V_{IH}-V_{CC}	–1.165		–0.880	V	2
Transmitter Differential Input Voltage	V_D	0.3		See Table Above	V	
Data Output Load	R_{DL}	50			Ω	3
Signal Detect Output Load	R_{SDL}	7	10		Ω	4
Conducted Noise on Data and Signal Detect Outputs			TBD		Hz/V_{pp}	

Process Compatibility

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Hand Lead Soldering Temperature/Time	T_{SOLD}/t_{SOLD}			+270/10	°C/sec.	
Wave Soldering and Aqueous Wash	T_{SOLD}/t_{SOLD}			+270/10	°C/sec.	

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs without damaging the ESD protection circuit.
2. Compatible with 10 K, 10 KH and 100 K ECL and PECL signals.
3. The outputs are terminated to V_{CC} - 2 V.
4. The outputs are terminated to ground.

Transmitter Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCT}		65	130	mA	5
Power Dissipation	P_{DIST}		0.35	0.68	W	
Data Input Current – Low	I_{IL}	–350	0		µA	
Data Input Current – High	I_{IH}		16	350	µA	

Receiver Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCR}		100	120	mA	
Power Dissipation	P_{DISR}		0.4	0.5	W	6
Data Output Voltage – Low	$V_{OL} – V_{CC}$	–1.950		–1.620	V	7
Data Output Voltage – High	$V_{OH} – V_{CC}$	–1.045		–0.740	V	7
Data Output Rise Time	t_r	0.2	0.3	0.51	ns	8
Data Output Fall Time	t_f	0.2	0.3	0.51	ns	8
Signal Detect Output Voltage – Low	$V_{OL} – V_{CC}$	–1.840		–1.620	V	7
Signal Detect Output Voltage – High	$V_{OH} – V_{CC}$	–1.045		–0.880	V	7
Signal Detect Assert Time (Off to On)	t_{SDA}			TBD	µs	9
Signal Detect Assert Time (On to Off)	t_{SDD}			TBD	µs	10

Notes:

5. The typical value is at +70°C; maximum value is an end of life value.
6. Power dissipation value is the power dissipated in the receiver itself. It is calculated as the sum of the products of V_{CC} and I_{CC} minus the sum of the products of the output voltages and currents.
7. These outputs are compatible with 10 K, 10 KH and 100 K ECL and PECL inputs.
8. These values are under review and may be replaced by an eye mask test.
9. The Signal Detect output will change from logic “0” to “1” within TBD us of a step transition in optical input power from no light to –18 dBm.
10. The Signal Detect output will change from logic “1” to “0” within TBD us of a step transition in optical input power from –16 dBm to no light.

Transmitter Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 fiber	P_O	–13		–3	dBm avg.	
Optical Extinction Ratio		9			dB	
Center Wavelength	λC	1270		1355	nm	
Spectral Width – rms	σ			4	nm rms	
RIN_{12}				–116	dB/Hz	

Receiver Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum	P_{IN}	–3		–20	dBm avg.	11
Return Loss		12			dB	
Signal Detect – Asserted	P_A	P_D + 1.5 dB			dBm avg.	
Signal Detect – Deasserted	P_D	–45			dBm avg.	
Signal Detect – Hysteresis	$P_A – P_D$	1.5			dB	

Note:

11. The sensitivity is provided at a BER of 1×10^{-12}.

Table 1. Pinout Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board, they are embedded in the nonconductive plastic housing and are not tied to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
2	RD+	Receiver Data Out See recommended circuit schematic.
3	RD–	Receiver Data Out Bar See recommended circuit schematic.
4	SD	Signal Detect Normal optical input levels to the receiver result in a logic “1” output. Low optical input levels to the receiver result in a fault condition indication shown by a logic “0” output. Signal Detect is a single-ended, low-power, PECL output. Since SD is a low-power PECL output, complete the interconnection of SD output with other PECL inputs using a 10 kΩ pull-down resistor to V_{EE} to allow biasing of this interconnection. Do not load this SD output with standard PECL, 50 Ω to V_{CC} – 2 V, termination. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	V_{CCR}	Receiver Power Supply Provide +5 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply Provide +5 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	TD–	Transmitter Data In Bar See recommended circuit schematic.
8	TD+	Transmitter Data In See recommended circuit schematic.
9	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.

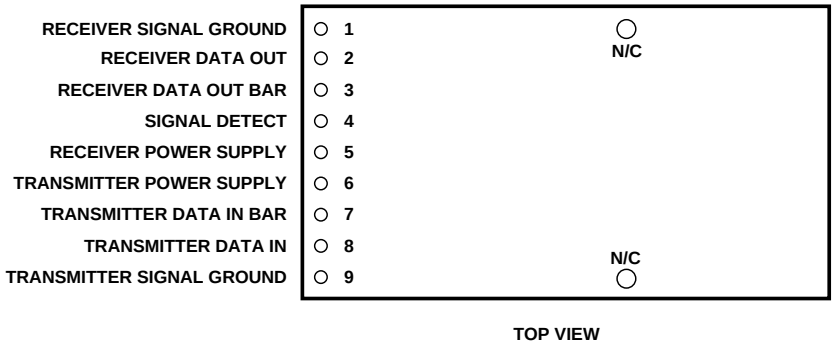
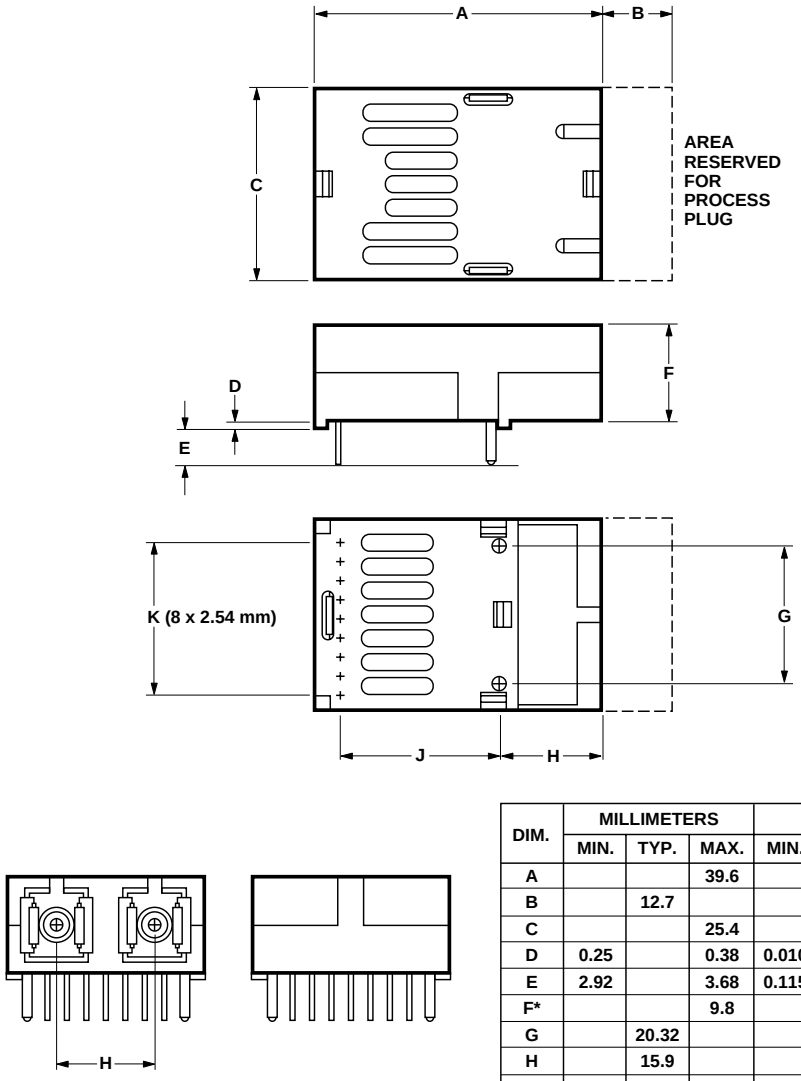


Figure 1. Pinout.



DIM.	MILLIMETERS			INCHES		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			39.6			1.559
B		12.7			0.500	
C			25.4			1.000
D	0.25		0.38	0.010		0.015
E	2.92		3.68	0.115		0.145
F*			9.8			0.386
G		20.32			0.800	
H		15.9			0.626	
J		20.32			0.800	
K		20.32			0.800	

*PRE-RELEASE SAMPLES MAY HAVE HEIGHT UP TO 10.35 mm (0.407 INCHES).

Figure 2. Package Outline Drawing and Pinout.

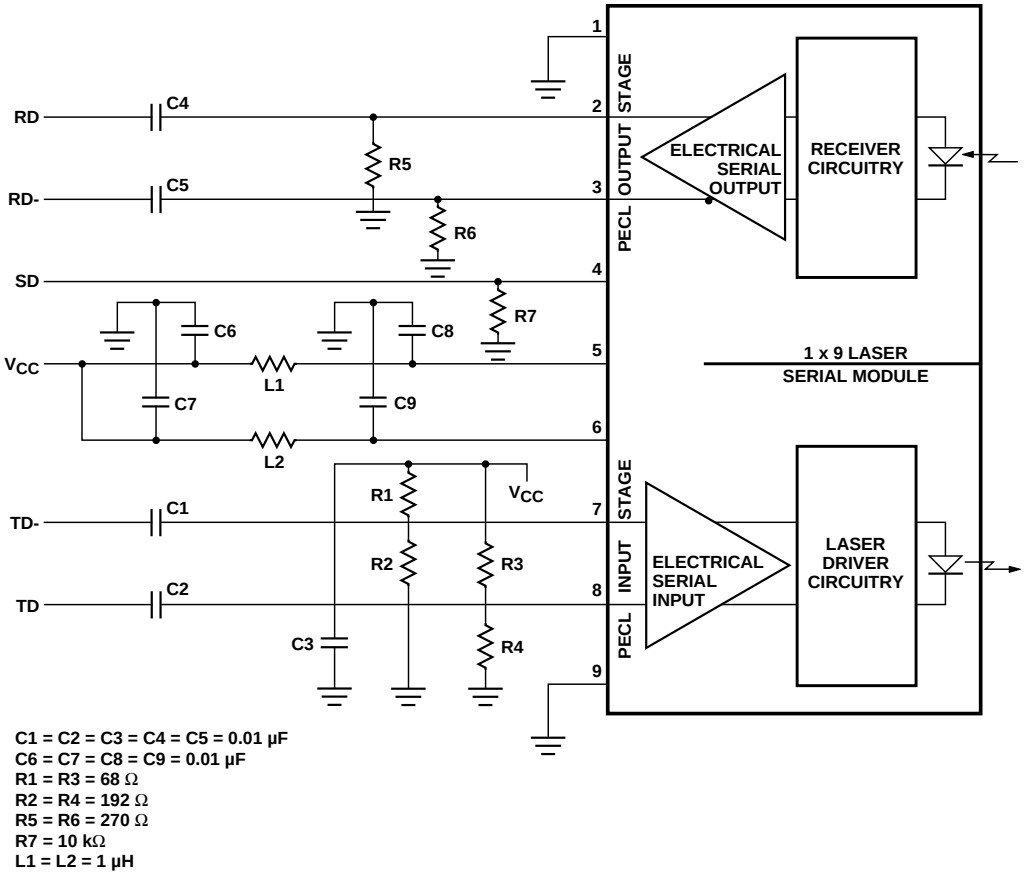
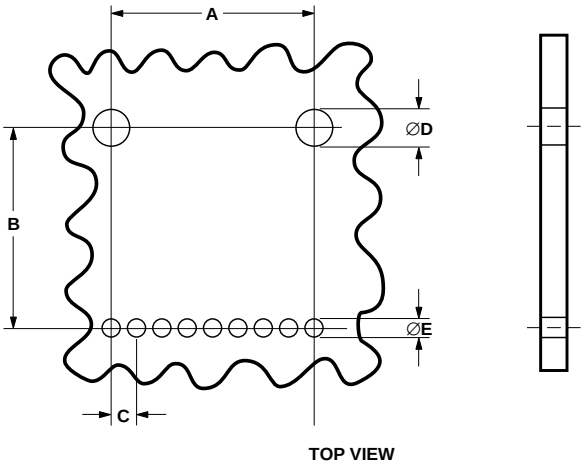


Figure 3. Recommended Circuit Schematic.



DIM.	MILLIMETERS			INCHES		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	–	20.32	–	–	0.800	–
B	–	20.32	–	–	0.800	–
C	–	2.54	–	–	0.100	–
∅D	1.8	–	2.0	0.071	–	0.079
∅E	0.7	–	0.9	0.028	–	0.036

Figure 4. Recommended Board Layout Hole Pattern.