

Advance Information

Two-Channel Distributed System Interface (DSI) Physical Interface Device

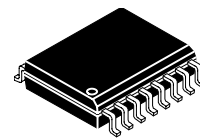
The 33790 is a two-channel physical layer interface IC for the Distributed System Interface (DSI) bus. It is designed to meet automotive requirements. It can also be used in nonautomotive applications. It supports bidirectional communication between slave and master ICs. Some slave devices derive a regulated 5.0 V from the bus, which can be used to power sensors, thereby eliminating the need for additional circuitry and wiring.

Features

- Two Independent DSI Compatible Busses
- Pinout Matched to MC68HC55 (SPI to DSI Logic)
- Wave-Shaped Bus Output Voltage
- Independent Thermal Shutdown and Current Limit
- Return Signalling Current Detection
- Internal Logic Input Pull-Ups and Pull-Downs
- On-Board Charge Pump
- 2 kV ESD Capability
- Communications Rate Up to 150 kbps

33790

TWO-CHANNEL DISTRIBUTED SYSTEM INTERFACE (DSI) PHYSICAL INTERFACE DEVICE

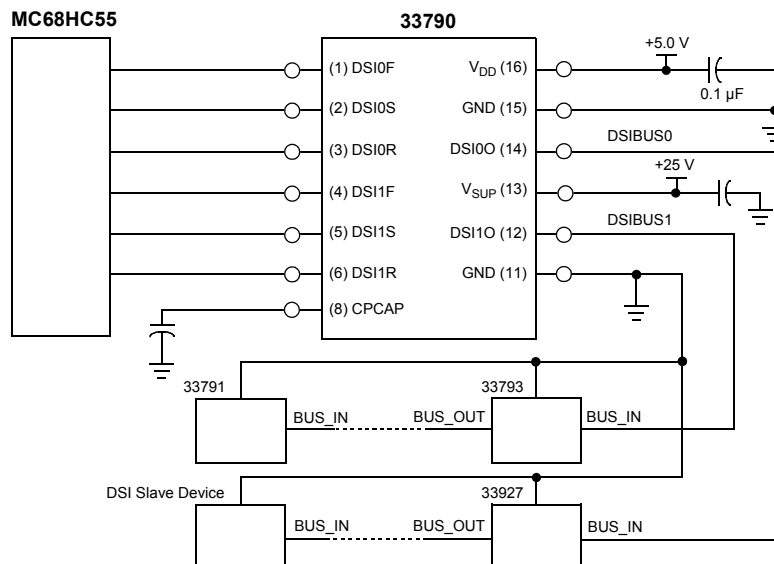


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(16-LEAD SOICW)

ORDERING INFORMATION

| Device | Temperature Range (T _A) | Package |
|-----------|-------------------------------------|---------|
| MC33790DW | -40 to +85°C | SO-16W |

33790 Simplified Application Diagram



This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

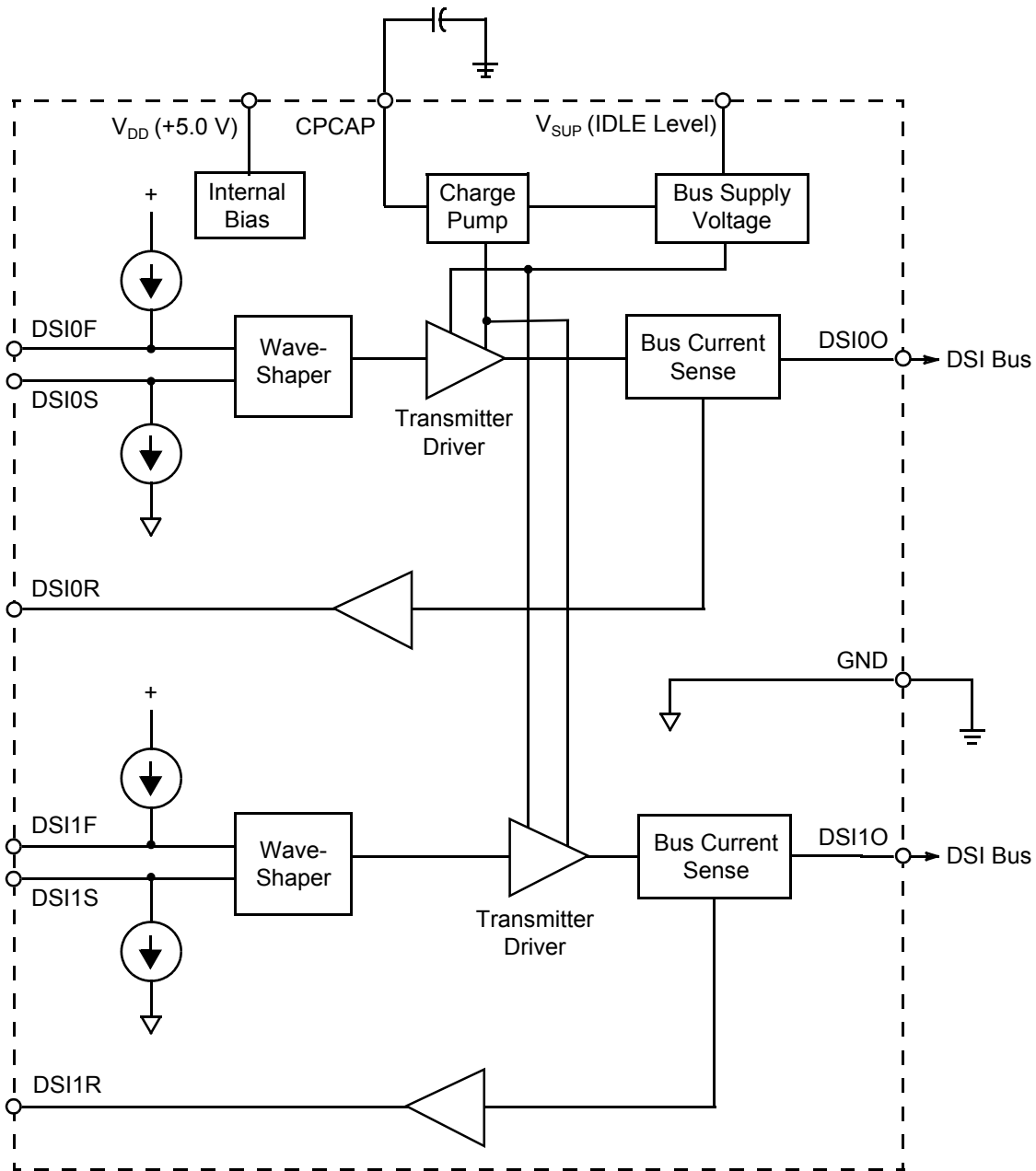
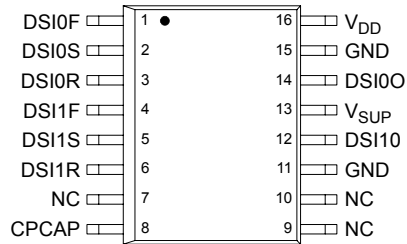


Figure 1. 33790 Simplified Block Diagram



PIN FUNCTION DESCRIPTION

| Pin | Pin Name | Description |
|-----|------------------|---|
| 1 | DSI0F | This logic input controls the frame output for DSI channel 0 in accordance with Table 1, page 8. |
| 2 | DSI0S | This logic input controls the signalling output for DSI channel 0 in accordance with Table 1, page 8. |
| 3 | DSI0R | This logic output provides the return data for DSI channel 0 in accordance with Table 1, page 8. |
| 4 | DSI1F | This logic input controls the frame output for DSI channel 1 in accordance with Table 1, page 8. |
| 5 | DSI1S | This logic input controls the signalling output for DSI channel 1 in accordance with Table 1, page 8. |
| 6 | DSI1R | This logic output provides the return data for DSI channel 1 in accordance with Table 1, page 8. |
| 7 | NC | Unused. |
| 8 | CPCAP | Charge pump capacitor. Used to store and filter charge pump output. |
| 9 | NC | Unused. |
| 10 | NC | Unused. |
| 11 | GND | Circuit and bus ground return. |
| 12 | DSI10 | DSI bus 1 input/output. |
| 13 | V _{SUP} | Idle level supply input. The voltage supplied to this pin sets the idle level on the DSI bus. |
| 14 | DSI00 | DSI bus 0 input/output. |
| 15 | GND | Circuit and bus ground return. |
| 16 | V _{DD} | 5.0 V logic supply input. |

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

| Rating | Symbol | Value | Unit |
|---|---|--|------|
| Supply Voltage Continuous Load Dump - $t < 300$ ms | V_{SUP} $V_{SUP(t)}$ | -0.5 to 25 40 | V |
| Maximum Voltage on Input/Output Pins | V_{DD} DSIxS, DSIxF (Note 1) DSIxO (Note 1) | -0.3 to 5.5 -0.3 to $V_{DD}+0.3$ -0.3 to $V_{SUP}+0.3$ | V |
| Operating Temperature | T_A | -40 to +85 | °C |
| Storage Temperature | T_{stg} | -55 to +150 | °C |
| Operating Junction Temperature | T_J | -40 to +150 | °C |
| Lead Temperature (IR Reflow Soldering for >60 s @ >183°C), 10 s @ >215°C | T_{solder} | 230 | °C |
| Continuous Current per Pin | V_{DD} DSIxR V_{SUP} | 0 to 10 -2.5 to 5.0 500 | mA |
| Thermal Resistance Junction to Ambient | $R_{\theta J-A}$ | 45 | °C/W |
| Thermal Shutdown | T_{SD} | 155 to 190 | °C |
| ESD Voltage (All Pins) Human Body Model (Note 2) Machine Model (Note 3) | V_{ESD1} V_{ESD2} | ± 2000 ± 200 | V |

Notes

1. $R=0 \Omega$.
2. ESD1 performed in accordance with the Human Body Model ($C_{ZAP}=100$ pF, $R_{ZAP}=1500 \Omega$).
3. ESD2 performed in accordance with the Machine Model ($C_{ZAP}=200$ pF, $R_{ZAP}=0 \Omega$).

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$, $8.0\text{ V} \leq V_{SUP} \leq 25.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

SUPPLY

| | | | | | |
|--|--------------------------|--------|----------|--------------|----|
| I_{SUP} Supply Current/Channel (not including I_{OUT}) DSIx0 = Idle Voltage, $-100\text{ mA} < I_{OUT} < 0\text{ mA}$ DSIx0 = Output High Voltage, $I_{OUT} = 12\text{ mA}$ | I_{SUPI} I_{SUPH} | – – | – 5.0 | 3.25 9.00 | mA |
| I_{DD} Supply Current/Channel | I_{DD} | – | – | 1.0 | mA |

BUS TRANSMITTER

| | | | | | |
|---|--------------|-------|-----|-------|---------------|
| V_{SUP} to DSIXO on Resistance (During Idle) $I_{OUT} = -100\text{ mA}$ | $R_{DS(on)}$ | – | – | 10 | Ω |
| Output High Voltage DSIx0 ($-15\text{ mA} \leq I_{OUT} \leq 1.0\text{ mA}$) | $DSIV_{OH}$ | 4.175 | 4.5 | 4.825 | V |
| Output Low Voltage DSIx0 ($-15\text{ mA} \leq I_{OUT} \leq 1.0\text{ mA}$) | $DSIV_{OL}$ | 1.325 | 1.5 | 1.675 | V |
| Output High-Side Current Limit (Note 4) | I_{CLH} | -100 | – | -200 | mA |
| Output Low-Side Current Limit (Note 4) | I_{CLL} | 110 | – | 220 | mA |
| Input Leakage DSIx0 when DSIXF is high and DSIXS is low ($0\text{ V} \leq DSIXO \leq \min(V_{SUP} = 16.5\text{ V})$) | DSI_{IB} | -200 | – | 50 | μA |

BUS RECEIVER

| | | | | | |
|--------------------------|----------|------|------|------|----|
| Return Current Threshold | I_{RH} | -5.0 | -6.0 | -7.0 | mA |
|--------------------------|----------|------|------|------|----|

MICROCONTROLLER INTERFACE

| | | | | | |
|--|-----------|--------------------|---|--------------------|---------------|
| Logic Input Thresholds DSIXS, DSIXF | V_{ITH} | 1.10 | – | 2.20 | V |
| Output High Voltage DSIXR Pin = -0.5 mA | V_{OH} | $0.8 \cdot V_{DD}$ | – | V_{DD} | V |
| Output Low Voltage DSIXR Pin = 1.0 mA | V_{OL} | 0.0 | – | $0.2 \cdot V_{DD}$ | V |
| Internal Pull-Up for DSIXF | I_{IL} | -100 | – | -10 | μA |
| Internal Pull-Down for DSIXS | I_{IH} | 10 | – | 100 | μA |

Notes

- After 10 μs settling time (assured by design).

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$, $8.0\text{ V} \leq V_{SUP} \leq 25.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

MICROCONTROLLER INTERFACE

| | | | | | |
|--|------------|---------------|-----------|---------------|---------------|
| Microcontroller Signal Cycle Time | t_{cyc} | 6.6 | – | 1000 | μs |
| Microcontroller Signal Low Time | t_{cycL} | 2.0 | – | 667 | μs |
| Microcontroller Signal High Time | t_{cycH} | 2.0 | – | 667 | μs |
| Microcontroller Signal Duty Cycle for Logic Zero | DC_{Lo} | 30 | 33 | 36 | % |
| Microcontroller Signal Duty Cycle for Logic One | DC_{Hi} | 60.0 | 66.7 | 72.0 | % |
| Microcontroller Signal Slew Time (Note 5) | t_{slew} | – | – | 500 | ns |
| Frame Start to Signal Delay Time | t_{DLY1} | $t_{cyc}-0.1$ | t_{cyc} | $t_{cyc}+0.1$ | μs |
| Signal End to Frame End Delay Time | t_{DLY2} | 1 | – | – | μs |
| Rise Time (Note 5) | t_{RISE} | 0 | – | 100 | ns |
| Fall Time (Note 5) | t_{FALL} | 0 | – | 100 | ns |

BUS TRANSMITTER

| | | | | | |
|---|--------------------|------|-----|------|------------------------|
| Idle to Frame and Frame to Idle Slew Rate $C \leq 5.0\text{ nF}$ | $t_{slew(FRAME)}$ | – | 6.0 | 10.0 | $\text{V}/\mu\text{s}$ |
| Signal High to Low and Signal Low to High Slew Rate $C \leq 5.0\text{ nF}$ | $t_{slew(SIGNAL)}$ | 3.0 | 4.5 | 8.0 | $\text{V}/\mu\text{s}$ |
| Data Valid ($V_{SUPx} = 25\text{ V}$, $C_L \leq 5.0\text{ nF}$) | | | | | μs |
| DSIxF, Vin(th) to DSIxO = 5.5 V | t_{DVLD1} | 2.44 | – | 6.90 | |
| DSIxS, Vin(th) to DSIxO = 2.0 V | t_{DVLD2} | 0.25 | – | 1.63 | |
| DSIxS, Vin(th) to DSIxO = 4.0 V | t_{DVLD3} | 0.25 | – | 1.63 | |

Notes

- Slew times and rise and fall times between 10% and 90% of output high and low levels.

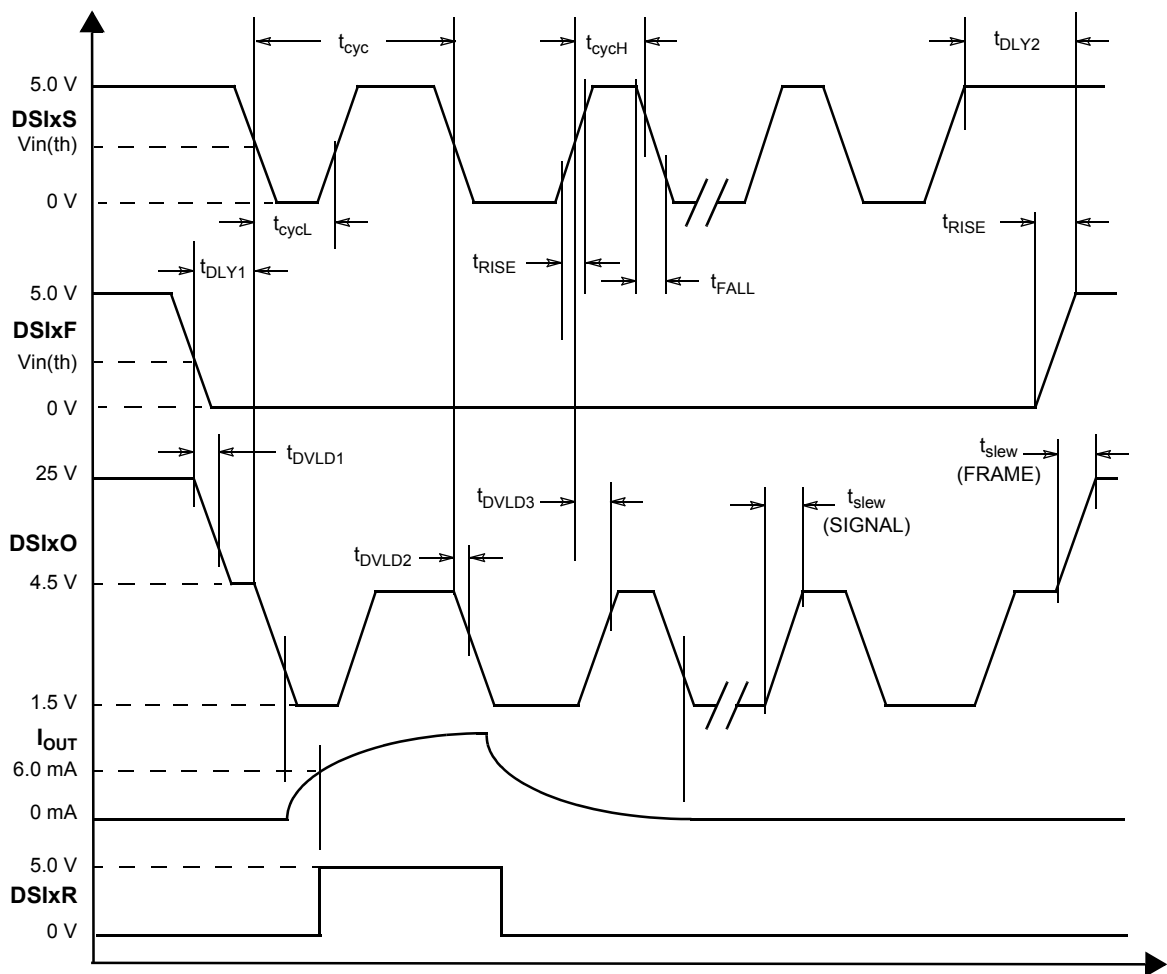


Figure 2. Timing Characteristics

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33790 is designed to provide the interface between logic and the DSI bus. It accepts signals with a typical 0-to-5.0 V logic level to control the state of the bus output (Idle Level, Logic High Level, Logic Low Level, and High Impedance). It detects the current drawn from the bus output during signaling and outputs a 0-to-5.0 V logic level corresponding to the bus current being

above (Logic 1 out) the bus return logic 1 current or below (Logic 0 out). The 33790 contains current limiting of the bus outputs as required by the DSI Bus specification and thermal shutdown to protect itself from damage. Two independent DSI bus outputs are provided by the IC.

FUNCTIONAL DESCRIPTION

Bus Driver and Receiver

The Wave-Shaper converts the 0-to-5.0 V logic inputs from DS_{ix}F (frame) and DS_{ix}S (signal) to a wave-shaped signal on the DS_{ix}O output, as shown in the timing diagrams in Figure 2 and the truth table in Table 1. The Bus Current Sense detects the current being drawn by the device(s) on the bus during signalling (DS_{ix}F=0). If the current is above a set level, DS_{ix}R will be high; otherwise, it is low.

Table 1. DSI Bus Truth Table

| DS _{ix} F | DS _{ix} S | T _{LIM} | DS _{ix} R | DS _{ix} O |
|--------------------|--------------------|------------------|--------------------|---------------------------------|
| 0 | 0 | 0 | Return Data | Low (1.5 V) |
| 0 | 1 | 0 | Return Data | High (4.5 V) |
| 1 | 0 | 0 | 0 | High Impedance |
| 1 | 1 | 0 | 0 | Idle ≥ V _{SUP} - 0.5 V |
| X | X | 1 | 1 | High Impedance |

The current for the idle state is from the supply connected to V_{SUP} and this supply should not be current limited below 250 mA per channel. During idle state, the voltage on the DSI bus will be very close to the V_{SUP} voltage.

Internal thermal shutdown circuitry and current limit individually protect the DS_{ix}O outputs from shorts to battery and ground.

Typically, the thermal shutdown occurs between 160°C and 170°C. If the junction temperature rises above this temperature, the output drivers for DS_{ix}O are disabled by the thermal shutdown circuitry. The output drivers remain off until the junction temperature decreases below approximately 155°C, at which time the thermal shutdown circuitry turns off and the outputs are re-enabled. Each DS_{ix}O output has a unique thermal sense and shutdown circuit, so a short on one channel does not affect the other channel.

Charge Pump

The charge pump uses on-board capacitors to step the input voltage up to the voltage needed to drive the on-board transmitter FETs. A filter/storage capacitor is connected to CPCAP to hold the stepped-up voltage.

Input Pull-Ups and Pull-Downs

Internal current pull-ups are used on the DS_{ix}F pins and pull-downs on the DS_{ix}S pins. If these pins are left unconnected, their associated DSI bus will go to the unused (high impedance) state.

APPLICATIONS

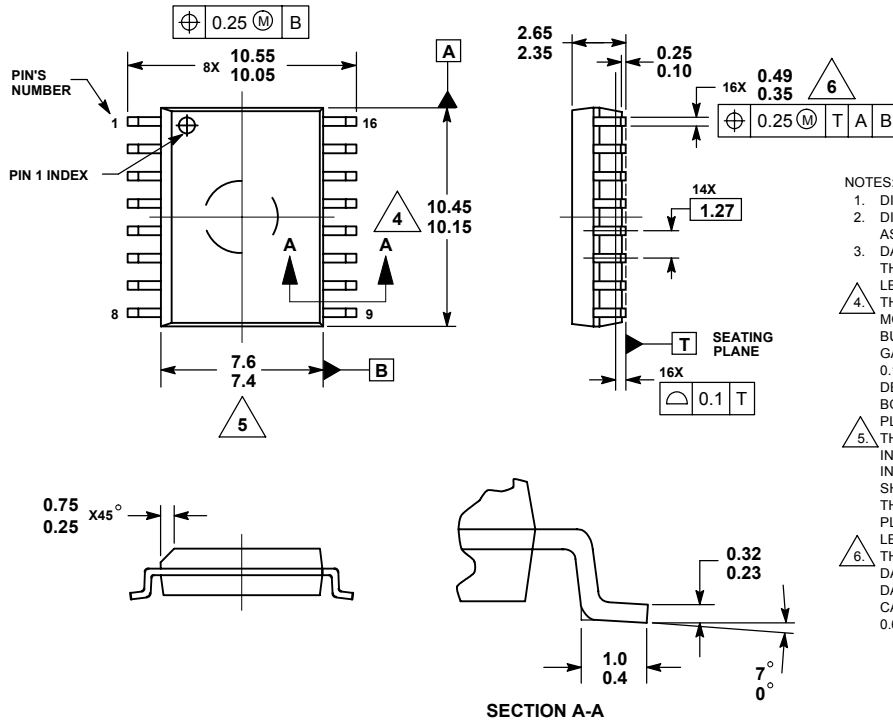
The 33790 is intended for use in a DSI system. This device supplies the interface between standard logic levels and the voltage and current required for the DSI bus. Two independent DSI busses are supported by this part. The 33790 does not form the timing for the DSI bus. This is done by logic either embedded in a microcontroller or by the MC68HC55, which uses SPI commands and forms DSI protocol for communications over the DSI bus.

The pins from the MC68HC55 are made to line up with the pins connecting to the 33790. This includes all the DS_{ix}F, DS_{ix}S, and DS_{ix}R pins.

A capacitor attached to CPCAP serves as a charge reservoir for the gate drive charge pump. This circuit creates a voltage that is higher than the source of the n-channel output transistor. This allows turning on of the transistor enough to prevent any significant voltage drop across it. The rest of charge pump electronics are completely self-contained on the IC.

PACKAGE DIMENSIONS

DW SUFFIX
 (16-LEAD SOIC WIDE BODY)
 PLASTIC PACKAGE
 CASE 751G-04
 ISSUE D



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
 4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
 5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
 6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62mm.

NOTES

NOTES

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1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1 Minami-Azabu. Minato-ku, Tokyo 106-8573 Japan.

81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tao Po, N.T.,

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