Ordering number : EN2967

CMOS LSI

SANYO No.2967

LC86104A

Liquid Crystal Display Controller/ Driver, On-chip 4K bytes ROM and On-chip 168 bytes RAM

8-BIT SINGLE CHIP MICROCOMPUTER LC86104A

The LC86104A microcomputer is an 8-bit single chip microcomputer with the following On-chip functional blocks:
- CPU: Operable at a minimum cycle time of 1 microsecond.
- On-chip ROM: Capacity = 4K bytes
- On-chip RAM: Capacity = 168 bytes
- Dot matrix Liquid Crystal automatic display controller/driver
- Two 16-bit timers/counters
- Seven-source 5-level vectored interrupt system

All of the above functions are fabricated on a single chip.

General purpose applications:
(1) Data bank control
(2) Remote controlling for VCR, Tuner, and the like.
(3) Controlling for CD, Tuner, and the like.
(4) Controlling for small-sized measuring instruments

Features:
(1) Read-Only Memory (ROM): 4096 x 8 bits
(2) Random Access Memory (RAM): 168 bytes, 128 x 8 bits for computation (general purpose RAM) and 40 x 8 bits for data display (display RAM)
(3) Cycle time: Cycle time varies depending on system clock sources. The selectable system clock sources are shown in the table below.

Cycle time	System clock source	Oscillation frequency	Operating voltage range	Remarks
1 μS	Ceramic(CF) oscillation specification	12MHz	4.5～6.0V	
4 μS	Ceramic(CF) oscillation specification	3MHz	2.5～6.0V	
15 μS	RC (Resistor and Capacitor) oscillation specification	800KHz	2.5～6.0V	
366 μS	Crystal (X'tal) oscillation specification	32KHz	2.5～6.0V	

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(4) Current dissipation
a. Basic system operation mode

Current dissipation	System clock source	Oscillation frequency	Operating voltage range	Remarks
9.5mA TYP	Ceramic(CF) oscillation specification	12MHz	5.0V	Display segments OFF
1.4mA TYP	Ceramic(CF) oscillation specification	3MHz	2.9V	Display segments OFF
390μA TYP	RC (Resistor and Capacitor) oscillation specification	800KHz	2.9V	Display segments OFF
15μA TYP	Crystal (X'tal) oscillation specification	32KHz	2.9V	Display segments OFF and CF/RC oscillation in idle state

b. HALT operation mode

Current dissipation	System clock source	Oscillation frequency	Operating voltage range	Remarks
3mA TYP	Ceramic(CF) oscillation specification	12MHz	5.0V	Display segments OFF
440μA TYP	Ceramic(CF) oscillation specification	3MHz	2.9V	Display segments OFF
150μA TYP	RC (Resistor and Capacitor) oscillation specification	800KHz	2.9V	Display segments OFF
5μA TYP	Crystal (X'tal) oscillation specification	32KHz	2.9V	Display segments OFF and CF/RC oscillation in idle state

(5) Ports
- Input/output ports: 5 ports (37 port pins)
  Input/output port software programmable in 8-bit unit: 1 port (8 port pins)
  Input/output port software programmable in single-bit unit: 4 ports (29 port pins)

(6) Liquid Crystal Display Drivers
- Common driver pins: 8
- Segment driver pins: 40 (Extendable to 200 segments with LC7930 x 4)
- Display signal duty mode: Static duty cycle to 1/8 duty cycle
- Display biasing mode: Static bias to 1/5 bias

(7) On-chip character generator ROM
- ROM capacity: 5600 bits
- Character font: 5 x 7 dots (Max.)
- Number of characters: 160

(8) Liquid Crystal Display control instruction
- Cursor display ON/OFF/blinking
- Display character blinking
- Display ON/OFF

(9) Timer
- Two 16-bit timers/counters software programmable
  Mode 0: 13-bit timers/counters
  Mode 1: 16-bit timers/counters
  Mode 2: 8-bit automatic reloadable timers/counters

(10) Interrupt mechanism:
- 7 sources and 5 vectored interrupts:
  External interrupt $\overline{\text{INT0}}$
  External interrupt $\overline{\text{INT1}}$
  Timer/counter interrupt T0
  Timer/counter interrupt T1, and
  Divider/port 1/port 3 interrupt

(11) Stack levels
- 128 levels (Max.): Stack area included in the RAM area

(12) Two oscillation circuits
- One for CF or RC oscillation: Generate the system clocks and Liquid Crystal Display clocks. Note that the CF oscillation or the RC oscillation can be selected by the mask option.
- One for X'tal oscillation: Generate time base clock, Liquid Crystal Display clocks and the system clocks.

(13) Liquid Crystal Display display data transfer rates
- 2/Fcf, 4/Fcf, 8/Fcf --- 256/Fcf
  2/Fxt, 4/Fxt, 8/Fxt --- 256/Fxt

One of the display data transfer rates can be selected by the mask option.

Note: The Fcf indicates the oscillation frequency output by the CF oscillation circuit or the RC oscillation circuit.

Note: The Fxt indicates the oscillation frequency output by the crystal (X'tal) oscillation circuit.

Note: The frame frequency Ffrm for Liquid Crystal display can be gained in the following manner:
Ffrm = 1/(display data transfer rate x total display dot number)

(14) Standby function
- HALT mode function
  The HALT mode is used to reduce power dissipation. In this operation mode, program execution is stopped. This operation mode can be released by interrupt request signals or the initial system reset request signal.
- HOLD mode function
  The HOLD mode is used to freeze both of the CF/RC oscillation and crystal (X'tal) oscillation. It can be released by the system reset request signal or the "L" level input signal to the external interrupt pin ($\overline{\text{INT0}}$).
  Program execution is started again after the HOLD mode is released by the input signal to the $\overline{\text{INT0}}$ pin. However, in this release operation, it should be kept in mind that program execution may enter abnormal state due to unstable oscillation.
  In order to prevent it, you can set a desired data in timer/counter 0 to generate a wait time period. The oscillation will become stable for this wait time period.

(15) Factory shipment
- Chip delivery form
- QIP 100 delivery form

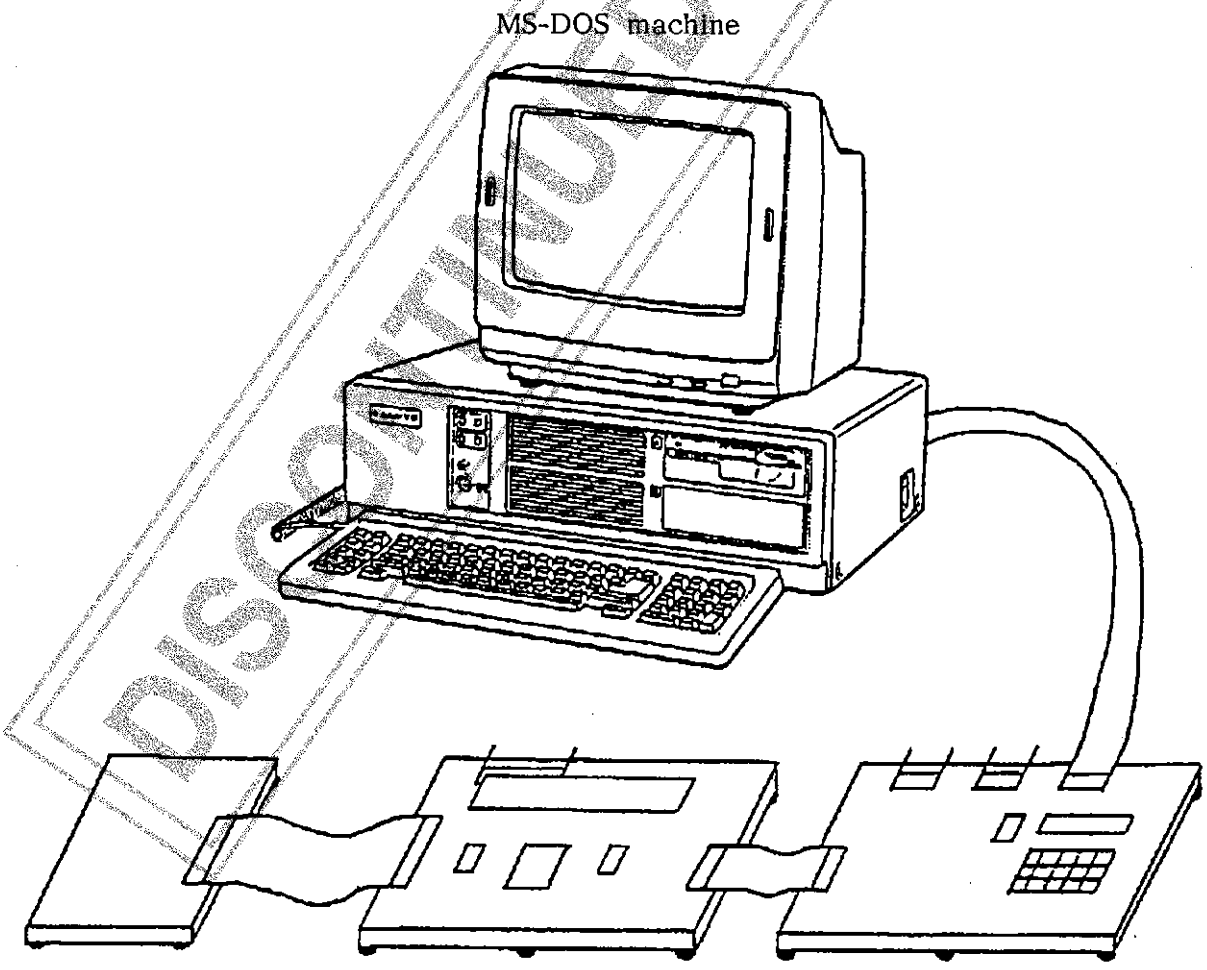
Development Support system

The development support system for the LC86104A applications consists of the following support tools:

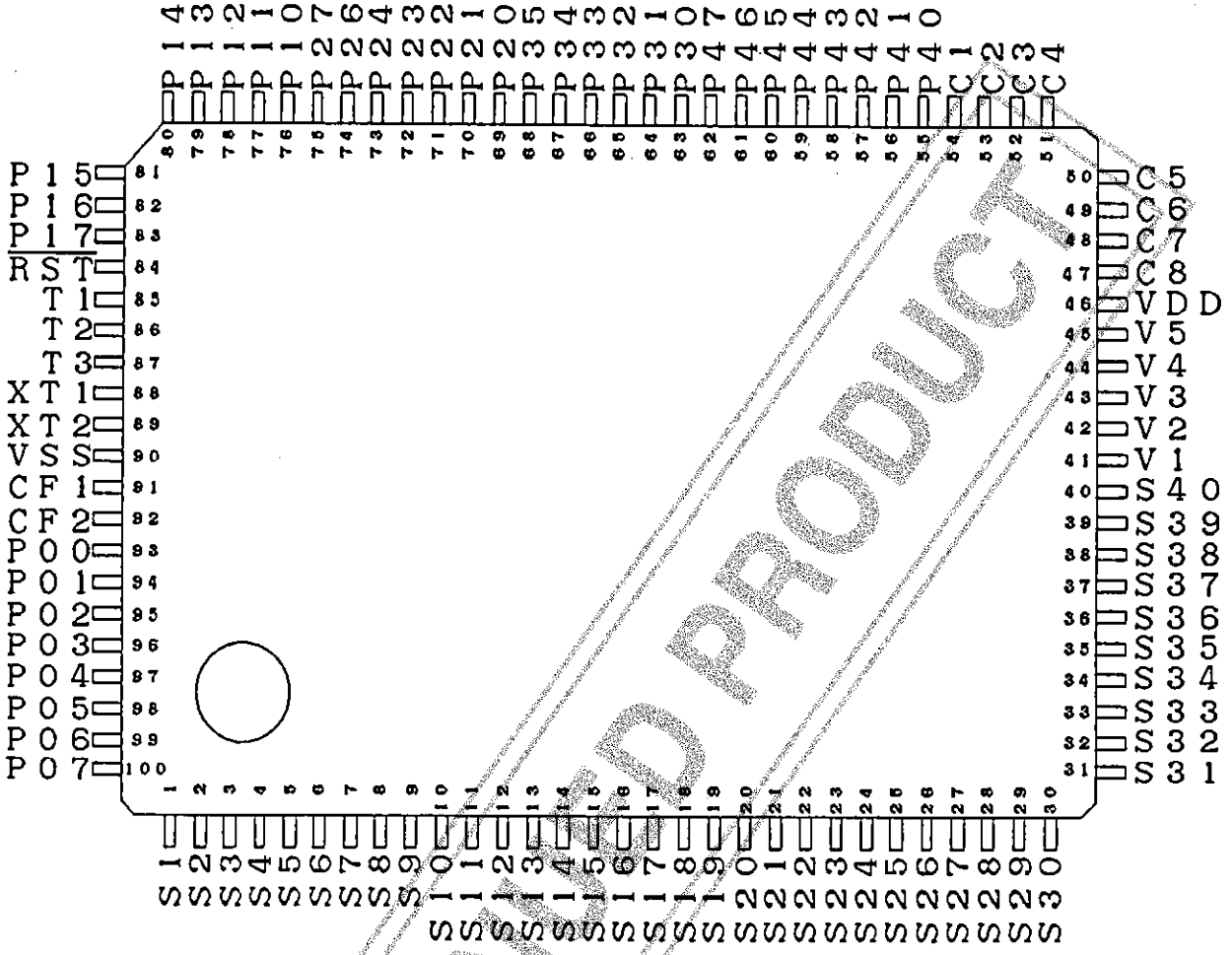
(1) User's Manual
    LC86104A user's manual
(2) Development support tool manual
    LC86104A development support tool manual
(3) Development support tools
  (a) Tools for developing the LC86104A application programs
    - MS-DOS machine
    - Macro assemblers (M86104.EXE and L86104.EXE)
    - Mask option selections program (SU86104.EXE)
  (b) Tools for evaluating the LC86104A application systems
    - Evaluation (EVA) chip: LC86999
    - Evaluation (EVA) chip board: TB86104
    - Evaluation (EVA) kit: EVA510

  Note: MS-DOS is a trademark of Microsoft Corporation.
  Note: The EVA510 board has the same function as the EVA410 board except for the monitor ROM.

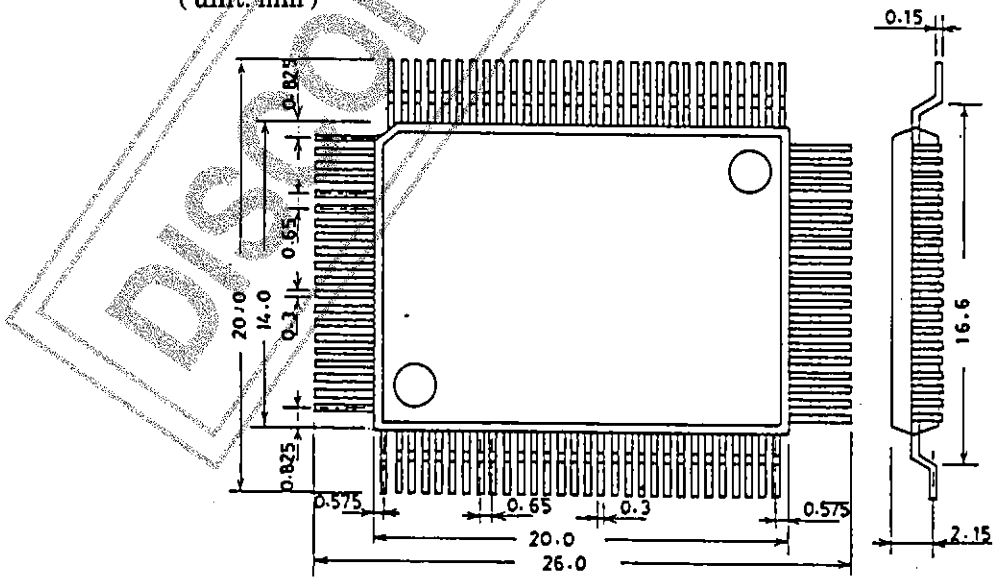
Outline of the development support system



Pin assignment

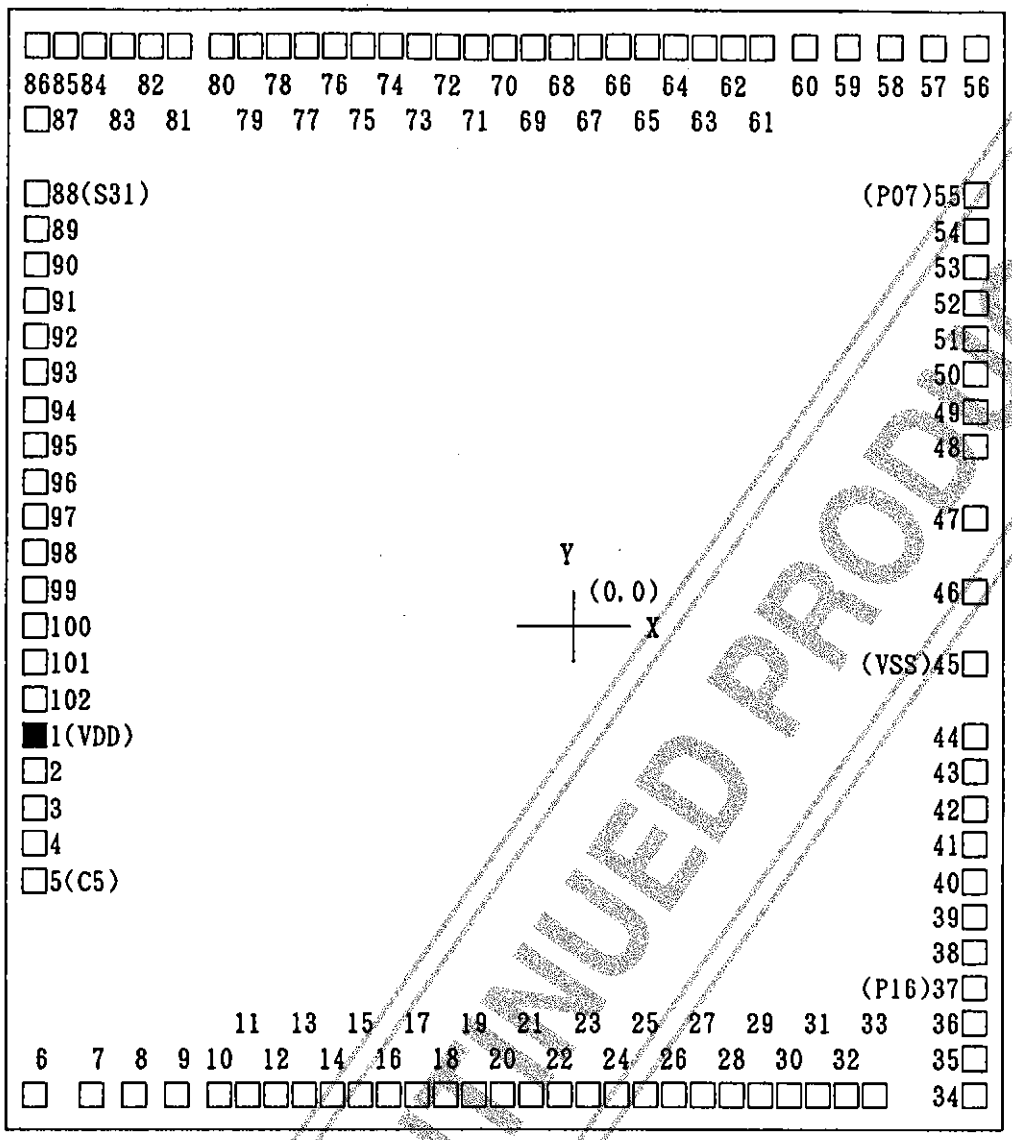


Package Dimensions 3089-Q100ALSI
(unit: mm)



SANYO: QIP100A

Pad assignment



Chip size (X x Y)
5.75mm x 4.70mm

Chip height
480um

Pad size
120μm x 120μm

Pad coordinate values

Pin number	Pad number	Pin name	Pad coordinate value X μm	Pad coordinate value Y μm	Pin number	Pad number	Pin name	Pad coordinate value X μm	Pad coordinate value Y μm
46	1	VDD	−2676	− 781	56	11	P41	−1697	−2011
47	2	C8	↓	− 941	57	12	P42	−1537	↓
48	3	C7	↓	−1101	58	13	P43	−1377	↓
49	4	C6	↓	−1261	59	14	P44	−1217	↓
50	5	C5	↓	−1421	60	15	P45	−1057	↓
51	6	C4	−2676	−2011	61	16	P46	− 897	↓
52	7	C3	−2429	↓	62	17	P47	− 737	↓
53	8	C2	−2249	↓	63	18	P30	− 577	↓
54	9	C1	−2068	↓	64	19	P31	− 417	↓
55	10	P40	−1857	−2011	65	20	P32	− 257	−2011

Pin number	Pad number	Pin name	Pad coordinate value		Pin number	Pad number	Pin name	Pad coordinate value	
			X μm	Y μm				X μm	Y μm
66	21	P33	−97	−2011	7	62	S7	1425	2150
67	23	P34	62	↓	8	63	S8	1265	↓
68	23	P35	222	↓	9	64	S9	1105	↓
69	24	P20	382	↓	10	65	S10	945	↓
70	25	P21	542	↓	11	66	S11	785	↓
71	26	P22	702	↓	12	67	S12	625	↓
72	27	P23	862	↓	13	68	S13	465	↓
73	28	P24	1022	↓	14	69	S14	305	↓
74	29	P26	1182	↓	15	70	S15	145	↓
75	30	P27	1342	↓	16	71	S16	−15	↓
76	31	P10	1502	↓	17	72	S17	−175	↓
77	32	P11	1662	↓	18	73	S18	−335	↓
78	33	P12	1822	↓	19	74	S19	−495	↓
79	34	P13	2530	−2011	20	75	S20	−655	↓
80	35	P14	↓	−1838	21	76	S21	−815	↓
81	36	P15	↓	−1672	22	77	S22	−975	↓
82	37	P16	↓	−1505	23	78	S23	−1135	↓
83	38	P17	↓	−1339	24	79	S24	−1295	↓
84	39	RST	↓	−1160	25	80	S25	−1455	↓
85	40	T1	↓	−1000	26	81	S26	−1773	↓
86	41	T2	↓	−840	27	82	S27	−1954	↓
87	42	T3	↓	−680	28	83	S28	−2134	↓
88	43	XT1	↓	−503	29	84	S29	−2315	↓
89	44	XT2	↓	−343	30	85	S30	−2495	↓
90	45	VSS	↓	−104	−	86	−	−2676	2150
91	46	CF1	↓	128	−	87	−	↓	1838
92	47	CF2	↓	288	31	88	S31	↓	1618
93	48	P00	↓	487	32	89	S32	↓	1458
94	49	P01	↓	647	33	90	S33	↓	1298
95	50	P02	↓	807	34	91	S34	↓	1138
96	51	P03	↓	967	35	92	S35	↓	978
97	52	P04	↓	1127	36	93	S36	↓	818
98	53	P05	↓	1287	37	94	S37	↓	658
99	54	P06	↓	1447	38	95	S38	↓	498
100	55	P07	↓	1607	39	96	S39	↓	338
1	56	S1	2530	2150	40	97	S40	↓	178
2	57	S2	2350	↓	41	98	V1	↓	18
3	58	S3	2170	↓	42	99	V2	↓	−141
4	59	S4	1989	↓	43	100	V3	↓	−301
5	60	S5	1809	↓	44	101	V4	↓	−461
6	61	S6	1585	2150	45	102	V5	−2676	−621

Note: Test pins T1 and T2 should be left unconnected.
Note: Test pin T3 should be connected with the V_{DD} pin.
Note: The chip substrate should be connected with the V_{SS} pin or be left unconnected.
Note: Pin-to-pin soldering connection should be adopted in mounting the QIP 100 package onto the printed circuit board (PCB). Entire package dipping should be avoided for this purpose.

Pin Description

Pin name	Pin number	I/O	Function Description
VSS	90	Output	Should be connected with the negative supply voltage pin.
VDD	46	Input	Should be connected with the positive supply voltage pin.
P00 ↓ P07	93 ↓ 100	Input/ output	Eight-bit input/output port with internal pull-up transistors. Data can be input/output from/to the port in 8 bits unit.
P10 ↓ P17	76 ↓ 83	Input/ output	Eight-bit input/output port with internal pull-up transistors. Data can be input/output from/to the port in a single bit unit.
P10	76	Input	Port pins 76 to 79 can be also used as the external signal input pins:
P11	77	Input	T0: External signal input pin to timer/counter 0.
P12	78	Input	T1: External signal input pin to timer/counter 1.
P13	79	Input	$\overline{INT0}$: External interrupt 0 input pin $\overline{INT1}$: External interrupt 1 input pin
P20 ↓ P24	69 ↓ 73	Input/ output	Seven-bit input/output port with internal pull-up transistors. Data can be input/output from/to the port in a single bit unit.
P26	74		
P27	75		
P30 ↓ P35	63 ↓ 68	Input/ output	Six-bit input/output port with internal pull-up transistors. Data can be input/output from/to the port in a single bit unit.
P40 ↓ P47	55 ↓ 62	Input/ output	Eight-bit input/output port with internal pull-up transistors. Data can be input/output from/to the port in a single bit unit.
			Port pins 55 to 60 can be also used as the special output pins:
P40	55	Output	CL1: Latch signal output to external Liquid Crystal Display driver circuit
P41	56	Output	CL2: Shift signal output to external Liquid Crystal Display driver circuit
P42	57	Output	D0: Data signal output to external Liquid Crystal Display driver circuit
P43	58	Output	M: Synchronization signal output to external Liquid Crystal Display driver circuit
P44	59	Output	ALM: Alarm signal output to the ALM output pin
P45	60	Output	PLS: Pulse signal output to the pulse output pin
V1 ↓ V5	41 ↓ 45	Input/ output	Voltage supply pins to Liquid Crystal Display drivers.
C1 ↓ C8	54 ↓ 47	Output	Common driver pins to Liquid Crystal Display drivers.

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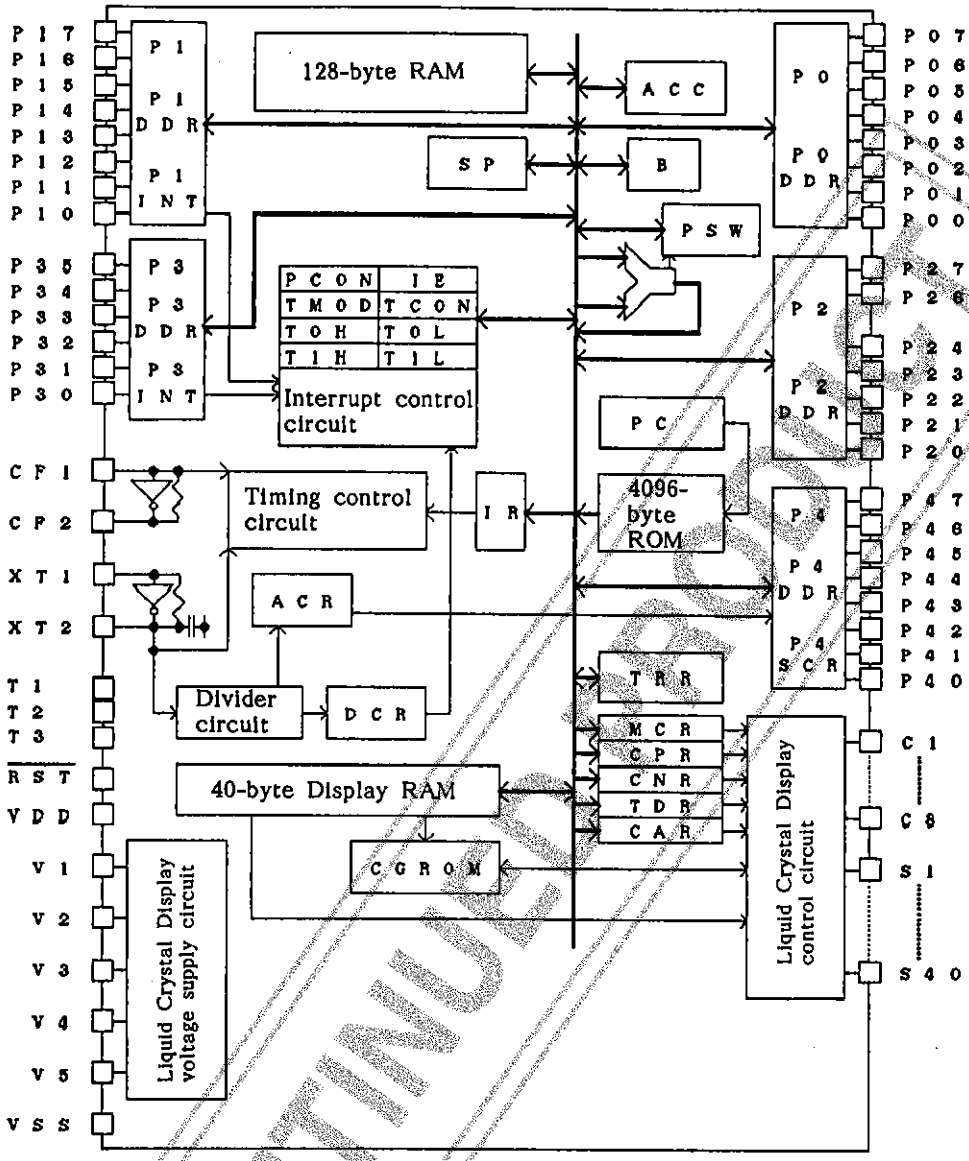
Pin name	Pin number	I/O	Functional Description
S 1 ↓ S 4 0	1 ↓ 4 0	Output	Segment driver pins to Liquid Crystal Display.
$\overline{\text{R S T}}$	8 4	Input	Reset signal input pin with an internal pull-up transistor.
T 1	8 5	Output	Should be left unconnected.
T 2	8 6	Output	Should be left unconnected.
T 3	8 7	Output	Should be connected with the V_{DD} pin.
X T 1	8 8	Input	Crystal oscillation input pin. Should be connected with the Crystal (X'tal) resonator with a 32.768kHz frequency.
X T 2	8 9	Output	Crystal oscillation output pin. Should be connected with the Crystal (X'tal) resonator with a 32.768kHz frequency. The internal 20pF capacitor is provided between the XT2 pin and the V_{SS} pin.
C F 1	9 1	Input	Ceramic oscillation input pin. Or RC (Resistor and Capacitor) oscillation input pin.
C F 2	9 2	Output	Ceramic oscillation output pin. Or RC (Resistor and Capacitor) oscillation output pin.

Functional block diagram



ACC	ACCUMULATOR	IE	INTERRUPT ENABLE REGISTER
B	B REGISTER	TMOD	TIMER/COUNTER MODE CONTROL REGISTER
PSW	PROGRAM STATUS WORD	TCON	TIMER/COUNTER CONTROL REGISTER
SP	STACK POINTER	TOH	TIMER/COUNTER0 HIGH BYTE
TRL	TABLE REFERENCE REGISTER LOW BYTE	TOL	TIMER/COUNTER0 LOW BYTE
TRH	TABLE REFERENCE REGISTER HIGH BYTE	T1H	TIMER/COUNTER1 HIGH BYTE
P0	PORT0 LATCH	T1L	TIMER/COUNTER1 LOW BYTE
P0DDR	PORT0 DATA DIRECTION REGISTER	PCON	POWER CONTROL REGISTER
P1	PORT1 LATCH	PC	PROGRAM COUNTER
P1DDR	PORT1 DATA DIRECTION REGISTER	IR	INSTRUCTION REGISTER
P1INT	PORT1 INTERRUPT REGISTER	MCR	MODE CONTROL REGISTER
P2	PORT2 LATCH	CPR	CHARACTER PITCH REGISTER
P2DDR	PORT2 DATA DIRECTION REGISTER	CNR	CHARACTER NUMBER REGISTER
P3	PORT3 LATCH	TDR	TIME DIVISION REGISTER
P3DDR	PORT3 DATA DIRECTION REGISTER	CAR	CURSOR ADDRESS REGISTER
P3INT	PORT1 INTERRUPT REGISTER	DR	DISPLAY RAM
P4	PORT4 LATCH	CGROM	CHARACTER GENERATOR ROM
P4DDR	PORT4 DATA DIRECTION REGISTER	ACR	ALARM CONTROL REGISTER
P4SCR	PORT4 SIGNAL CHANGE REGISTER	DCR	DIVIDER CONTROL REGISTER

Symbol	Address	Read/Write	Name	Initial reset value
—	—	—	Memory space	—

(1) Program memory (ROM) space
The LC86000 series microcomputers have a program memory (ROM) space of 64K bytes.

(2) Data memory (RAM) space
The LC86000 series microcomputers have a data memory (RAM) space of 512 bytes. The 512-byte RAM area can be functionally divided into the two areas: 256-byte data memory (RAM: 000H to 0FFH)) and 256-byte special function register (SFR) area (100H to 1FFH).
The 256-byte RAM area includes the stack area and the SFR area contains the accumulator (ACC), the program status word (PSW), timers, ports and the like. The SFR area allows the LC86000 series microcomputers to employ the full memory mapped I/O architecture.
The first 4 address areas (00H to 03H) in the data memory (RAM) can be used as the four 8-bit indirect address registers for allowing the user to make an access to the RAM in the indirect address mode. Of the above 4 indirect address registers, the first two registers with addresses 00H and 01H are used when the RAM area between address 00H and FFH is indirectly accessed. The remaining two index registers are used when the SFR area between address 100H and address 1FFH is indirectly accessed.
Bits 3 and 4 of the program status word (PSW) can be used with the indirect address registers to select 4 RAM banks.
The relationship between the indirect address registers, bits 3 and 4 of the PSW and the RAM addresses is shown in the table below.

PSW bit 4	PSW bit 3	Indirect address register	RAM address	Function
0	0	R 0	0 0 H	Indirect RAM addressing
		R 1	0 1 H	Indirect RAM addressing
		R 2	0 2 H	Indirect SFR addressing
		R 3	0 3 H	Indirect SFR addressing
0	1	R 0	0 4 H	Indirect RAM addressing
		R 1	0 5 H	Indirect RAM addressing
		R 2	0 6 H	Indirect SFR addressing
		R 3	0 7 H	Indirect SFR addressing
1	0	R 0	0 8 H	Indirect RAM addressing
		R 1	0 9 H	Indirect RAM addressing
		R 2	0 A H	Indirect SFR addressing
		R 3	0 B H	Indirect SFR addressing
1	1	R 0	0 C H	Indirect RAM addressing
		R 1	0 D H	Indirect RAM addressing
		R 2	0 E H	Indirect SFR addressing
		R 3	0 F H	Indirect SFR addressing

Symbol	Address	Read/Write	Name	Initial reset value
PC	–	–	Program counter	0000H

The program counter (PC) is a 16-bit register. It is used to point to the address in the program memory (ROM), which stores the next instruction to be executed. Normally, the content of the program counter (PC) is incremented by 1 each time one instruction is executed. However, the PC register will be loaded with predefined address data when branch instruction or subroutine instruction is executed in your application program.
In addition to this, the PC content will change according to interrupt requests and the initial reset request.
The table below shows the contents of the program counter (PC) when the above mentioned operations are performed.

Operation type		Program counter value
Initial reset		0000H
External interrupt 0		0003H
Timer/counter 0 interrupt		000BH
External interrupt 1		0013H
Timer/counter 1 interrupt		001BH
Divider circuit/port 1/ port 3 interrupt		0023H
Unconditional branching operation	JMP a12	PC15～12＝Current page、PC11～00＝a12
	JMPF a16	PC15～00＝a16
	BR r8	(PC+2) + (−128～+127)
	BRF r16	(PC+2) + (0～+65536)
Conditional branching operation	BZ r8	(PC+2) + (−128～+127)
Subroutine all operation	CALL a12	PC15～12＝Current page、PC11～00＝a12
	CALLF a16	PC15～00＝a16
	CALLR r16	(PC+2) + (0～+65536)

Note: The current page indicates the page area storing the instruction to be executed next.

Symbol	Address	Read/Write	Name	Initial reset value
ROM	–	Read only	Program memory	–

The program memory is a 4K-byte ROM (4096 x 8 bits). It stores a user application program to be executed on the LC86104A microcomputer. The whole content of the program memory (ROM) can be referenced by using the LDC instruction.

Symbol	Address	Read/Write	Name	Initial reset value
RAM	00H ↓ 7FH	Read/Write	Data memory	Unpredictable

The data memory is a 128-byte static RAM (128 x 8 bits). The first four bytes (00H to 03H) of the RAM are used as the indirect address registers for indirect addressing. The first two indirect address registers (00H and 01H) of the four are used for indirect RAM addressing and the remaining two registers (02H and 03H) for indirect special function register (SFR) addressing. In addition, these indirect address registers can be used with bits 3 and 4 of the program status word (PSW) to select 4 banks.

Symbol	Address	Read/Write	Name	Initial reset value
ACC	100H	Read/Write	Accumulator	00H

MSB							LSB
ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0

The accumulator (ACC) is a register used for calculation (logical or arithmetic), data transfer and data input/output.

Note: If the current content of the accumulator (ACC) is transferred to the ACC itself, the data in the accumulator (ACC) will be destroyed. For example, this may happen if you use the LD ACC instruction in your application program.

Symbol	Address	Read/Write	Name	Initial reset value
PSW	101H	Read/Write	Program status word	00×000××B

MSB							LSB
CY	AC	–	IRBK1	IRBK0	OV	–	–

CY: Carry flag

The carry flag (CY) is a flag which is set or reset when arithmetic operation is carried out. The carry flag (CY) will be set when an addition type instruction is executed in your application program and then a carry from the most significant bit (MSB) occurs. It will be reset when an addition type instruction is executed in your application program but a carry from the most significant bit (MSB) does not occur.

The carry flag (CY) will be set when a subtraction type or comparison type instruction is executed in your application program and a borrow to the most significant bit (MSB) occurs. It will be reset when a subtraction type or comparison type instruction is executed in your application program and a borrow to the most significant bit (MSB) does not occur.

In addition, the carry flag (CY) will be affected when a carry-through rotation type instruction is executed in your application program. It will be reset when an multiplication/division type instruction is executed in your application program.

AC: Auxiliary Carry Flag

The auxiliary carry flag (AC) is a flag which is set or reset when arithmetic operation instruction is executed in your application program.

The auxiliary carry flag (AC) will be set when an addition type instructiois executed in your application program and a carry from the third bit occurs. It will be reset when an addition type instruction is executed in your application program but a carry from the third bit does not occur.

The auxiliary carry flag (AC) will be set when a subtraction type instruction is executed in your application program and a borrow to the third bit occurs. It will be reset when a subtraction type instruction is executed in your application program but a borrow to the third bit does not occur.

IRBK1: Indirect address register bank 1

IRBK0: Indirect address register bank 0

These two bits (IRBK0 and IRBK1) of the program status word (PSW) are used to select 4 bank values for the indirect address registers.

As previously stated, the first 4 bytes of the RAM are used as the four indirect address registers for indirect addressing. Bits IRBK0 and IRBK1 can be jointly used with these four indirect address registers to make an indirect access to an address in a selected RAM bank area. For detailed information, please refer to Memory Space.

OV: Overflow flag

The overflow flag (OV) is a flag which is set or reset when an addition type or subtraction type instruction with signed variables is executed in your application program.

The overflow flag (OV) will be set when an addition type or subtraction type instruction with signed variables is executed in your application program and an overflow error then occurs. Otherwise it will be reset.

The overflow flag (OV) will be set when a multiplication type instruction is executed in your application program and the resulted product exceeds 256. It will be reset if the resulted product is less than 256.

In addition, the overflow flag (OV) will be set when a division type instruction is executed in your application program and the divisor is "0". Otherwise, it will not affected.

Symbol	Address	Read/Write	Name	Initial reset value
B	102H	Read/Write	B register	00H

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0

The B register is paired with the accumulator (ACC) and then used when a multiplication type or division type instruction is executed in your application program. In other operations, this register can be used as a general purpose register.

Symbol	Address	Read/Write	Name	Initial reset value
TRL	104H	Read/Write	Table reference register low-order byte	00H

MSB							LSB
TRL7	TRL6	TRL5	TRL4	TRL3	TRL2	TRL1	TRL0

The table reference register low-order byte is used to hold the low-order byte of a ROM address specified by the LDC instruction. This 8-bit register can be used as a general purpose register when any instruction other than the LDC instruction is executed in your application program.

Symbol	Address	Read/Write	Name	Initial reset value
TRH	105H	Read/Write	Table reference register high-order byte	00H

MSB							LSB
TRH7	TRH6	TRH5	TRH4	TRH3	TRH2	TRH1	TRH0

The table reference register high-order byte is used to hold the high-order byte of a ROM address specified by the LDC instruction. This 8-bit register can be used as a general purpose register when any instruction other than the LDC instruction is executed in your application program.

Symbol	Address	Read/Write	Name	Initial reset value
SP	106H	Read/Write	Stack pointer	Unpredictable

MSB							LSB
SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The stack pointer (SP) is incremented by 1 when the PUSH instruction is executed in your application program. It is decremented by 1 when the POP instruction is executed in your application program.
The stack pointer (SP) is incremented by 2 when the CALL instruction is used in your application program. It is decremented by 2 when the RET instruction is executed in your application program.
The stack pointer (SP) will be incremented by 2 when an interrupt request is accepted by the system, and will be decremented by 2 when the RETI instruction is executed at the end of the interrupt servicing routine. Note that the RETI instruction is used to transfer program execution back to the main routine from the interrupt service routine.
The stack pointer value will become unpredictable at power on.
Therefore, you should set an appropriate value in the stack pointer within the initial routine after power is applied.

Symbol	Address	Read/Write	Name	Initial reset value
PCON	107H	Read/Write	Power control register	×××××000B

MSB							LSB
–	–	–	–	–	PCON2	PCON1	PCON0

PCON2: Power control register bit 2
- 0: Disable the INT0 HOLD mode release request. Note that the $\overline{\text{INT0}}$ request signal becomes active when the L level voltage is applied to the P12 pin.
- 1: Enable the INT0 HOLD mode release request. Note that the $\overline{\text{INT0}}$ request signal becomes active when the L level voltage is applied to the P12 pin. In this case, program execution will start when timer/counter 0 outputs an overflow signal. As stated in the preceding paragraph, the overflow signal from timer/counter 0 will start the program execution. Therefore, timer/counter 0 can be used to prevent program execution from entering abnormal state when it is restarted immediately after the HOLD mode is released. For this purpose, you have to set an appropriate data in timer/counter 0 in advance. As a result, program execution will be restarted after the wait time period defined by the data in timer/counter 0 elapses. Note that the oscillation stabilization time period requires such wait time period.

PCON1: Power control register bit 1
- 0: Disable the HOLD mode request.
- 1: Enable the HOLD mode request. The HOLD mode stops both of the CF/RC oscillation circuit and the X'tal oscillation circuit. The microcomputer is allowed to operate in the low current dissipation mode. That is, only the leakage current operates the LSI.
  The HOLD mode can be released by the reset request signal or by applying L level voltage to the $\overline{\text{INT0}}$ (P12) pin with PCON2 = 1. In this case, the HOLD mode should be selected after all the interrupt requests are disabled. If you fail to follow this procedure, program may enter abnormal run state. Please keep it in mind.

PCON0: Power control register bit 0
- 0: Disable the HALT mode request.
- 1: Enable the HALT mode request. The HALT mode stops the program execution. This mode can be released by the reset request. It can be also released when an interrupt request is accepted by the system.

Symbol	Address	Read/Write	Name	Initial reset value
IE	108H	Read/Write	Interrupt enable control register	0××000000B

MSB							LSB
IE7	–	–	IE4	IE3	IE2	IE1	IE0

IE7: Interrupt enable control register bit 7
- 0: Disable all the interrupt requests.
- 1: Enable all the interrupt requests selected by bits IE4 to IE0.

IE4: Interrupt enable control register bit 4
- 0: Disable an interrupt request from the divider circuit, port 1 or port 3.
- 1: Enable an interrupt request from the divider circuit, port 1 or port 3. --- Vectored address 23H

IE3: Interrupt enable control register bit 3
- 0: Disable the interrupt request from timer/counter 1.
- 1: Enable the interrupt request from timer/counter 1. --- Vectored address 1BH

IE2: Interrupt enable control register bit 2
- 0: Disable the external interrupt 1 request.
- 1: Enable the external interrupt 1 request. --- Vectored address 13H

IE1: Interrupt enable control register bit 1
- 0: Disable the interrupt request from timer/counter 0.
- 1: Enable the interrupt request from timer/counter 0. --- Vectored address 0BH

IE0: Interrupt enable control register bit 0
- 0: Disable the external interrupt 0 request.
- 1: Enable the external interrupt 1 request. --- Vectored address 03H

Note: Some interrupt request flags are automatically reset or others are not automatically reset when interrupt requests are accepted by the system. These flags are as follows:

Interrupt flags to be automatically reset:
- Timer/counter control register bit 7 (interrupt request by timer/counter 1)
- Timer/counter control register bit 5 (interrupt request by timer/counter 0)
- Timer/counter control register bit 3 (external interrupt 1) --- Falling edge detection mode
- Timer/counter control register bit 1 (external interrupt 0) --- Falling edge detection mode

Interrupt request flags not to be automatically reset:
- Timer/counter control register bit 3 (external interrupt 1) --- L level detection mode
- Timer/counter control register bit 1 (external interrupt 0) --- L level detection mode
- Divider circuit control register bit 1 (interrupt from the divider circuit)
- Port 1 interrupt register bit 1 (interrupt from port 1)
- Port 3 interrupt register bit 1 (interrupt from port 3)

Note: Timer/counter interrupt detection mode from the falling edge detection and L level signal detection modes is selected by software.

Symbol	Address	Read/Write	Name	Initial reset value
TCON	110H	Read/Write	Timer/counter control register	00H

MSB							LSB
TCON7	TCON6	TCON5	TCON4	TCON3	TCON2	TCON1	TCON0

TCON7: Timer/counter control register bit 7
Timer/counter control register bit 7 is set when timer/counter 1 outputs an overflow signal and then automatically reset when an interrupt servicing routine is started.

TCON6: Timer/counter control register bit 6
0: Stop the timer/counter 1 operation.
1: Start the timer/counter 1 operation.

TCON5: Timer/counter control register bit 5
Timer/counter control register bit 5 is set when timer/counter 0 outputs an overflow signal and then automatically reset when an interrupt servicing routine is started.

TCON4: Timer/counter control register bit 4
0: Stops the timer/counter 0 operation.
1: Start the timer/counter 0 operation.

TCON3: Timer/counter control register bit 3
Timer/counter control register bit 3 is set when an external interrupt request signal from the $\overline{INT1}$ pin is generated and then automatically reset when the interrupt servicing routine is started. Please note keep it in mind that this bit is automatically reset only when the falling edge detection mode has been selected.

TCON2: Timer/counter control register bit 2
Timer/counter control register bit 2 is used to select a desired $\overline{INT1}$ interrupt detection mode from the falling edge detection and L level signal detection modes.
0: Select the L level signal detection mode.
1: Select the falling edge detection mode.
The H level signal before the interrupt request and the L level signal for triggering an interrupt should remain active for more than one machine cycles.

TCON1: Timer/counter control register bit 1
Timer/counter control register bit 1 is set when an external request signal from the $\overline{INT0}$ pin is generated and then automatically reset when the interrupt servicing routine is started. Please note this bit is automatically reset only if the falling edge detection mode has been selected.

TCON0: Timer/counter control register bit 0
Timer/counter control register bit 0 is used to select a desired $\overline{INT0}$ interrupt detection mode from the falling edge detection and L level signal detection modes.
0: Select the L level signal detection mode.
1: Select the falling edge detection mode.
The H level signal before the interrupt request and the L level signal for triggering an interrupt should remain active for more than one machine cycles.

Symbol	Address	Read/Write	Name	Initial reset value
TMOD	111H	Read/Write	Timer/counter mode control register	00H

MSB							LSB
TMOD7	TMOD6	TMOD5	TMOD4	TMOD3	TMOD2	TMOD1	TMOD0

TMOD7: Timer/counter mode control register bit 7

Timer/counter mode control register bit 7 is used to specify a desired input pulse to the timer/counter 1 gate.

0: Select the unconditional pulse input to the timer/counter 1 gate.

1: Select the conditional pulse input to the timer/counter 1 gate. In this case, pulses are input to timer/counter 1 only if the $\overline{INT1}$ (P13) = H level. Otherwise, they are not input to the timer/counter 1 gate.

TMOD6: Timer/counter mode control register bit 6

Timer/counter mode control register bit 6 is used to select the operation mode of timer/counter 1 from the timer operation and counter operation.

0: Select the timer operation mode. In this operation mode, timer/counter 1 will increment its value by 1 each machine cycle.

1: Select the event counter operation mode. In this operation mode, timer/counter 1 will count up the input clocks from the T1 (P11) pin.

TMOD5: Timer/counter mode control bit 5

TMOD4: Timer counter mode register bit 4

Mode	TMOD5	TMOD4	Timer/counter 1 mode
0	0	0	13-bit timer/counter
1	0	1	16-bit timer/counter
2	1	0	8-bit reload timer/counter

TMOD3: Timer/counter mode control register bit 3

Timer/counter mode control register bit 3 is used to specify a desired input pulse to the timer/counter 0 gate.

0: Select the unconditional pulse input to the timer/counter 0 gate.

1: Select the conditional pulse input to the timer/counter 0 gate. In this case, pulses are input to timer/counter 0 only if the $\overline{INT0}$ (P12) = H level. Otherwise, they are not input to the timer/counter 0 gate.

TMOD2: Timer/counter mode control register bit 2

Timer/counter mode control register bit 2 is used to select the operation mode of timer/counter 0 from the timer operation and counter operation.

0: Select the timer operation mode. In this operation mode, timer/counter 0 will increment its value by 1 each machine cycle.

1: Select the event counter operation mode. In this operation mode, timer/counter 0 will count up the input clocks from the T0 (P10) pin.

TMOD1: Timer/counter mode control bit 1

TMOD0: Timer counter mode register bit 0

Mode	TMOD1	TMOD0	Timer/counter 0 mode
0	0	0	13-bit timer/counter
1	0	1	16-bit timer/counter
2	1	0	8-bit reload timer/counter

Symbol	Address	Read/Write	Name	Initial reset value
T0L	112H	Read/Write	Timer/counter 0 low-order byte	00H

MSB							LSB
T0L7	T0L6	T0L5	T0L4	T0L3	T0L2	T0L1	T0L0

Symbol	Address	Read/Write	Name	Initial reset value
T0H	114H	Read/Write	Timer/counter 0 high-order byte	00H

MSB							LSB
T0H7	T0H6	T0H5	T0H4	T0H3	T0H2	T0H1	T0H0

Operation modes (selectable by bits TMOD0 and TMOD1)

(1) Mode 0 (13-bit timer/counter)

	MSB							LSB
T0H	12	11	10	09	08	07	06	05
T0L				04	03	02	01	00

(2) Mode 1 (16-bit timer/counter)

	MSB							LSB
T0H	15	14	13	12	11	10	09	08
T0L	07	06	05	04	03	02	01	00

(3) Mode 2 (8-bit reload timer/counter)

	MSB							LSB
T0H	07	06	05	04	03	02	01	00
T0L	07	06	05	04	03	02	01	00

Symbol	Address	Read/Write	Name	Initial reset value
T1L	113H	Read/Write	Timer/counter 1 low-order byte	00H

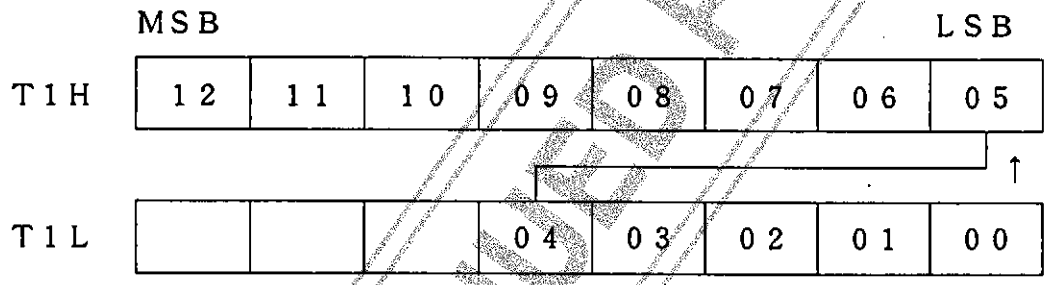
MSB							LSB
T1L7	T1L6	T1L5	T1L4	T1L3	T1L2	T1L1	T1L0

Symbol	Address	Read/Write	Name	Initial reset value
T1H	115H	Read/Write	Timer/counter 1 high-order byte	00H

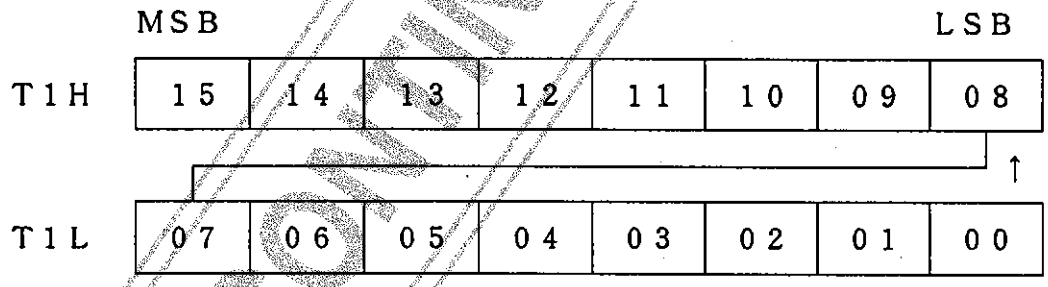
MSB							LSB
T1H7	T1H6	T1H5	T1H4	T1H3	T1H2	T1H1	T1H0

Operation modes (selectable by bits TMOD4 and TMOD5)

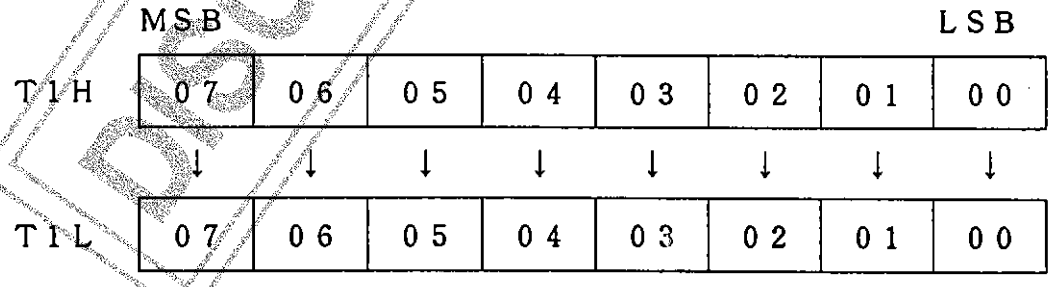
(1) Mode 0 (13-bit timer/counter)



(2) Mode 1 (16-bit timer/counter)



(3) Mode 2 (8-bit reload timer/counter)



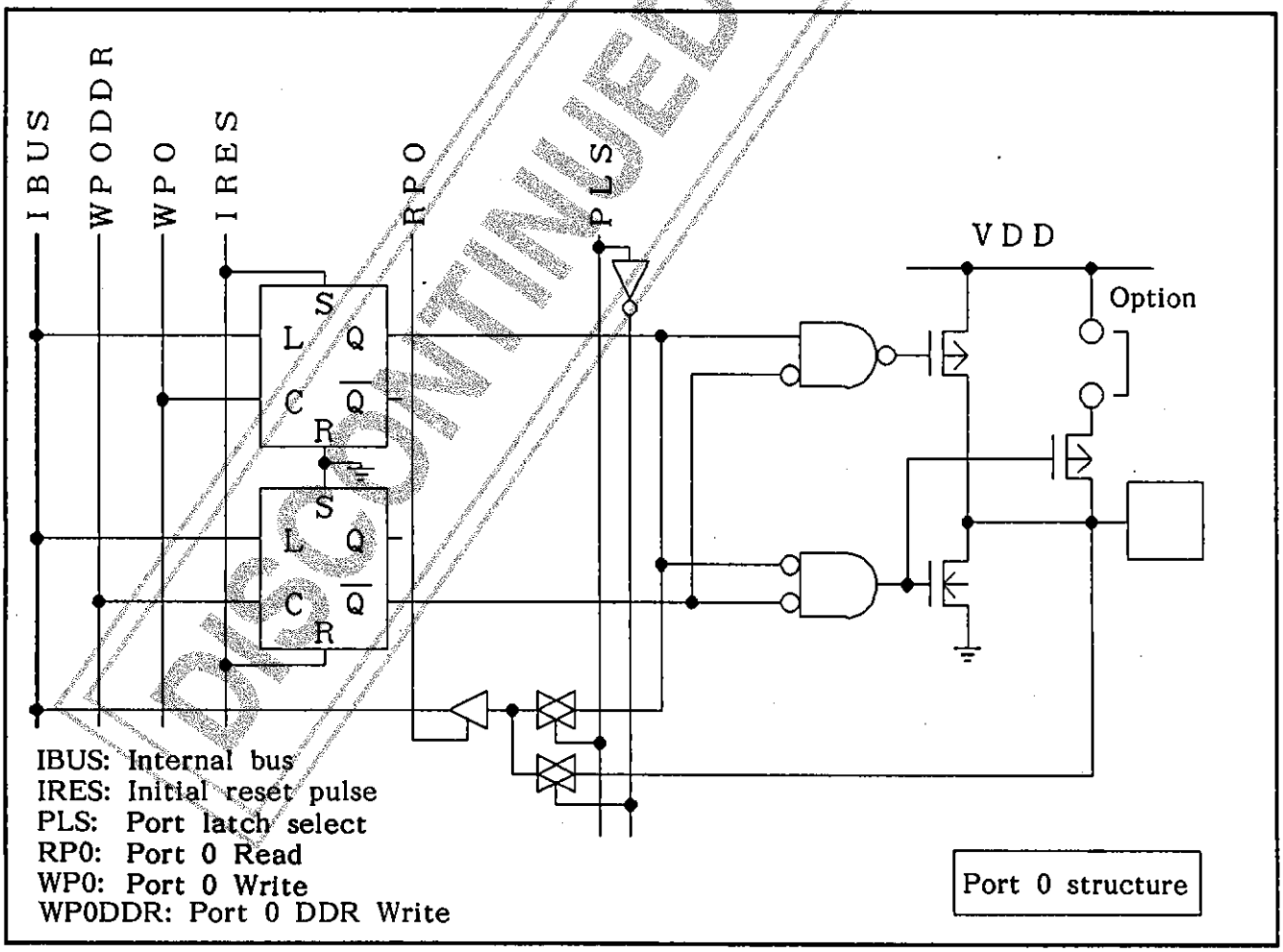
Symbol	Address	Read/Write	Name	Initial reset value
P0	140H	Read/Write	Port 0 latch	FFH

MSB							LSB
P07	P06	P05	P04	P03	P02	P01	P00

Symbol	Address	Read/Write	Name	Initial reset value
P0DDR	141H	Write only	Port 0 data direction register	××××××××0B

MSB							LSB
—	—	—	—	—	—	—	P0DDR

The port 0 data direction register is used to select a desired port 0 operation mode from the input and output modes in a byte unit.
P0DDR 0: Input mode 1: Output mode
Note: This register cannot be accessed by a bit manipulation instruction.



Port 0 structure

Symbol	Address	Read/Write	Name	Initial reset value
P1	144H	Read/Write	Port 1 latch	FFH

MSB							LSB
P17	P16	P15	P14	P13	P12	P11	P10

The following port 1 pins can be used for special signal input.

Port name	Special signal input
P13	External interrupt signal input ($\overline{INT1}$)
P12	External interrupt signal input ($\overline{INT0}$)
P11	External clock input to Timer/counter 1 (T1)
P10	External clock input to Timer/counter 0 (T0)

Symbol	Address	Read/Write	Name	Initial reset value
P1DDR	145H	Write only	Port 1 data direction register	00H

MSB							LSB
P17 DDR	P16 DDR	P15 DDR	P14 DDR	P13 DDR	P12 DDR	P11 DDR	P10 DDR

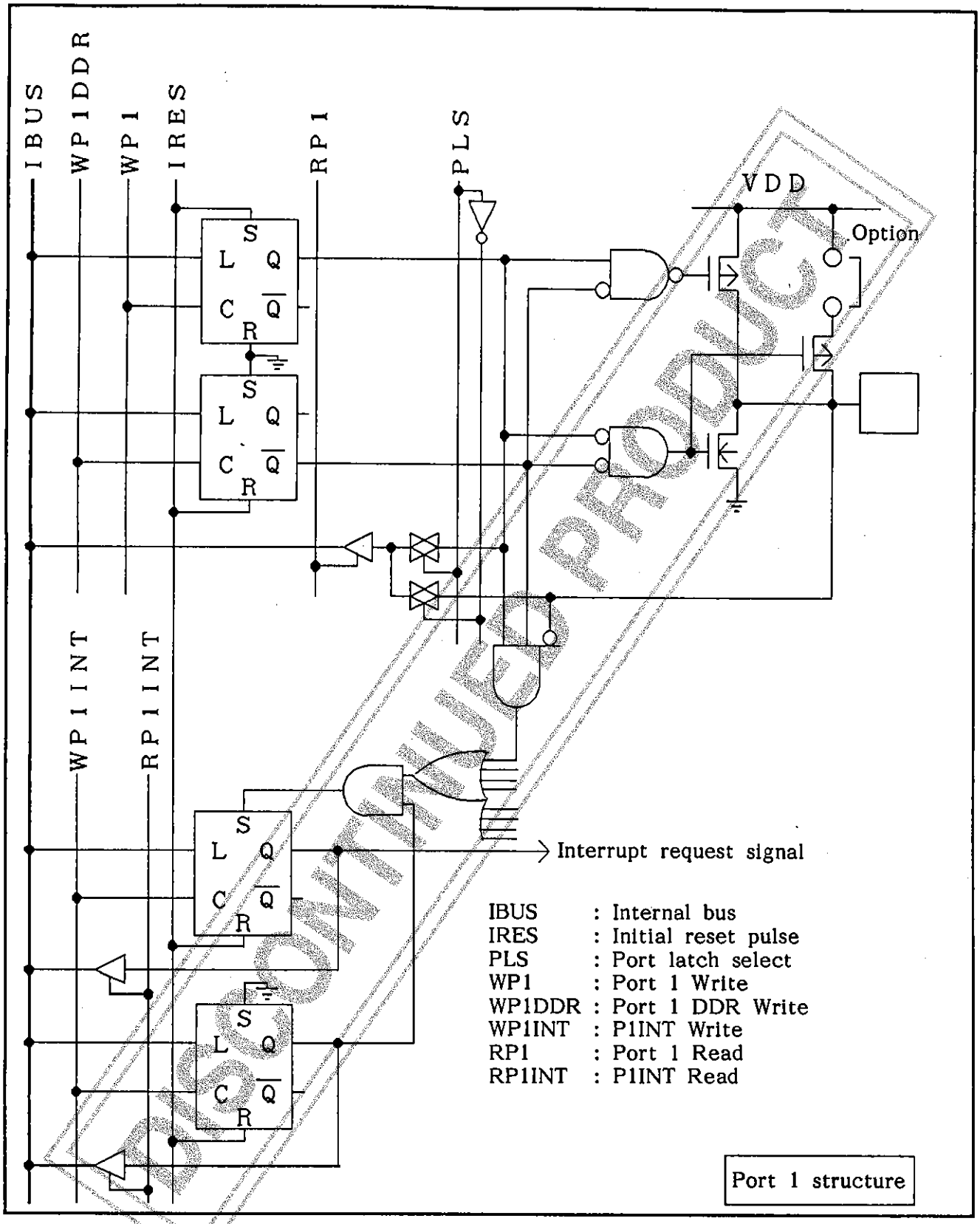
The port 1 data direction register is used to select a desired port 1 operation mode from the input and output modes in a single bit unit.
P1XDDR (X: 0 to 7) 0: Input mode 1: Output mode
Note: This register cannot be accessed by a bit manipulation instruction.

Symbol	Address	Read/Write	Name	Initial reset value
P1INT	146H	Read/Write	Port 1 interrupt control register	××××××00B

MSB							LSB
–	–	–	–	–	–	P1F	P1C

P1F: Port 1 interrupt flag
The port 1 interrupt flag is set when an L level signal is applied to an input port pin of port 1. In this case, the input port pin of port 1 should be set to the input mode in advance. In addition, the port output latch, and port 1 interrupt control bit P1C should be also set beforehand.

P1C: Port 1 interrupt control bit
0: Disable the interrupt from port 1.
1: Enable the interrupt from port 1.



Port 1 structure

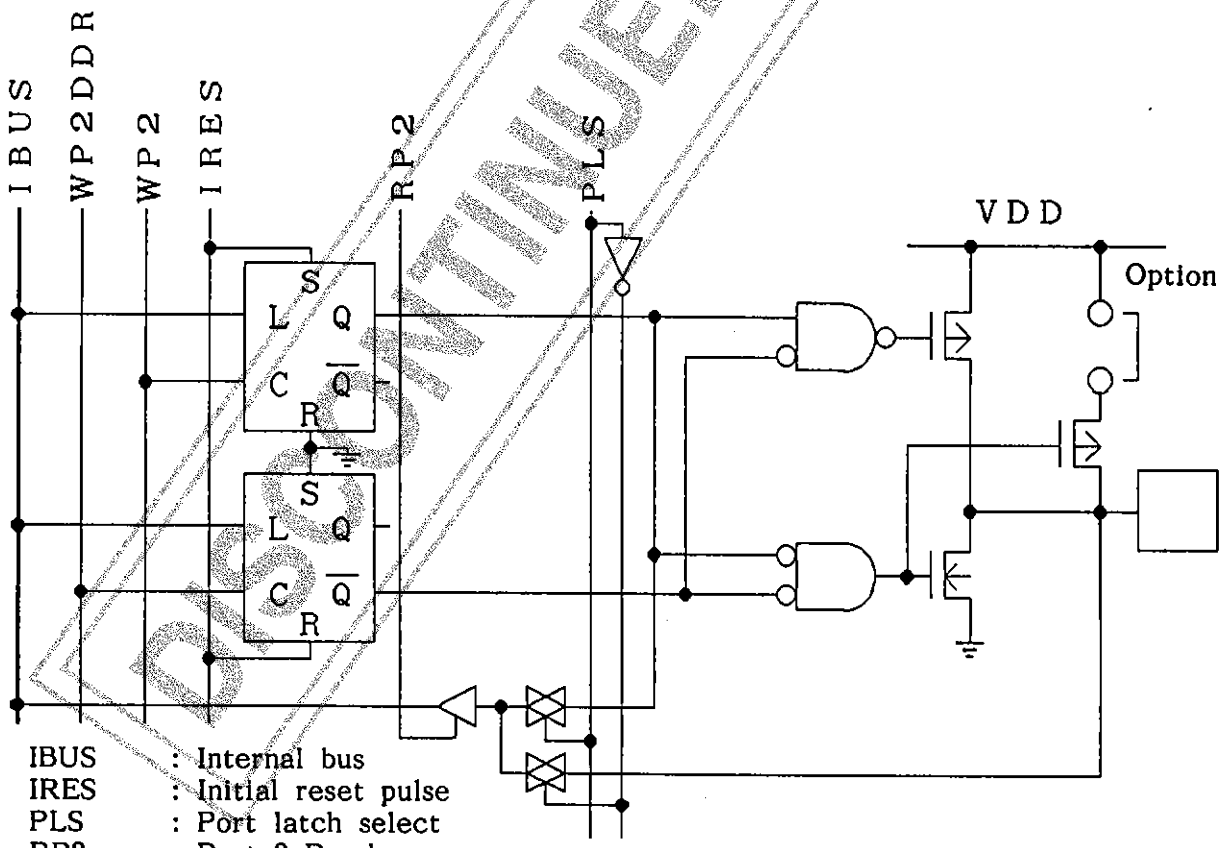
Symbol	Address	Read/Write	Name	Initial reset value
P2	148H	Read/Write	Port 2 latch	11×11111B

MSB							LSB
P27	P26	–	P24	P23	P22	P21	P20

Symbol	Address	Read/Write	Name	Initial reset value
P2DDR	149H	Write only	Port 2 data direction register	00×00000B

MSB							LSB
P27 DDR	P26 DDR	–	P24 DDR	P23 DDR	P22 DDR	P21 DDR	P20 DDR

The port 2 data direction register is used to select a desired port 2 operation mode from the input and output modes in a single bit unit.
P2XDDR (X: 0 to 4,6,7) 0: Input mode 1: Output mode
Note: This register cannot be accessed by a bit manipulation instruction.



IBUS : Internal bus
IRES : Initial reset pulse
PLS : Port latch select
RP2 : Port 2 Read
WP2 : Port 2 Write
WP2DDR : Port 2 DDR Write

Port 2 structure

Symbol	Address	Read/Write	Name	Initial reset value
P3	14CH	Read/Write	Port 3 latch	××111111B

MSB							LSB
–	–	P35	P34	P33	P32	P31	P30

Symbol	Address	Read/Write	Name	Initial reset value
P3DDR	14DH	Write only	Port 3 data direction register	××000000B

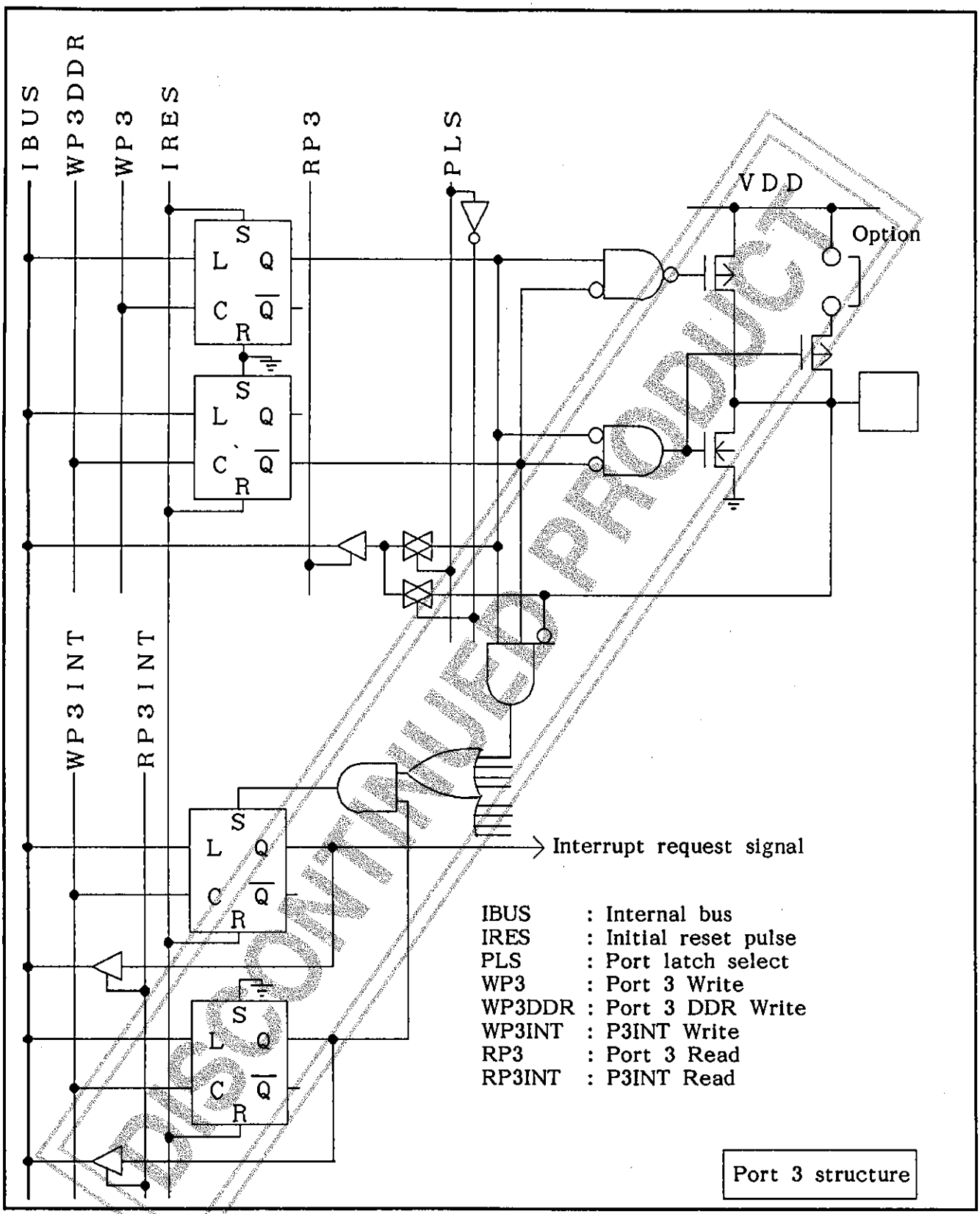
MSB							LSB
–	–	P35 DDR	P34 DDR	P33 DDR	P32 DDR	P31 DDR	P30 DDR

The port 3 data direction register is used to select a desired port 3 operation mode from the input and output modes in a single bit unit.
P3XDDR (X: 0 to 5) 0: Input mode 1: Output mode
Note: This register cannot be accessed by a bit manipulation instruction.

Symbol	Address	Read/Write	Name	Initial reset value
P3INT	14EH	Read/Write	Port 3 interrupt control register	××××××00B

MSB							LSB
–	–	–	–	–	–	P3F	P3C

P3F: Port 3 interrupt flag
The port 3 interrupt flag is set when an L level signal is applied to an input port pin of port 1. In this case, the input port pin of port 3 should be set to the input mode in advance. In addition, the port output latch, and port 3 interrupt control bit P3C should be also set beforehand.
P3C: Port 3 interrupt control bit
0: Disable the interrupt from port 3.
1: Enable the interrupt from port 3.



Port 3 structure

Symbol	Address	Read/Write	Name	Initial reset value
P4	150H	Read/Write	Port 4 latch	FFH

MSB							LSB
P47	P46	P45	P44	P43	P42	P41	P40

The following port 4 pins can be used for special output function.

Port pin name	Special output function
P45	Pulse output pin
P44	Alarm output pin
P43	External Liquid Crystal Display driver output pin (synchronization signal output M)
P42	External Liquid Crystal Display driver output pin (data signal output DO)
P41	External Liquid Crystal Display driver output pin (shift signal output CL2)
P40	External Liquid Crystal Display driver output pin (latch signal output CL1)

Symbol	Address	Read/Write	Name	Initial reset value
P4DDR	151H	Write only	Port 4 data direction register	00H

MSB							LSB
P47 DDR	P46 DDR	P45 DDR	P44 DDR	P43 DDR	P42 DDR	P41 DDR	P40 DDR

The port 4 data direction register is used to select a desired port 4 operation mode from the input and output modes in a single bit unit.
P4XDDR (X: 0 to 7) 0: Input mode 1: Output mode
Note: This register cannot be accessed by a bit manipulation instruction.

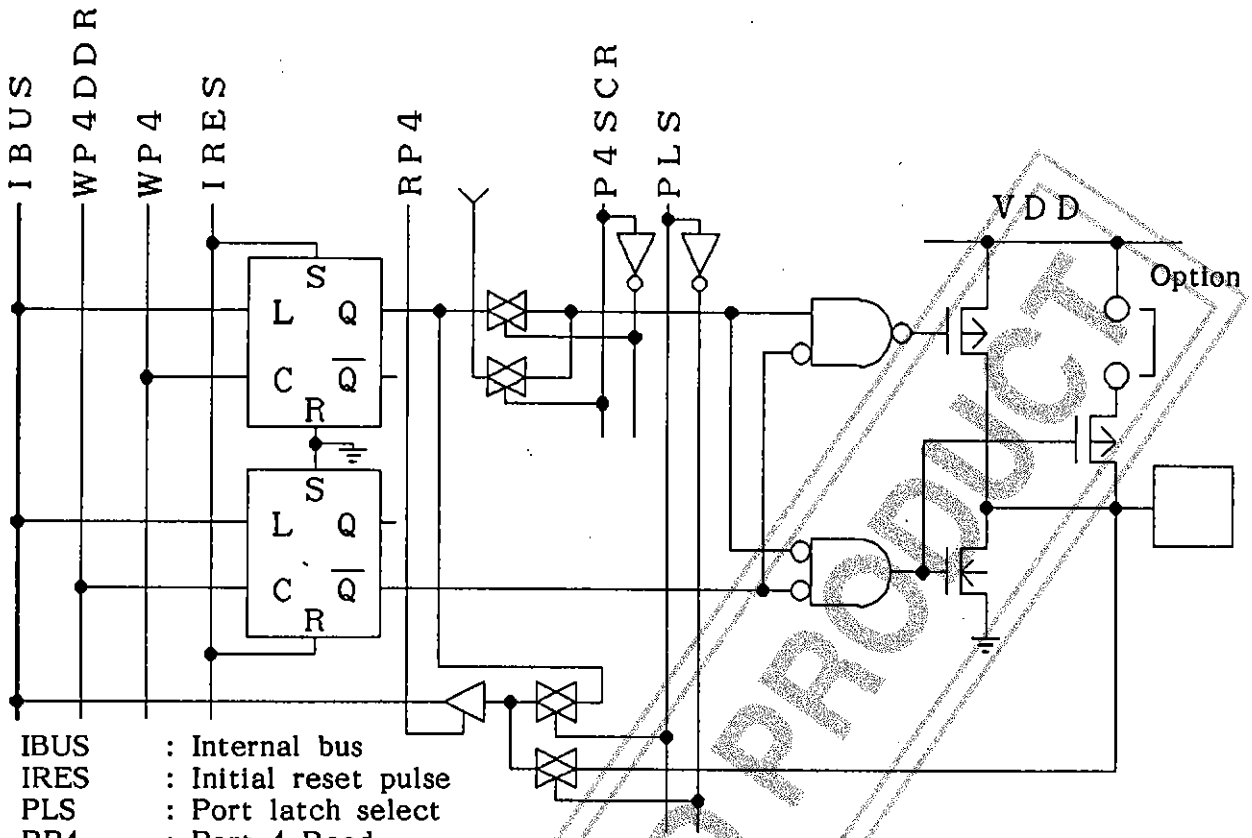
Symbol	Address	Read/Write	Name	Initial reset value
P4SCR	152H	Write only	Port 4 output signal selection register	××00×××0B

MSB							LSB
—	—	P45 SCR	P44 SCR	—	—	—	P40 SCR

P45SCR: P45 output signal selection bit
0: Select the P45 port latch output.
1: Select the pulse signal output.
P44SCR: P44 output signal selection bit
0: Select the P44 port latch output.
1: Select the alarm signal output.
P40SCR: P40 -P43 output signal selection bit

P40～P43	P40SCR	Output signal
P43	0	Select the P43 port latch output.
	1	Select the external Liquid Crystal Display driver output (synchronization signal output M).
P42	0	Select the P42 port latch output.
	1	Select the external Liquid Crystal Display driver output (data signal output DO).
P41	0	Select the P41 port latch output.
	1	Select the external Liquid Crystal Display driver output (shift signal output CL2).
P40	0	Select the P40 port latch output.
	1	Select the external Liquid Crystal Display driver output (latch signal output CL1).

Note: If you are to select the external Liquid Crystal Display driver output, please reset bit 0 of the mode control register to activate the character display mode.
Note: This register cannot be accessed by a bit manipulation instruction.



Port 4 structure

Symbol	Address	Read/Write	Name	Initial reset value
DR	180H ↓ 1A7H	Read/Write	Display RAM	Unpredictable

The display RAM is a static RAM with a capacity of 40 bytes (40 x 8 bits). The liquid Crystal Display driver circuit receives the display data from the display RAM and then generates dot matrix Liquid Crystal Display driver signals. There are two types of Liquid Crystal Display modes available on the LC86104A microcomputer: Graphic display mode and Character display mode. In the graphic display mode, every single bit of the display RAM can be used to turn on/off a single Liquid Crystal Display dot. In the character display mode, the internal character generator ROM is used to output a predefined dot character pattern to the Liquid Crystal Display driver circuit after receiving a character code already stored in the display RAM from the Liquid Crystal Display control circuit.

Symbol	Address	Read/Write	Name	Initial reset value
CG ROM	—	—	Character generator ROM	—

The character generator ROM (CGROM) is a 5600-bit ROM used in the character display mode.
The Liquid Crystal Display control circuit receives a character code already stored in the display RAM and then transfers it to the character generator ROM. The character generator ROM generates the corresponding dot pattern according to the character code output by the control circuit. Finally, the Liquid Crystal Display driver circuit generates a dot matrix Liquid Crystal Display driver signals to display a desired character on the panel.
The character generator ROM (CGROM) contents can be defined by the user. That is, you can set up to 160 types of character patterns in the character generator ROM (CGROM). Please note that each character pattern should have a character font of 5 x 7 dots (Max.).

Symbol	Address	Read/Write	Name	Initial reset value
MCR	1E0H	Write Only	Mode control register	××××0000B

MSB							LSB
–	–	–	–	MCR3	MCR2	MCR1	MCR0

MCR3: Mode control register bit 3
- 0: Place the Liquid Crystal Display in the OFF state. In this case, the supply voltage pins (V1 to V5) for Liquid Crystal Display are electronically connected with the V_{DD} pin. The common driver pins (C1 to C8) and segment driver pins (S1 to S40) are also electronically connected with the V_{DD} pin.
- 1: Place the Liquid Crystal Display in the ON state. In this case, you can output a desired signal to the common driver pins (C1 to C8) and the segment driver pins (S1 to S40) by electronically connecting the V5 supply voltage pin to the V_{SS} pin. To control display brightness, add a resistor between the V5 pin and the V_{SS} pin.

MCR2: Mode control register bit 2

MCR1: Mode control register bit 1

Mode control register bits 1 and 2 (MCR1 and MCR2) are used to control cursor display operation. The cursor display operations are shown in the table below. Note that these two bits can be effective only in the character display mode (MCR0 = 0).

MCR2	MCR1	Cursor display	Blink	Description
0	0	OFF	–	Place the cursor display operation in the OFF state.
0	1	ON	–	Place the cursor display operation in the ON state. The cursor is displayed under the display character specified by the cursor address register (CAR).
1	0	OFF	Character	The display character specified by the cursor address register (CAR) will blink. Black-White blinking mode.
1	1	ON	Cursor	The cursor is displayed under the display character specified by the cursor address register (CAR) and then blinks.

MCR0: Mode control register bit 0
- 0: Character display mode
  The character display mode uses an internal character generator ROM to generate a desired dot pattern. The dot pattern is generated according to a character code stored in the display RAM.
- 1: Graphic display mode
  Each bit of the display RAM is used to turn on or off a single dot of the Liquid Crystal Display panel.

Note: This register cannot be accessed by a bit manipulation instruction.

Symbol	Address	Read/Write	Name	Initial reset value
CPR	1E1H	Write Only	Character pitch register	×000×000B

MSB							LSB
–	CPR6	CPR5	CPR4	–	CPR2	CPR1	CPR0

CPR6: Character pitch register bit 6
CPR5: Character pitch register bit 5
CPR4: Character pitch register bit 4
Character display mode: These character pitch register bits are used to specify the number of bits per character in the vertical direction (Vp).
Graphic display mode: These character pitch register bits have no significance.
The table below shows the relationship between the combinations of these bits and the vertical number of bits per character.

CPR6	CPR5	CPR4	Vp
0	0	0	1
0	0	1	2
0	1	0	3
↓	↓	↓	↓
1	0	1	6
1	1	0	7
1	1	1	8

CPR2: Character pitch register bit 2
CPR1: Character pitch register bit 1
CPR0: Character pitch register bit 0
Character display mode: These character pitch register bits are used to specify the number of bits per character in the horizontal direction (Hp).
Graphic display mode: These character pitch register bits are used to specify the effective number of display bits of each display RAM address.
The table below shows the relationship between the combinations of these bits and the number of bits (Hp).

CPR2	CPR1	CPR0	Hp
0	0	0	Not assigned.
0	0	1	Not assigned.
0	1	0	Not assigned.
0	1	1	4
↓	↓	↓	↓
1	1	1	8

Note: Hp values 1 through 3 cannot be specified. Please keep it in mind.
Note: This register cannot be accessed by a bit manipulation instruction.

Symbol	Address	Read/Write	Name	Initial reset value
CNR	1E3H	Write Only	Character number register	××000000B

MSB							LSB
–	–	CNR5	CNR4	CNR3	CNR2	CNR1	CNR0

CNR5: Character number register bit 5
↓ ↓
CNR0: Character number register bit 0

Character display mode: These character number register bits are used to specify the number of characters in the horizontal direction.
Graphic display mode: These character count register bits are used to specify the number of bytes in the horizontal direction (Hn). The total number of dots in the horizontal direction can be calculated by (Hp x Hn).
The table below shows the relationship between the combinations of these bits and Hn.

CNR5	CNR4	CNR3	CNR2	CNR1	CNR0	Hn
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
↓	↓	↓	↓	↓	↓	↓
1	0	0	1	0	1	38
1	0	0	1	1	0	39
1	0	0	1	1	1	40

Note: This register cannot be accessed by a bit manipulation instruction.

Symbol	Address	Read/Write	Name	Initial reset value
TDR	1E4H	Write Only	Time division register	×××××000B

MSB							LSB
–	–	–	–	–	TDR2	TDR1	TDR0

TDR2: Time division register bit 2
TDR1: Time division register bit 1
TDR0: Time division register bit 0

These time division register bits are used to specify the number of character lines in the vertical direction (Nx). Note that these vertical character lines are controlled by time division technique. The reciprocal of Nx indicates a display duty cycle. The total number of display dots on the Liquid Crystal Display panel can be calculated by (Hp x Hn x Nx).

The table below shows the relationship between the combinations of these bits and the number of vertical character lines (Nx).

TDR2	TDR1	TDR0	Vertical character line count (Nx)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Note: This register cannot be accessed by a bit manipulation instruction.

Symbol	Address	Read/Write	Name	Initial reset value
CAR	1E5H	Read/Write	Cursor address register	××000000B

MSB							LSB
–	–	CAR5	CAR4	CAR3	CAR2	CAR1	CAR0

CAR5: Cursor address register bit 5

↓ ↓

CAR0: Cursor address register bit 0

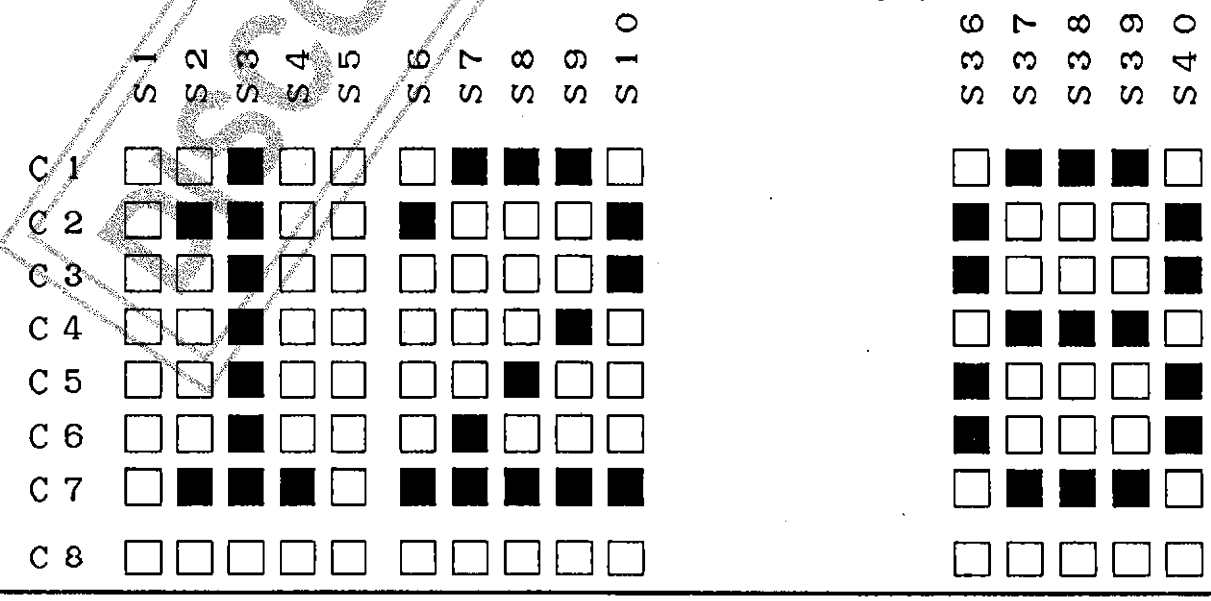
Character display mode: These cursor address register bits are used to specify a display RAM address whose content will be displayed on the Liquid Crystal Display panel marked by a cursor. Note that the cursor is displayed under the display character and that the cursor display is controlled by the mode control register (MCR).

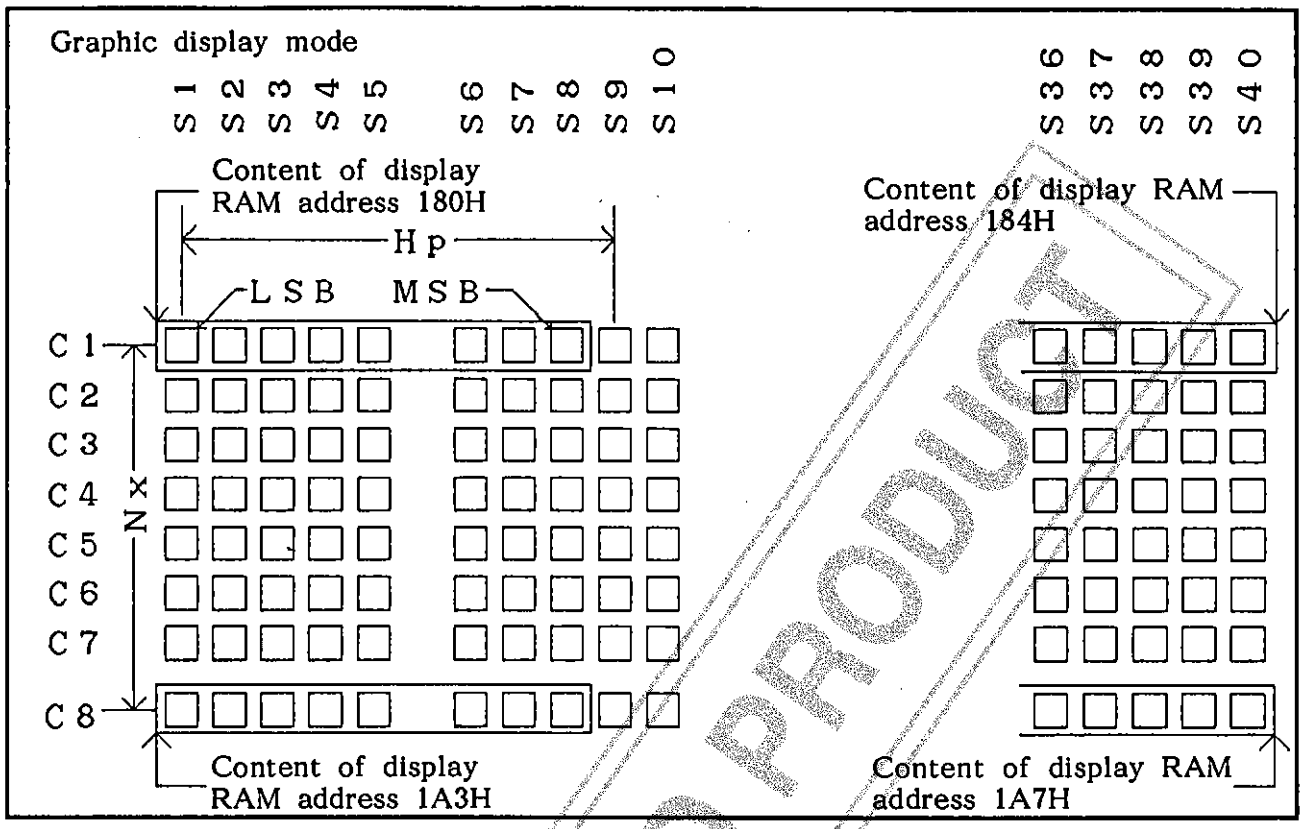
Graphic display mode: These cursor address register bits have no significance.

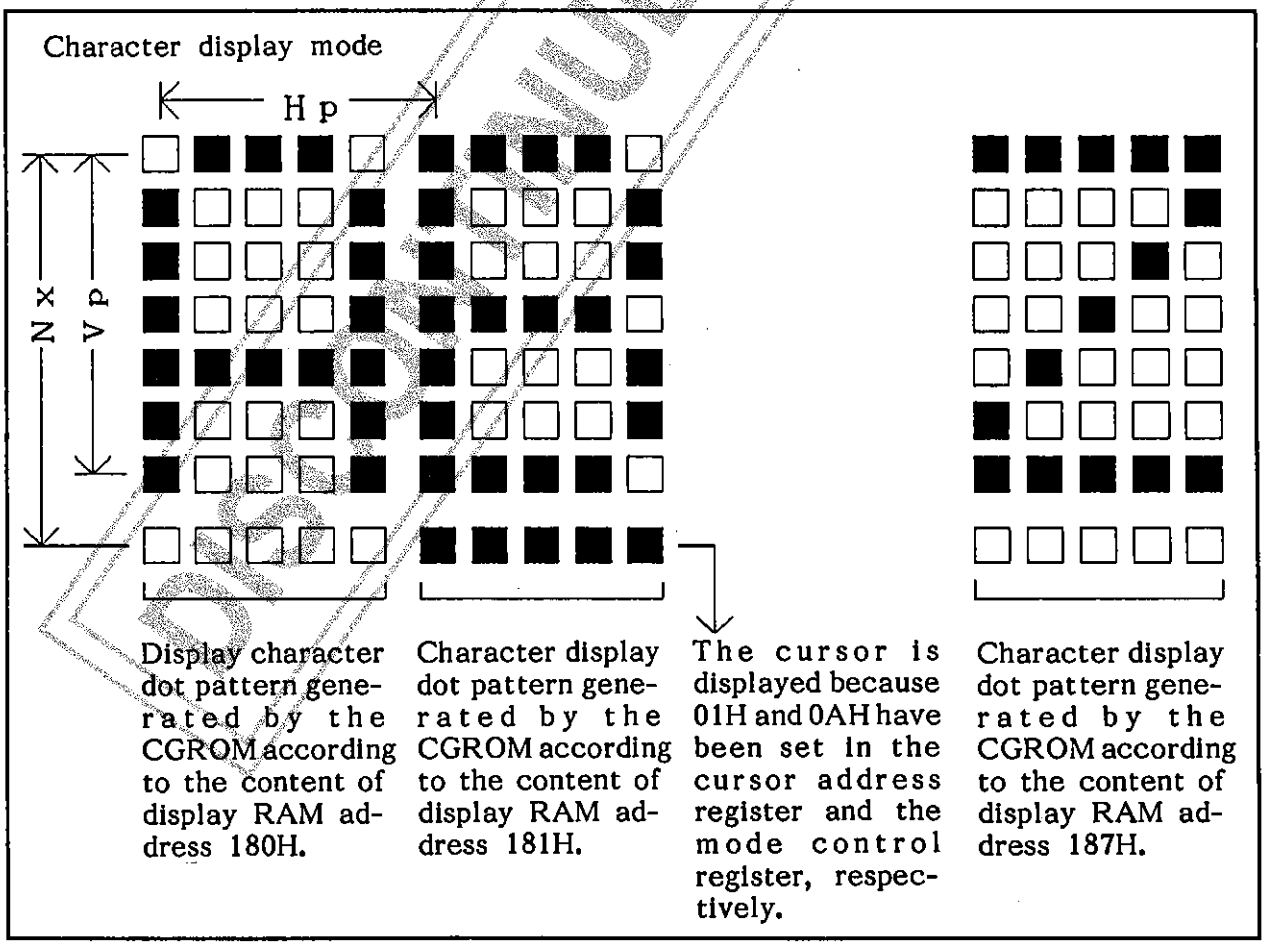
The table below shows the relationship between the combinations of these bits and the display RAM addresses.

CAR5	CAR4	CAR3	CAR2	CAR1	CAR0	Specifiable display RAM address
0	0	0	0	0	0	180H
0	0	0	0	0	1	181H
0	0	0	0	1	0	182H
↓	↓	↓	↓	↓	↓	↓
1	0	0	1	0	1	1A5H
1	0	0	1	1	0	1A6H
1	0	0	1	1	1	1A7H

Common driver pins, segment driver pins and character display



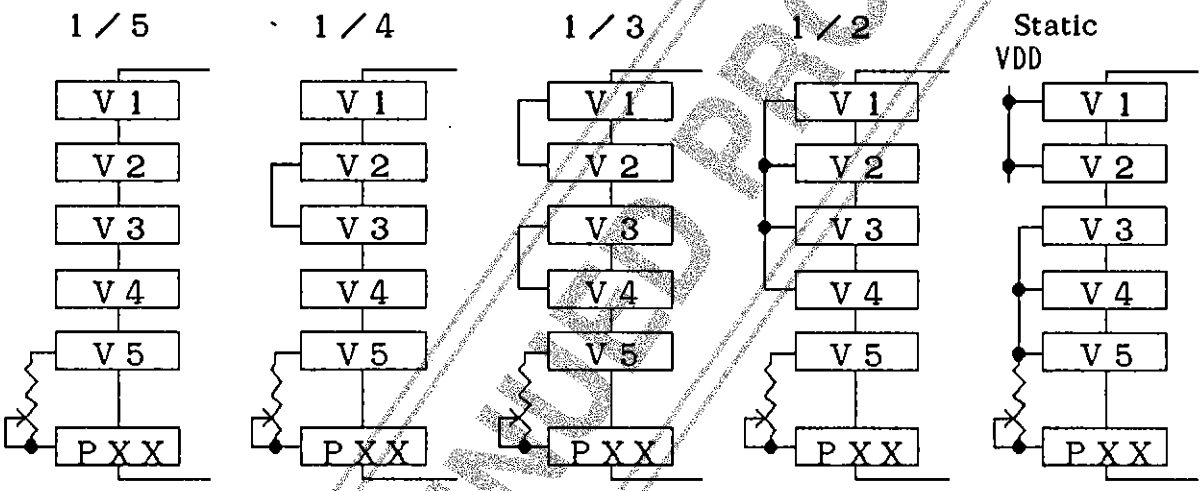




Hp, Hn, Vp, Nx and Liquid Crystal display

Symbol	Name	Meaning	Value
Hp	Horizontal character pitch	Character pitch in horizontal direction	4 to 8 bits
Hn	Horizontal character count	Character display mode: Character count per line (or in horizontal direction). Graphic display mode: Byte count per line (or in horizontal direction).	1 to 40 characters
Vp	Vertical character pitch	Character pitch in vertical direction	1 to 8 bits
Nx	Vertical character line count	Display duty cycle	1 to 8 lines

Bias modes



Note:

Set port pin PXX to the L level when you are to turn on the Liquid Crystal Display panel. In this case, set bit 3 of the mode control register (MCR) first and then set the PXX pin to the L level.

Set port pin PXX to the H level and then reset bit 3 of the mode control register (MCR) when you are to turn off the Liquid Crystal Display panel.

If you do not follow the above procedures, excessive current at about 1mA will be dissipated by the LSI when the display panel is turned on/off.

Symbol	Address	Read/Write	Name	Initial reset value
ACR	1FCH	Write Only	Alarm control register	00×00000B

MSB							LSB
ACR7	ACR6	—	ACR4	ACR3	ACR2	ACR1	ACR0

ACR7: Alarm control register bit 7
- 0: Disable the pulse output to sound an alarm tone.
- 1: Enable the pulse output to sound an alarm tone.

Note: The pulse output reverses its polarity by an overflow signal from timer/counter 0 if alarm control register bit 6 (ACR6) has been set to "1".

ACR6: Alarm control register bit 6
- 0: Fix the pulse output at the "H" level.
- 1: Allow the pulse output to reverse its polarity by an overflow signal from timer/counter 0.

ACR4: Alarm control register bit 4
- 0: Select the fundamental frequency of 4kHz for the alarm tone specified by bits ACR0 to ACR3.
- 1: Select the fundamental frequency of 2kHz for the alarm tone specified by bits ACR0 to ACR3.

ACR3: Alarm control register bit 3
- 0: Disable the fundamental frequency selected by ACR4 to generate the alarm tone signal.
- 1: Enable the fundamental frequency selected by ACR4 to generate the alarm tone signal.

ACR2: Alarm control bit 2
- 0: Disable the combination of the signal frequencies of 32Hz, 4Hz, and 4kHz or 2kHz (fundamental frequency selected by ACR4) to sound an alarm tone.
- 1: Enable the combination of the signal frequencies of 32Hz, 4Hz, and 4kHz or 2kHz (fundamental frequency selected by ACR4) to sound an alarm tone.

ACR1: Alarm control register bit 1
- 0: Disable the combination of the signal frequencies of 4Hz, 1Hz and 4kHz or 2kHz (fundamental frequency selected by ACR4) to sound an alarm tone.
- 1: Enable the combination of the signal frequencies of 4Hz, 1Hz, and 4kHz or 2kHz (fundamental frequency selected by ACR4) to sound an alarm tone.

ACR0: Alarm control register bit 0
- 0: Disable the combination of the signal frequencies of 32Hz, 4Hz, 1Hz and 4kHz or 2kHz (fundamental frequency selected by ACR4) to sound an alarm tone.
- 1: Enable the combination of the signal frequencies of 32Hz, 4Hz, 1Hz, and 4kHz or 2kHz (fundamental frequency selected by ACR4) to sound an alarm tone.

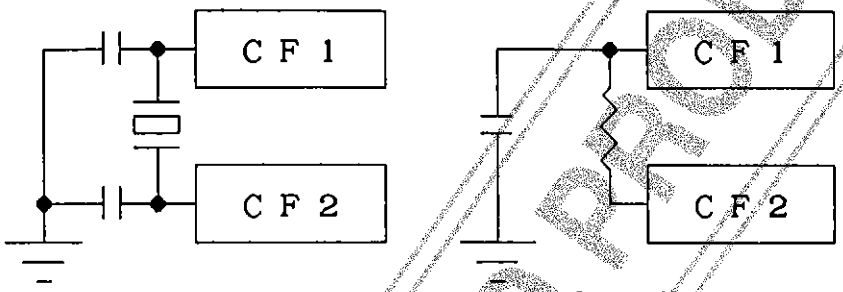
Note: To enable an alarm tone signal to be output to port pin P44, you have to set pin P44 to the output mode. In addition, bit 4 of the port 4 output signal selection register (P4SCR) should be set to "1".

Note: This register cannot be accessed by a bit manipulation instruction. Please keep it in mind.

Symbol	Address	Read/Write	Name	Initial reset value
–	–	–	CF/RC oscillation circuit	–

The CF/RC oscillation circuit is composed of the CF1 and CF2 pins, and ceramic oscillator or RC oscillator. The ceramic oscillator or the RC oscillator can be selected by the mask option.
The CF/RC oscillation signal can be as the system clock signal and the Liquid Crystal Display timing control signals.

The figures below show the example CF and RC oscillation circuits.



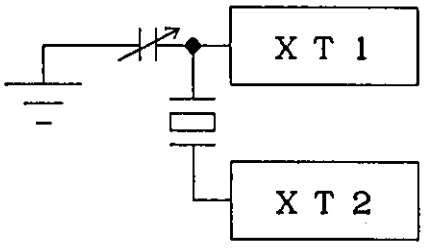
CF oscillation circuit

RC oscillation circuit

Symbol	Address	Read/Write	Name	Initial reset value
–	–	–	XTAL oscillation circuit	–

The XTAL oscillation circuit is composed of the XT1 and XT2 pins, and the Crystal (XTAL) resonator. The capacitor of 20pF is provided between the XT2 pin and the VSS pin. The XTAL oscillation signal can be used as the timer base clock signal, system clock signal, and the Liquid Crystal Display timing control signals.
The Liquid Crystal Display timing control signal source can be selected from the CF/RC oscillation circuit and the XTAL oscillation circuit by the mask option.

The figure below shows the example XTAL resonator oscillation circuit.



XTAL resonator oscillation circuit

Symbol	Address	Read/Write	Name	Initial reset value
DIVR	–	–	Divider circuit	0000H

The divider circuit receives the signal frequency output from the 32kHz XTAL resonator oscillation circuit and then divides its input signal. This divider circuit is a up-counter with 15 output taps. The outputs from the divider circuit can be used to supply time base clock and alarm tone signals to the system.

Symbol	Address	Read/Write	Name	Initial reset value
DCR	1FDH	Read/Write	Divider circuit control register	××××××000B

MSB							LSB
–	–	–	–	–	DCR2	DCR1	DCR0

DCR2: Divider circuit control register bit 2
- 0: Reset the divider circuit.
- 1: Enable the divider circuit to divide the input signal frequency from the 32kHz XTAL resonator oscillation circuit.

DCR1: Divider circuit control register bit 1

The DCR1 is used to generate an interrupt request. This bit is set by an overflow signal from the divider circuit every 500 milliseconds with the DCR0 = 1. Please note that the DCR1 is not reset when the interrupt request is accepted by the system and thereby must be reset within the interrupt servicing routine.

DCR0: Divider circuit control register bit 0
- 0: Disable the DCR1 to be set by an overflow signal from the divider circuit every 500 milliseconds.
- 1: Enable the DCR1 to be set by an overflow signal from the divider circuit every 500 milliseconds.

Symbol	Address	Read/Write	Name	Initial reset value
OCR	1FEH	Write Only	Oscillation control register	×××××××0B

MSB							LSB
–	–	–	–	–	–	–	OCR0

OCR0: Oscillation control register bit 0
- 0: Start the CF/RC oscillation circuit.
- 1: Stop the CF/RC oscillation circuit.

Note: Set bit 0 of the system clock control register (SCR) to "1" when you write a data to the oscillation control register (OCR). That is, start or stop the CF/RC oscillation circuit after switching the system clock source to the XTAL resonator oscillation circuit. If you do not follow this advice, the system may enter the abnormal run state. Please keep it in mind.

Note: This register cannot be accessed by a bit manipulation instruction.

Symbol	Address	Read/Write	Name	Initial reset value
SCR	1FFH	Write Only	System clock control register	××××××××0B

MSB							LSB
–	–	–	–	–	–	–	SCR0

SCR0: System clock control register bit 0
0: Select the CF/RC oscillation circuit as the system clock source.
1: Select the XTAL oscillation circuit as the system clock source.

Note: Set bit 0 of the system clock control register (SCR) to "1" when you write a data to the oscillation control register (OCR). That is, start or stop the CF/RC oscillation circuit after switching the system clock source to the XTAL resonator oscillation circuit. If you do not follow this advice, the system may enter the abnormal run state. Please keep it in mind.
Note: This register cannot be accessed by a bit manipulation instruction.

User mask options

The following user mask options are available on the LC86104A microcomputer.

User mask option	Optional items	Description
CF/RC oscillation circuit selection	- CF oscillation circuit - RC oscillation circuit	Select the CF oscillation circuit with the CF1 and CF2 pins or the RC oscillation circuit with the CF1 and CF2 pins
Liquid Crystal Display controller clock source selection	- XTAL oscillation circuit - CF/RC oscillation circuit	Select either the XTAL oscillation circuit or the CF/RC oscillation circuit as the Liquid Crystal Display controller clock source.
Liquid Crystal Display controller clock division rate selection	- 1/1 - 1/2 - 1/4 - 1/8 - 1/16 - 1/32 - 1/64 - 1/128	Select the division rate of the Liquid Crystal Display controller clock. This user mask option allows the divider to output the clock with a desired Liquid Crystal Display frame frequency (Ffrm: 40Hz to 80Hz) to the display control circuit.
Port 0 pull-up transistor (resistor) selection	- Pull-up circuit selection - Non pull-up circuit selection	Select the port 0 input circuit type from the pull-up input circuit configuration and the open input circuit configuration.
Port 1 pull-up transistor (resistor) selection	- Pull-up circuit selection - Non pull-up circuit selection	Select the port 1 input circuit type from the pull-up input circuit configuration and the open input circuit configuration.
Port 2 pull-up transistor (resistor) selection	- Pull-up circuit selection - Non pull-up circuit selection	Select the port 2 input circuit type from the pull-up input circuit configuration and the open input circuit configuration.
Port 3 pull-up transistor (resistor) selection	- Pull-up circuit selection - Non pull-up circuit selection	Select the port 3 input circuit type from the pull-up input circuit configuration and the open input circuit configuration.
Port 4 pull-up transistor (resistor) selection	- Pull-up circuit selection - Non pull-up circuit selection	Select the port 4 input circuit type from the pull-up input circuit configuration and the open input circuit configuration.

Note: The Liquid Crystal Display frame frequency can be calculated by the following formula:
Ffrm = (Fosc x Ndiv)/(2 x Ndot)
Fosc: Oscillation frequency from a Liquid Crystal Display controller clock source
Ndiv: Division rate for Liquid Crystal Display controller clock
Ndot: Total number of Liquid Crystal Display dots (Ndot = Hp x Hn x Nx)

Note: Pull-up transistor (resistor) can be selected in port unit by the user mask option. Please note that the pull-up resistor cannot be selected in a port bit unit by the option.

LC86104A Electrical characteristics

■ Absolute maximum ratings/V_{SS} = 0V and Ta = 25 ℃

Parameter	Symbol	Pins and Conditions	Limits		
			Min	Max	Unit
Supply voltage	VDD		−0.3	+7	V
Input voltage	VIN		−0.3	VDD +0.3	V
Peak output current	IOP	Input/output ports. Output current per pin.	−2	+20	mA
Average output current	IOA	Input/output port. Average output current per pin for 100 milliseconds.	−2	+20	mA
Output current 1	EIOA1	Port 0. Total output current.	−3	+30	mA
Output current 2	EIOA2	Ports 1, 2, 3, and 4. Total output current.	−23	+110	mA
Power dissipation (MAX.)	Pdmax	Ta = −30℃ ~ +70℃, QIP100		400	mW
Operating temperature range	Topr		−30	+70	℃
Storage temperature range	Tstg		−55	+150	℃

■ Recommended operating voltage range/Ta range = -30 ℃ to +70 ℃.

V_{DD} range = 2.5V to 6.0V. V_{SS} = 0V.

Parameter	Symbol	Pins and Conditions	Limits			Unit
			Min	Typ	Max	
Operating supply voltage range	VDD1	1μS≦TCYC≦366μS	4.5		6.0	V
	VDD2	4μS≦TCYC≦366μS	2.5		6.0	V
HOLD voltage	VHD	RAM and register hold voltage	2.0		6.0	V
Input high voltage	VIH1	All input port pins except for the $\overline{RST}$ pin	VDD		0.7 VDD	V
	VIH2	$\overline{RST}$	VDD		0.75 VDD	V
Input low voltage	VIL1	All input port pins except for the $\overline{RST}$ port pin	0		0.3 VDD	V
	VIL2	$\overline{RST}$	0		0.25 VDD	V
Oscillation frequency range	FOSC1	CF1、2(Ceramic oscillation) VDD=4.5～6.0V	11	12	13	MHz
	FOSC2	CF1、2(Ceramic oscillation) VDD=2.5～6.0V	2.5	3.0	3.5	MHz
	FOSC3	CF1、2 (RC oscillation) VDD=2.5～6.0V R=15KΩ、C=100pF	0.4	0.8	1.2	MHz
	FOSC4	XT1、2 (Crystal oscillation) VDD=2.5～6.0V	30	32	34	KHz

■ Electrical Characteristics/Ta = -30 ℃ to +70 ℃. VSS = 0V

Parameter	Symbol	Pins and Conditions	Limits			Unit
			Min	Typ	Max	
Output high voltage	VOH1	All output pins VDD=4.5V IOH=-1.0mA	0.9 VDD			V
	VOH2	All output pins VDD=2.5V IOH=-0.3mA	0.9 VDD			V
Output low voltage	VOL1	All output pins VDD=4.5V IOL=+4.0mA			0.1 VDD	V
	VOL2	All output pins VDD=2.5V IOL=+1.0mA			0.1 VDD	V
Pull-up transistor resistor	RP1	All input/output pins VDD=5V, VOH=0.9VDD	13	38	73	KΩ
	RP2	All input/output pins VDD=2.9V, VOH=0.9VDD	22	66	128	KΩ
	RP3	$\overline{RST}$, VDD=5V, VOH=0V	0.17	0.5	1.1	MΩ
	RP4	$\overline{RST}$, VDD=2.9V, VOH=0V	0.35	1	2.6	MΩ
Hysteresis voltage	VHYS	$\overline{RST}$		0.1 VDD		V
Input leak current	|ILI|	VIN=VDD OR VIN=VSS			1.0	μA
Pin capacitance	CP	FC=1MHz			10	pF
Current dissipation during basic operation	IDD1	Liquid Crystal Display OFF VDD=5V, FXT=32KHz FCF=12MHz		9.5	15	mA
	IDD2	Liquid Crystal Display OFF VDD=5V, FXT=32KHz FRC=800KHz		0.7	1.1	mA
	IDD3	Liquid Crystal Display OFF VDD=5V, FXT=32KHz FCF=FRC=0Hz		35	165	μA
	IDD4	Liquid Crystal Display OFF, VDD=2.9V FXT=32KHz, FCF=3MHz		1.4	2.2	mA
	IDD5	Liquid Crystal Display OFF VDD=2.9V, FXT=32KHz FRC=800KHz		390	615	μA
	IDD6	Liquid Crystal Display OFF VDD=2.9V, FXT=32KHz FCF=FRC=0Hz		15	42	μA

Parameter	Symbol	Pins and Conditions	Limits			Unit
			Min	Typ	Max	
Current dissipation during HALT operation	IDD7	Liquid Crystal Display OFF, VDD=5V FXT=32KHz FCF=12MHz		3.0	4.6	mA
	IDD8	Liquid Crystal Display OFF, VDD=5V FXT=32KHz FRC=800KHz		280	435	μA
	IDD9	Liquid Crystal Display OFF, VDD=5V FXT=32KHz FCF=FRC=0Hz		15	40	μA
	IDD10	Liquid Crystal Display OFF, VDD=2.9V FXT=32KHz、FCF=3MHz		440	705	μA
	IDD11	Liquid Crystal Display OFF, VDD=2.9V FXT=32KHz FRC=800KHz		150	240	μA
	IDD12	Liquid Crystal Display OFF, VDD=2.9V FXT=32KHz FCF=FRC=0Hz		5	19	μA
Current dissipation during HOLD operation	IDD13	Liquid Crystal Display OFF, VDD=5V			10	μA
	IDD14	Liquid Crystal Display OFF, VDD=2.9V			7	μA
Liquid Crystal Display current	ILC1	Liquid Crystal Display ON, VDD=5V V5=0V, 1/5 Bias mode	5	10	20	μA
	ILC29	Liquid Crystal Display ON, VDD=2.9V V5=0V, 1/5 Bias mode	2.9	5.8	12	μA

Note: During the Liquid Crystal Display OFF, you have to reset bit 3 (MCR3) of the mode control register without fail. If you do not follow this procedure, the IDD12 current value will be increased twice or three times.

Parameter	Symbol	Pins and Conditions	Limits			Unit
			Min	Typ	Max	
VDD-Ci voltage drop (i : 1～8)	| VD1 |	-15 micro Ampere per C pin VDD=2.9V			120	mV
VX-Ci voltage drop (X : 1、4) (i : 1～8)	| VD2 |	-15 micro Ampere per C pin VDD=2.9V			120	mV
VDD-Si voltage drop (i : 1～40)	| VD3 |	-15 micro Ampere per S pin VDD=2.9V			120	mV
V1 output voltage	VV1	VDD=2.9V, V5=0V Liquid Crystal Display clock frequency = 0Hz	0.75 VDD	0.80 VDD	0.85 VDD	V
V2 output voltage	VV2	VDD=2.9V, V5=0V Liquid Crystal Display clock frequency = 0Hz	0.55 VDD	0.60 VDD	0.65 VDD	V
V3 output voltage	VV3	VDD=2.9V, V5=0V Liquid Crystal Display clock frequency = 0Hz	0.35 VDD	0.40 VDD	0.45 VDD	V
V4 output voltage	VV4	VDD=2.9V, V5=0V Liquid Crystal Display clock frequency = 0Hz	0.15 VDD	0.20 VDD	0.25 VDD	V
Oscillation start time period	Tstt1	VDD=4.5 to 6.0V 12-MHz ceramic oscillation			30	mS
	Tstt2	VDD=2.5 to 6.0V 3-MHz ceramic oscillation			30	mS
	Tstt3	VDD=2.5 to 6.0V 32-KHz crystal (XTAL) oscillation			10	S

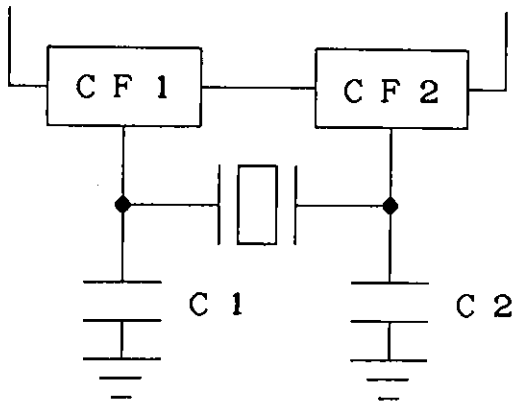


Figure 1. CF oscillation circuit

Table 1. Recommended ceramic oscillation constants

Oscillator type	Producer	Oscillator	C 1	C 2
12-MHz ceramic oscillator	Murata	CSA12.0 MT	33pF	33pF
		CST12.0 MT	On chip	On chip
	Kyocera	KBR – 12.0 M	33pF	33pF
3-MHz ceramic oscillator	Murata	CSA 3.00 MG	33pF	33pF
		CST 3.00 MGW	On chip	On chip
	Kyocera	–	–	–

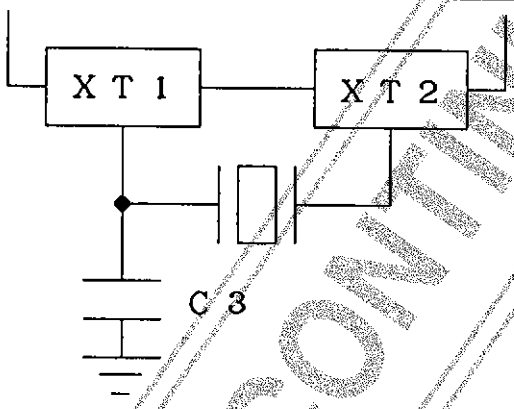
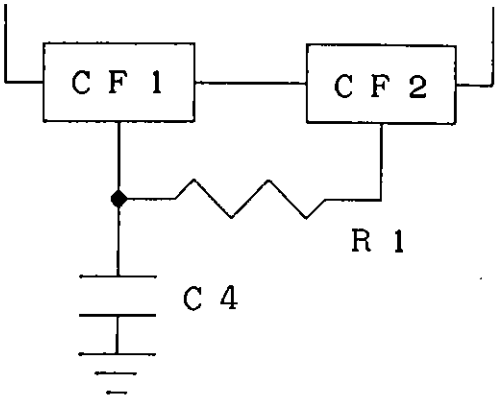


Figure 2. Crystal oscillation circuit

Table 2. Recommended crystal oscillation constants

Oscillator type	Producer	Oscillator	C 3
32.768kHz crystal (XTAL) oscillator	Daiwa Sinku	DT-38	22pF



R 1 = 1 5 K Ω

C 4 = 1 0 0 p F

Figure 3. RC oscillation circuit

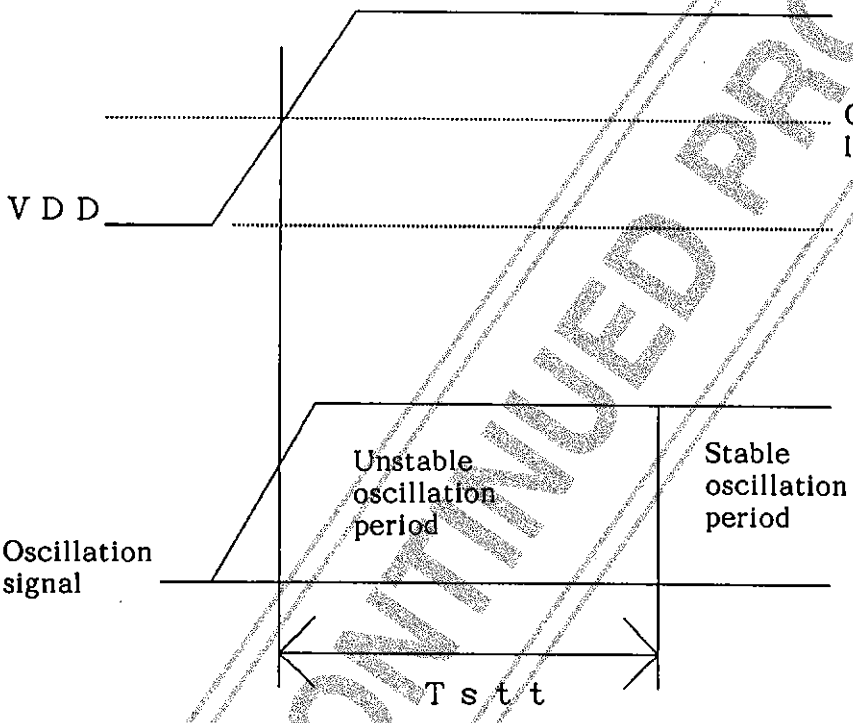
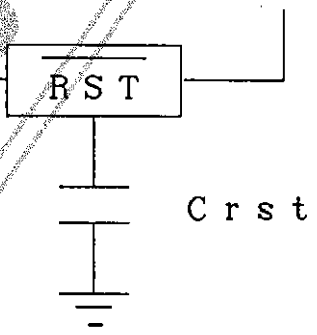


Figure 4. Oscillation start time period



Note: The reset time period will be 10 milliseconds to 100 milliseconds on the assumption that the rise time at power on is zero and the Crst is 0.1 micro Farad. The reset time period should be longer than the CF/RC oscillation start time period (Tsst). With this always in mind, select the Crst constant.

Figure 5. Reset circuit

Instruction set for the LC86104A microcomputer

Abbreviations

ACC(A)	: Accumulator
B	: B register
CY(C)	: Carry flag
AC	: Auxiliary carry flag
OV	: Overflow flag
PC	: Program counter
ROM	: Program memory
RAM	: Data memory
SFR	: Special function register
PSW	: Program status word
TRL	: Table read register low-order byte
TRH	: Table read register high-order byte
SP	: Stack pointer
P1	: Port 1
P2	: Port 2
P3	: Port 3
P4	: Port 4
Ri	: Indirect address register within the current bank (part of the internal RAM)
Rj	: Indirect address register within the current bank (part of the internal RAM)
d9	: Direct addressing data
#i8	: Immediate data
b3	: Bit addressing data
r8	: Relative addressing data
r16	: Relative addressing data
a12	: Absolute addressing data
a16	: Absolute addressing data
( )	: Indicates the contents.
←	: Data transfer and its direction
∧	: Logical AND
∨	: Logical OR
∀	: Exclusive OR
+	: Addition
-	: Subtraction
Set	: Sets a bit to 1.
Reset	: Sets a bit to 0.
Bit	: Binary digit contents (0 or 1)
Clear	: Sets all bits to 0.
Carry	: Carry for upper digits
Borrow	: Borrow from upper digits
Number of bytes (BYTES)	: One byte has 8 bits. Indicates the number of units of an instruction.
Number of cycles (CYCLES)	: Indicates the number of CPU basic instruction cycles required by the execution of an instruction.

■Arithmetic operations instruction

MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV
ADD #i8	1 0 0 0 0 0 0 1 i7i6i5i4i3i2ili0	2	1	(A)←(A)+#i8	○	○	○
ADD d9	1 0 0 0 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(A)+(d9)	○	○	○
ADD @Ri	1 0 0 0 0 1ili0	1	1	(A)←(A)+((Ri)) i:0,1,2,3	○	○	○
ADDC #i8	1 0 0 1 0 0 0 1 i7i6i5i4i3i2ili0	2	1	(A)←(A)+(C)+#i8	○	○	○
ADDC d9	1 0 0 1 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(A)+(C)+(d9)	○	○	○
ADDC @Ri	1 0 0 1 0 1ili0	1	1	(A)←(A)+(C)+((Ri)) i:0,1,2,3	○	○	○
SUB #i8	1 0 1 0 0 0 0 1 i7i6i5i4i3i2ili0	2	1	(A)←(A)-#i8	○	○	○
SUB d9	1 0 1 0 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(A)-(d9)	○	○	○
SUB @Ri	1 0 1 0 0 1ili0	1	1	(A)←(A)-((Ri)) i:0,1,2,3	○	○	○
SUBC #i8	1 0 1 1 0 0 0 1 i7i6i5i4i3i2ili0	2	1	(A)←(A)-(C)-#i8	○	○	○
SUBC d9	1 0 1 1 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(A)-(C)-(d9)	○	○	○
SUBC @Ri	1 0 1 1 0 1ili0	1	1	(A)←(A)-(C)-((Ri)) i:0,1,2,3	○	○	○
INC d9 *1	0 1 1 0 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(d9)←(d9)+1			
INC @Ri *1	0 1 1 0 0 1ili0	1	1	((Ri))←((Ri))+1 i:0,1,2,3			
DEC d9 *1	0 1 1 1 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(d9)←(d9)-1			
DEC @Ri *1	0 1 1 1 0 1ili0	1	1	((Ri))←((Ri))-1 i:0,1,2,3			
MUL	0 0 1 1 0 0 0 0	1	4	(B),(A)←(A)X(B)	○		○
DIV	0 1 0 0 0 0 0 0	1	4	(B),(A)←(A)/(B)	○		○

■Logical operations instruction

MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV
AND #i8	1 1 1 0 0 0 0 1 i7i6i5i4i3i2ili0	2	1	(A)←(A)∧#i8			
AND d9	1 1 1 0 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(A)∧(d9)			
AND @Ri	1 1 1 0 0 1ili0	1	1	(A)←(A)∧((Ri)) i:0,1,2,3			
OR #i8	1 1 0 1 0 0 0 1 i7i6i5i4i3i2ili0	2	1	(A)←(A)∨#i8			
OR d9	1 1 0 1 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(A)∨(d9)			
OR @Ri	1 1 0 1 0 1ili0	1	1	(A)←(A)∨((Ri)) i:0,1,2,3			
XOR #i8	1 1 1 1 0 0 0 1 i7i6i5i4i3i2ili0	2	1	(A)←(A)⊻#i8			
XOR d9	1 1 1 1 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(A)⊻(d9)			
XOR @Ri	1 1 1 1 0 1ili0	1	1	(A)←(A)⊻((Ri)) i:0,1,2,3			
ROL	1 1 1 0 0 0 0 0	1	1	←A7←A6←A5←A4← ↓ ↑ →A0→A1→A2→A3→			
ROLC	1 1 1 1 0 0 0 0	1	1	←C←A7←A6←A5←A4← ↓ ↑ → →A0→A1→A2→A3→	○		
ROR	1 1 0 0 0 0 0 0	1	1	→A7→A6→A5→A4→ ↑ ↓ ←A0←A1←A2←A3←			
RORC	1 1 0 1 0 0 0 0	1	1	→C→A7→A6→A5→A4→ ↑ ↓ ← ←A0←A1←A2←A3←	○		

■ Data transfer instruction

MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV
LD d9	0 0 0 0 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(A)←(d9)			
LD @Ri	0 0 0 0 0 1i1i0	1	1	(A)←((Ri)) i:0,1,2,3			
ST d9	0 0 0 1 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(d9)←(A)			
ST @Ri	0 0 0 1 0 1i1i0	1	1	((Ri))←(A) i:0,1,2,3			
MOV #i8,d9	0 0 1 0 0 0 1d8 d7d6d5d4d3d2d1d0 i7i6i5i4i3i2i1i0	3	2	(d9)←#i8			
MOV #i8,@Rj	0 0 1 0 0 1j1j0 i7i6i5i4i3i2i1i0	2	1	((Rj))←#i8 j:0,1,2,3			
LDC	1 1 0 0 0 0 0 1	1	2	(A)←((TRR+A)) [ROM]			
PUSH d9	0 1 1 0 0 0 0d8 d7d6d5d4d3d2d1d0	2	2	(SP)←(SP)+1,((SP))←(d9)			
POP d9	0 1 1 1 0 0 0d8 d7d6d5d4d3d2d1d0	2	2	(d9)←((SP)),(SP)←(SP)-1			
XCH d9	1 1 0 0 0 0 1d8 d7d6d5d4d3d2d1d0	2	1	(d9)↔(A)			
XCH @Ri	1 1 0 0 0 1i1i0	1	1	((Ri))↔(A) i:0,1,2,3			

■Branch instruction

MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV
JMP a12	0 0 1 a11 1 a10 a9 a8 a7a6a5a4a3a2a1a0	2	2	(PC)←(PC)+2: (PC11-00)←a12			
JMPF a16	0 0 1 0 0 0 0 1 a15 a14 a13 a12 a11 a10 a9 a8 a7a6a5a4a3a2a1a0	3	2	(PC)←a16			
BR r8	0 0 0 0 0 0 0 1 r7r6r5r4r3r2r1r0	2	2	(PC)←(PC)+2: (PC)←(PC)+r8			
BRF r16	0 0 0 1 0 0 0 1 r7r6r5r4r3r2r1r0 r15 r14 r13 r12 r11 r10 r9 r8	3	4	(PC)←(PC)+3: (PC)←(PC)-1+r16			
BZ r8	1 0 0 0 0 0 0 0 r7r6r5r4r3r2r1r0	2	2	(PC)←(PC)+2: if (A)=0, then (PC)←(PC)+r8			
BNZ r8	1 0 0 1 0 0 0 0 r7r6r5r4r3r2r1r0	2	2	(PC)←(PC)+2: if (A)≠0, then (PC)←(PC)+r8			
BP d9.b3.r8	0 1 1d8 1b2b1b0 d7d6d5d4d3d2d1d0 r7r6r5r4r3r2r1r0	3	2	(PC)←(PC)+3: if (d9.b3)=1, then (PC)←(PC)+r8			
BN d9.b3.r8	1 0 0d8 1b2b1b0 d7d6d5d4d3d2d1d0 r7r6r5r4r3r2r1r0	3	2	(PC)←(PC)+3: if (d9.b3)≠1, then (PC)←(PC)+r8			
DBNZ d9.r8 *	0 1 0 1 0 0 1d8 d7d6d5d4d3d2d1d0 r7r6r5r4r3r2r1r0	3	2	(PC)←(PC)+3: (d9)=(d9)-1: if (d9)≠0, then (PC)←(PC)+r8			
DBNZ @Ri.r8 *	0 1 0 1 0 1i1i0 r7r6r5r4r3r2r1r0	2	2	(PC)←(PC)+2: ((Ri))=((Ri))-1 i=0,1,2,3: if (d9)≠0, then (PC)←(PC)+r8			

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MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV

BE #i8, r8	0 0 1 1 0 0 0 1
	i7i6i5i4i3i2ili0
	r7r6r5r4r3r2r1r0
		3	2	(PC)←(PC)+3:
				if (A)=#i8,
				then (PC)←(PC)+r8:
				if (A)<#i8,
				then C←1 else C←0:
					○		

BE d9, r8	0 0 1 1 0 0 1d8
	d7d6d5d4d3d2d1d0
	r7r6r5r4r3r2r1r0
		3	2	(PC)←(PC)+3:
				if (A)=(d),
				then (PC)←(PC)+r8:
				if (A)<(d),
				then C←1 else C←0:
					○		

BE @Rj, #i8, r8	0 0 1 1 0 1j1j0
	i7i6i5i4i3i2ili0
	r7r6r5r4r3r2r1r0
		3	2	(PC)←(PC)+3:
				if ((Rj))=#i8,
				then (PC)←(PC)+r8:
				if ((Rj))<#i8,
				then C←1 else C←0:
					○		

BNE #i8, r8	0 1 0 0 0 0 0 1
	i7i6i5i4i3i2ili0
	r7r6r5r4r3r2r1r0
		3	2	(PC)←(PC)+3:
				if (A)≠#i8,
				then (PC)←(PC)+r8:
				if (A)<#i8,
				then C←1 else C←0:
					○		

BNE d9, r8	0 1 0 0 0 0 1d8
	d7d6d5d4d3d2d1d0
	r7r6r5r4r3r2r1r0
		3	2	(PC)←(PC)+3:
				if (A)≠(d),
				then (PC)←(PC)+r8:
				if (A)<(d),
				then C←1 else C←0:
					○		

BNE @Rj, i8, r8	0 1 0 0 0 1j1j0
	i7i6i5i4i3i2ili0
	r7r6r5r4r3r2r1r0
		3	2	(PC)←(PC)+3:
				if ((Rj))≠#i8,
				then (PC)←(PC)+r8:
				if ((Rj))<#i8,
				then C←1 else C←0:
					○		

Subroutine instruction

MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV
CALL a12	0 0 0 a11 1 a10 a9 a8 a7a6a5a4a3a2a1a0	2	2	(PC)←(PC)+2: (SP)←(SP)+1: ((SP))←PC7-0: (SP)←(SP)+1: ((SP))←PC15-8: (PC11-0)←a12			
CALLF a16	0 0 1 0 0 0 0 0 a15 a14 a13 a12 a11 a10 a9 a8 a7a6a5a4a3a2a1a0	3	2	(PC)←(PC)+3: (SP)←(SP)+1: ((SP))←PC7-0: (SP)←(SP)+1: ((SP))←PC15-8: (PC)←a16			
CALLR a16	0 0 0 1 0 0 0 0 a7a6a5a4a3a2a1a0 a15 a14 a13 a12 a11 a10 a9 a8	3	4	(PC)←(PC)+3: (SP)←(SP)+1: ((SP))←PC7-0: (SP)←(SP)+1: ((SP))←PC15-8: (PC)←(PC)-1+r16			
RET	1 0 1 0 0 0 0 0	1	2	(PC15-8)←((SP)): (SP)←(SP)-1: (PC7-0)←((SP)): (SP)←(SP)-1			
RETI	1 0 1 1 0 0 0 0	1	2	(PC15-8)←((SP)): (SP)←(SP)-1: (PC7-0)←((SP)): (SP)←(SP)-1			

Bit manipulation instruction

MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV
CLR1 d9.b3	1 1 0d8 1b2b1b0	2	1	(d9.b3)←0			
*	d7d6d5d4d3d2d1d0						
SET1 d9.b3	1 1 1d8 1b2b1b0	2	1	(d9.b3)←1			
*	d7d6d5d4d3d2d1d0						
NOT1 d9.b3	1 0 1d8 1b2b1b0	2	1	(d9.b3)←$\overline{(d9.b3)}$			
*	d7d6d5d4d3d2d1d0						

■ Other instructions

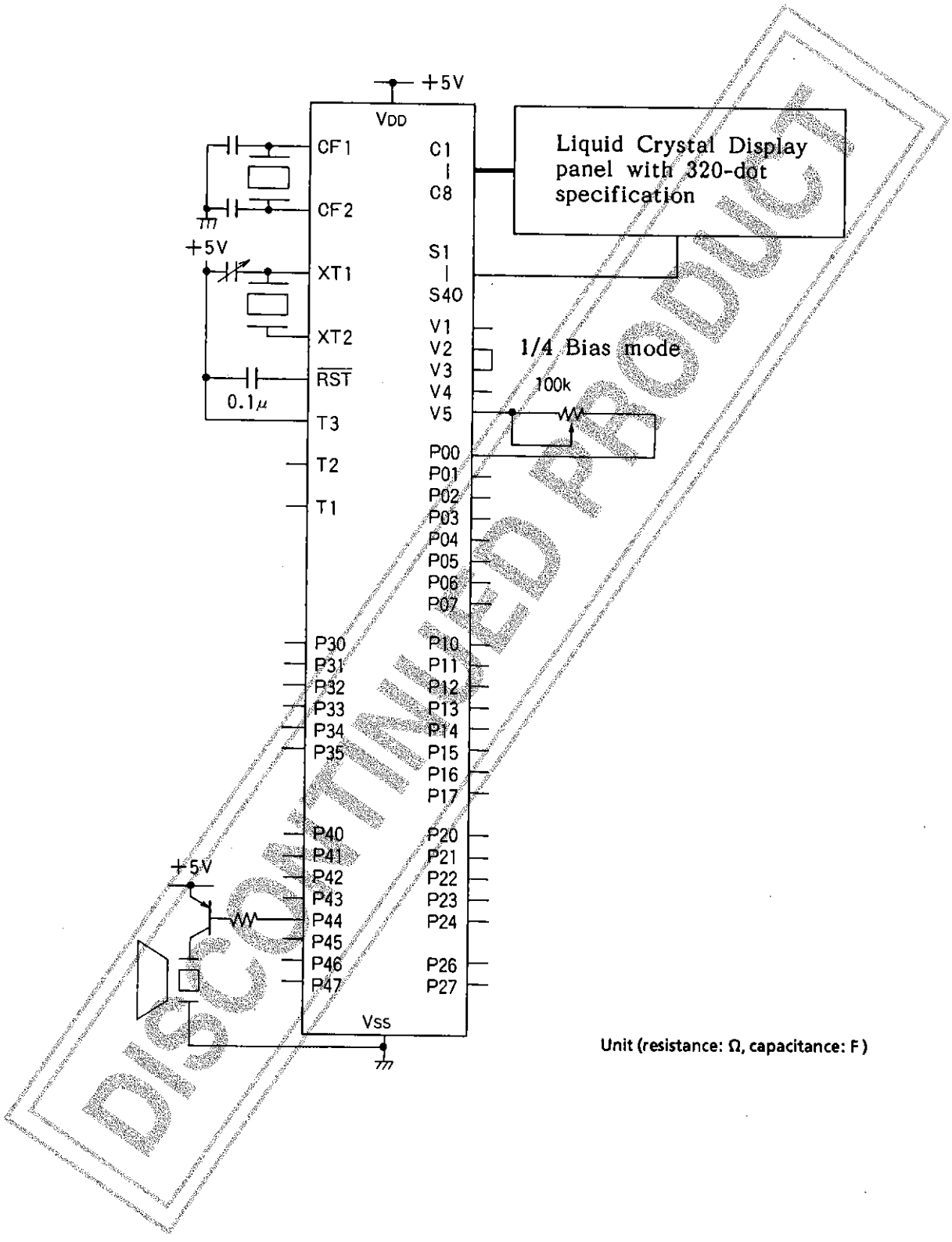
MNEMONIC	INSTRUCTION CODE	BYTES	CYCLES	DESCRIPTION	PSW		
					CY	AC	OV
NOP	0 0 0 0 0 0 0 0	1	1				

Note: If ports are addressed by the instructions marked with asterisks in byte units or bit units, their port latches will be selected. If ports are addressed by other instructions, external input signals to them will be selected.

Instruction map for the LC86104A microcomputer

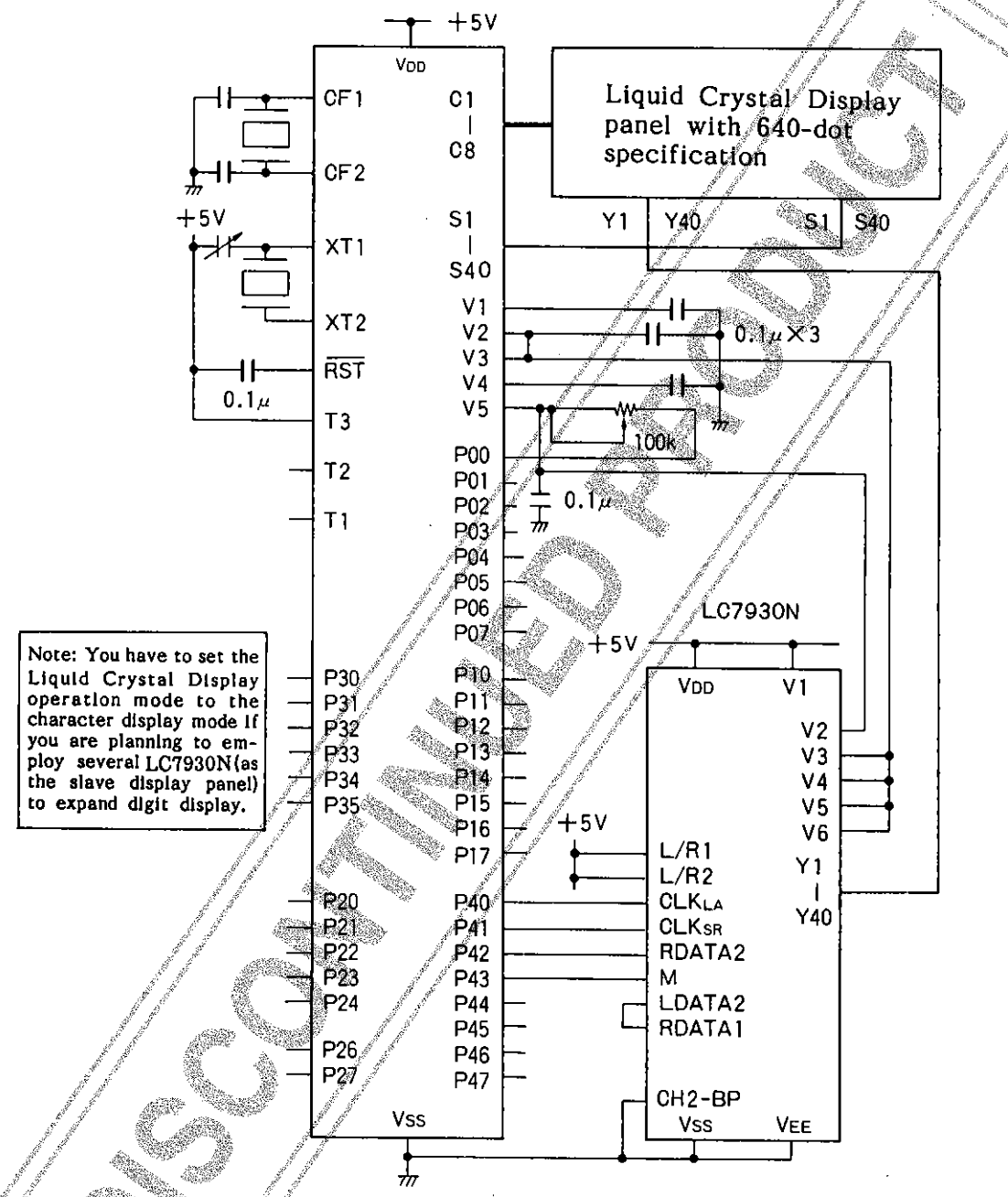
LOW BYTE / HIGH BYTE	0	1	2, 3	4-7	8-F
0	NOP	BR r8	LD d9	LD @Ri	CALL a12
1	CALLR r16	BRF r16	ST d9	ST @Ri	
2	CALLF a16	JMPF a16	MOV #i8, d9	MOV #i8, @Ri	JMP a12
3	MUL	BE #i8, r8	BE d9, r8	BE @Ri, #i8, r8	
4	DIV	BNE #i8, r8	BNE #d9, r8	BNE @Ri, #i8, r8	———
5	———	———	DBNZ d9, r8	DBNZ @Ri, r8	
6	PUSH d9		INC d9	INC @Ri	BP d9, b3, r8
7	POP d9		DEC d9	DEC @Ri	
8	BZ r8	ADD #i8	ADD d9	ADD @Ri	BN d9, b3, r8
9	BNZ r8	ADDC #i8	ADDC d9	ADDC @Ri	
A	RET	SUB #i8	SUB d9	SUB @Ri	NOT1 d9, b3
B	RETI	SUBC #i8	SUBC d9	SUBC @Ri	
C	ROR	LDC	XCH d9	XCH @Ri	CLR1 d9, b3
D	RORC	OR #i8	OR d9	OR @Ri	
E	ROL	AND #i8	AND d9	AND @Ri	SET1 d9, b3
F	ROLC	XOR #i8	XOR d9	XOR @Ri	

Example application circuit (1)



Unit (resistance: Ω, capacitance: F)

Example application circuit (2)



Unit (resistance: Ω, capacitance: F)