Data Sheet No. PD-6.015

International
IOR Rectifier

IR8400P

QUAD HIGH SIDE SWITCH

General Description

The IR8400P is a fully protected quad high side switch. It contains four common-drain DMOS N-channel power switches, each capable of switching a ground referenced load to a common positive power supply. The switches are fully protected from excessive voltage, current and temperature and are designed to drive resistive, inductive or capacitive loads in controlled manner. An instantaneous power sensing circuit calculates the product of the voltage across and the current through each DMOS switch and limits the power to a safe level. The maximum junction temperature, and thus power dissipation, is limited internally by an over-temperature shutdown circuit.

The device can be operated in a 'sleep' stand by mode to conserve power in battery driven applications. Separate ON/OFF control of each switch is provided through standard LSTTL/CMOS logic compatible inputs. A serial data interface is built in to provide extensive diagnostic information back to the microcontroller. Two direct-output error flags provide immediate indication of a general system fault and excessive operating temperature.

The IR8400P is packaged in a special leadframe that helps dissipate heat through the two ground pins on each side of the standard dual-in-line package. Overall junction-to-ambient thermal resistance can be reduced by the use of copper foil of a printed circuit board as heat-sinking pad.

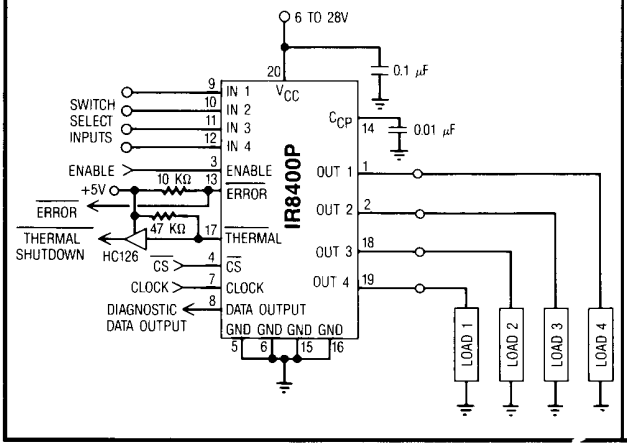
Applications

- Relay and solenoid drivers
- Lamp drivers
- Automotive fuel injector drivers
- Power supply output switching
- Motor drivers

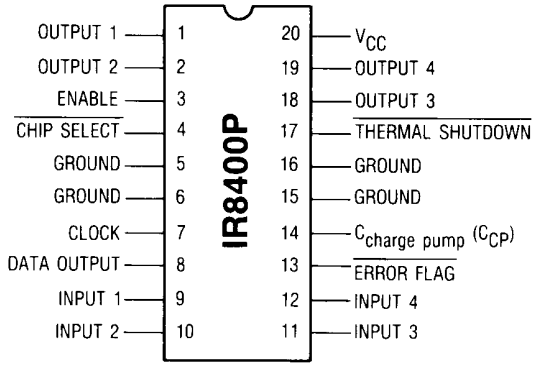
Features

- Four independent outputs with >3A peak, 1A continuous current capability
- 1.3Ω maximum ON resistance over operating temperature range
- True instantaneous power limit at 15W per switch
- High survival voltage (60V DC, 80V transient)
- –5V output clamp for discharging inductive loads
- Shorted load (to ground and supply) protection
- Two step over-temperature warning and shutdown
- Over-voltage shutdown at V_{CC} > 35V
- <10 μA supply current in "sleep" mode
- LSTTL/CMOS compatible logic inputs and outputs
- Serial data interface for 11 diagnostic checks:
  - Switch ON/OFF status
  - Open or shorted load
  - Operating temperature
  - Excessive supply voltage
- Two direct-output error flags
- Junction-to-case thermal resistance at 20°C/W

Typical Connection



Pinout Assignment



For mechanical specifications see back page

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur.

ESD is rated using the Human body model with 100 pF discharged through 1.5k resistor.

The maximum power dissipation is rated using the test condition of sufficient heatsinking such that T_C = 25°C.

The maximum allowable power dissipation is limited internally through thermal shutdown circuit if the junction temperature exceeds a certain limit.

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{CC}	Transient Supply Voltage		80	V	Pin 20, t = 10 ms
	Continuous Supply Voltage	-0.5	60		PIn 20
I_O	Transient Output Current (Each Switch)		3.75	A	Pin 1, 2, 18, 19
	Transient Output Current (Total, All Switch)		6		Pin 1 + 2 + 18 + 19
	Steady State Output Current (Each Switch)		1		Pin 1, 2, 18, 19
V_{IN}	Channel Logic Input Voltage	-0.3	16	V	Pin 9, 10, 11, 12
V_{EN}	Enable Logic Input Voltage	-0.3	16		Pin 3
V_{DG}	Diagnostic Logic Input Voltage	-0.3	6		Pin 4, 7
V_{ERR}	Error Flag Voltage		16		Pin 13
ESD	Electrostatic Discharge Susceptibility		2000		Pin 4-7, 9-17, 20
			1000		Pin 3, 8
			500		Pin 1, 2, 18, 19
P_D	Power Dissipation (Internally Limited)		5	W	T_C = 25°C, also see Fig. 13
T_j	Junction Temperature		150	°C	
T_S	Storage Temperature	-65	150		
T_L	Lead Temperature		260		Soldering, 10 seconds

Recommended Operating Conditions

Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits.

For guaranteed specifications and test conditions, see the Electrical Characteristics.

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{CC}	Supply Voltage	6	28	V	
T_A	Ambient Temperature	-40	125	°C	

Static Electrical Characteristics

V_{CC} = 12V, C_{CP} = 0.01 μF, unless otherwise specified.

All tests performed in DC conditions except where pulse test techniques are indicated with pulse width <5 ms and duty cycle <1%.

Symbol	Parameter	Min	Typ	Max	Min	Max	Units	Test Conditions	Reference
Power Supply (Pin 20)			$T_A = T_j$ = 25°C		T_A = -40 to 125°C				
I_{CC}	Supply Current		0.04	10			μA	V_{EN} = 0V	Fig. 1
			7.5	15			mA	V_{EN} = 5V, V_{IN}'s = 0V	
			7.5	15				V_{EN} = 5V, V_{IN}'s = 5V, Open Loads	
OV_{CC}	Supply Over-Voltage Shutdown Threshold		35	40			V		
	Supply Over-Voltage Shutdown Hysteresis		0.75						
Power Output (Pin 1, 2, 18, 19)									
R_{ON}	Output Switch On Resistance		0.8			1.3	Ω	I_O = 1A, Pulse Test	Fig. 2
I_{Olk}	Output Leakage		0.01	10			μA	V_{EN} = 5V, V_{IN}'s = 0V	
I_{Osc}	Output Short Circuit Current	0.8	1.2				A	V_{CC} = 12V, Pulse Test	Fig. 3
			2.4					V_{CC} = 6V, Pulse Test	Fig. 4
			0.6					V_{CC} = 28V, Pulse Test	Fig. 4
I_{Omax}	Maximum Output Current		3.75					$V_{CC} - V_O$ = 4V, Pulse Test	Fig. 4
V_{Oerr}	Shorted Load Error Threshold Voltage		4.1				V	Fig. 5	
I_{Oerr}	Open Load Error Threshold Current		150				μA		
V_{O-}	Output Voltage Negative Clamp		-5				V	I_O = 1A, Pulse Test	Fig. 6
Logic Functions									
V_{IH}	Logic "1" Input Voltage				2		V	Pin 3, 4, 7, 9, 10, 11, 12	Fig. 7
V_{IL}	Logic "0" Input Voltage					0.8		Pin 3, 4, 7, 9, 10, 11, 12	
R_{IN}	Channel Input Resistance		75		25		kΩ	Pin 9, 10, 11, 12	Fig. 8
I_{EN}	Enable Input Current		12			25	μA	Pin 3 = 2.4V	
I_{DGIN}	Diagnostic Logic "1" Input Current		0.001			1		Pin 4, 7	
	Diagnostic Logic "0" Input Current		-0.001			-1		Pin 4, 7	
V_{DGO}	Diagnostic Output Voltage		4.4		2.4		V	Pin 8 = -360 μ	
			5.1		4.5	5.5		Pin 8 = -10 μA	
I_{DGO}	Diagnostic Hi-Z State Output Current		0.05	10			μA	Pin 8 = 5V	
			-0.05	-10				Pin 8 = 0V	
I_{err}	Error Flag Leakage Current		0.001	10				Pin 13 = 12V	
	Error Flag Sink Current		4		1.6		mA	Pin 13 = 0.8V	Fig. 9
I_{TSD}	Thermal Shutdown Output Source Current	3	5				μA	Pin 17 = 2.4V	
	Thermal Shutdown Output Sink Current	250	360					PIn 17, 0.8V	

Dynamic Electrical Characteristics

V_{CC} = 12V, C_{CP} = 0.01 μF, unless otherwise specified.
See Timing Specification Diagram for the measurement thresholds and definitions.

		$T_A = T_j$ = 25°C			T_A = -40 to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Units**	**Test Conditions**	**Reference**
t_{don}	Channel Turn-On Delay		5	10				V_{EN} = 5V, I_O = 1A	Fig. 10
t_r	Channel Turn-On Rise Time		7	15				I_O = 1A	Fig. 11
t_{doff}	Channel Turn-Off Delay		0.5	2				V_{EN} = 5V, I_O = 1A	Fig. 12
t_f	Channel Turn-Off Fall Time		0.15	1				I_O = 1A	
t_{en}	Enable Turn-On Delay Time		30	50			μs	Pin 9 = 5V, Pin 3 to Pin 1	
t_{err}	Error Flag Reporting Delay		75	150				V_{EN} = 5V, Pin 9 to Pin 13 w/Pin 1 Open Load	
t_{ds}	Diagnostic Data Set-Up Time	0.5						C_L = 30 pF	
t_{1H},t_{0H}	Diagnostic Data Hi-Z Enable Time		2						
f_{clk}	Diagnostic Data Clock Frequency			1			MHz		

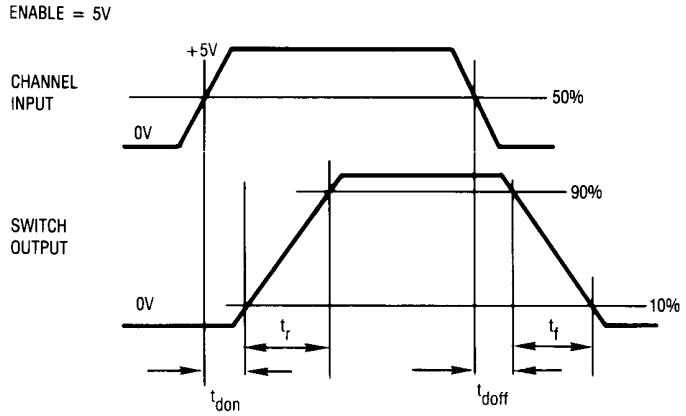
Thermal Characteristics

The junction to ambient thermal resistance rating is a function of the amount of heatsinking provided. Figure 14 shows a typical characteristics of (θ_{ja}) as function of heatsinking pad size.

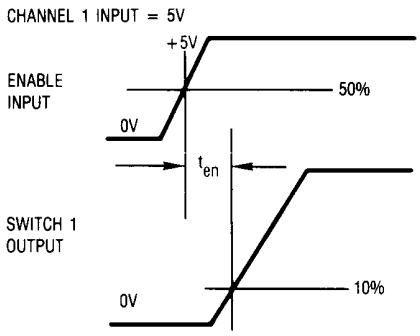
		$T_A = T_j$ = 25°C			T_A = -40 to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Units**	**Test Conditions**	**Reference**
(θ_{jc})	Thermal Resistance, Junction to Case		20				°C/W	Case = Pin 5, 6, 15, 16	
(θ_{ja})	Thermal Resistance, Junction to Ambient		60					No Heatsink	
T_{jw}	Thermal Warning Temperature		145				°C	Pin 13 <0.8V	
T_{jsd}	Thermal Shutdown Temperature		170					Pin 17 <0.8V	

Timing Specification Diagram

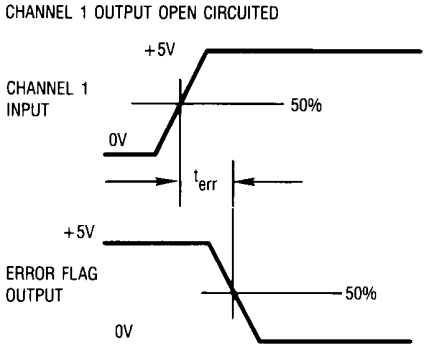
SWITCH TURN ON/OFF



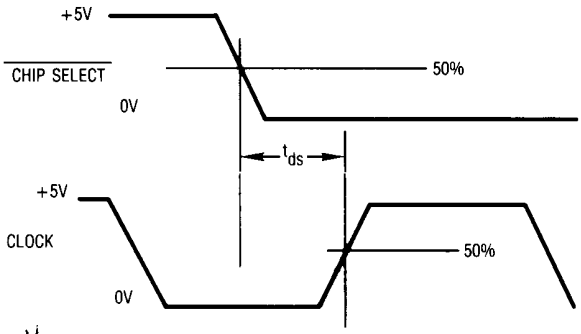
ENABLE TURN-ON



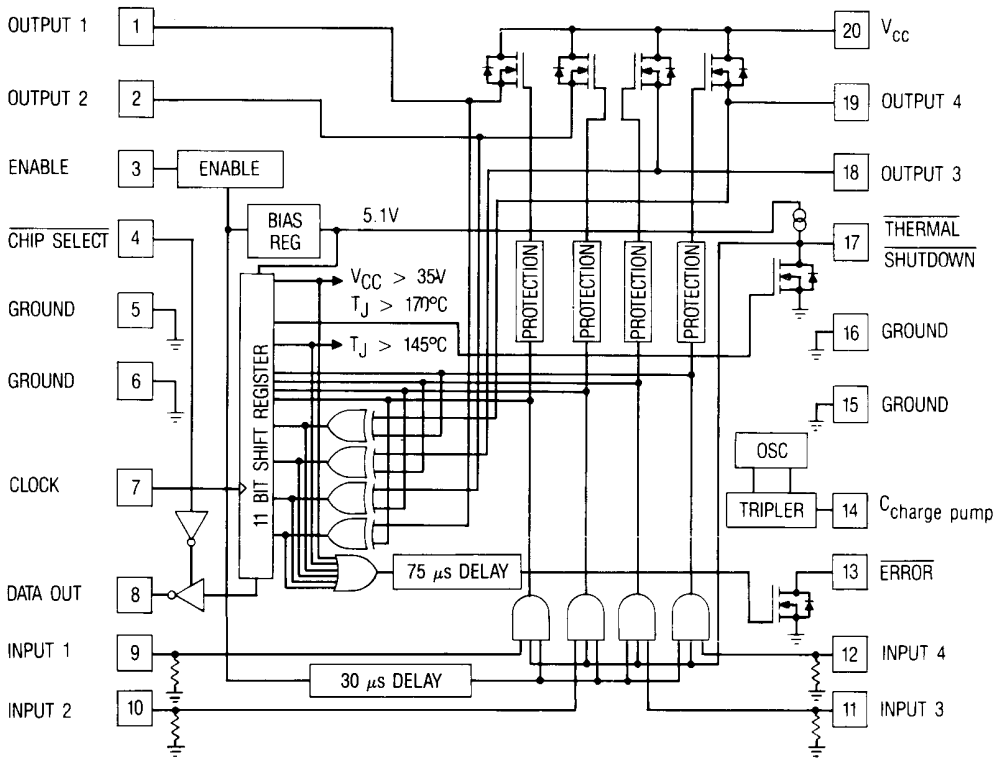
ERROR REPORTING DELAY



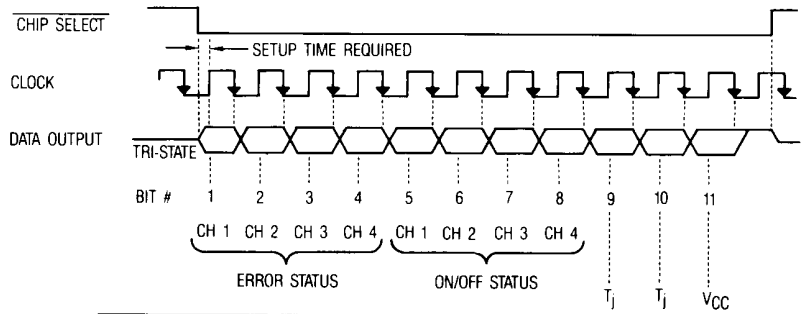
DATA SET-UP TIME



Functional Block Diagram



Serial Diagnostic Data Assignments



LOGIC 1	LOAD OK	SWITCH OFF	< 145°C	< 170°C	< 35V
LOGIC 0	LOAD ERROR	SWITCH ON	> 145°C	> 170°C	> 35V

Truth Table

Enable Input (Pin 3)	Chip Select Input (Pin 4)	Switch Control Input (Pins 8, 9, 10, 11)	Error Flag Output (Pin 13)	Thermal SD Output (Pin 17)	Condition
0	X	X	0	0	'Sleep' Mode, I_{supply} < 10 µA
1	X	0	1	1	Selected switch is OFF
1	X	1	1	1	Selected switch is ON Normal Operation
1	X	0	0	1	Switch is OFF, but; a) Load is open circuited, or b) Load is shorted to V_{CC}, or c) T_j > 145°C, or d) V_{CC} > 35V
1	X	1	0	1	Switch is ON, but; a) Load is shorted to ground, or b) Switch is in power limit, or c) T_j > 145°C, or d) V_{CC} > 35V and switch is actually OFF
1	X	1	0	0	T_j > 170°C, all switches are OFF
1	1	X	X	X	Data Output pin is Hi-Z State
1	0	X	X	X	Data Output pin is enabled and ready to output diagnostic information

Typical Performance Characteristics

V_{CC} = 12V, Temperature is the junction temperature unless otherwise noted.

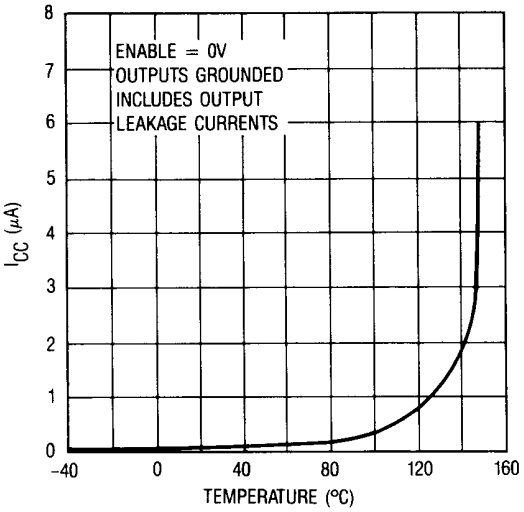


Fig. 1 — 'Sleep' Mode Supply Current vs. Temperature

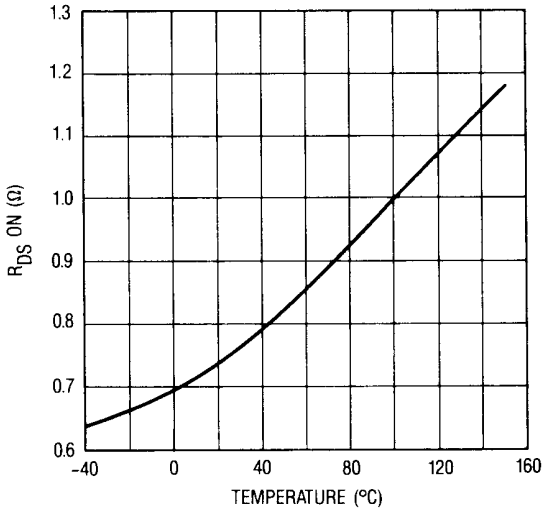


Fig. 2 — Switch ON Resistance vs. Temperature

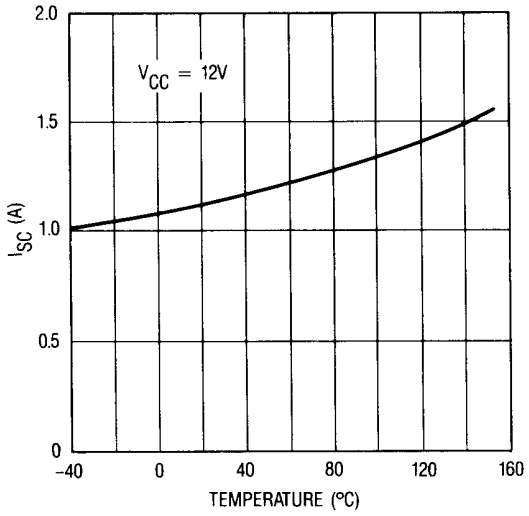


Fig. 3 — Short Circuit Current vs. Temperature

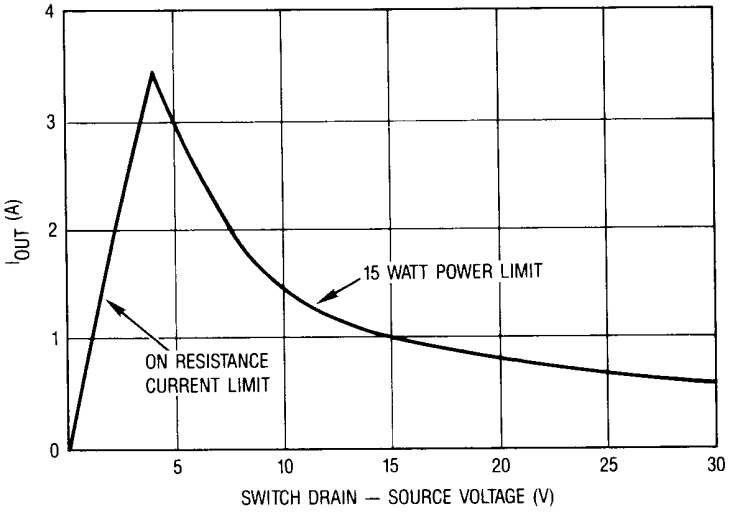


Fig. 4 — Maximum Output Transient Current vs. Drive-to-Source Voltage

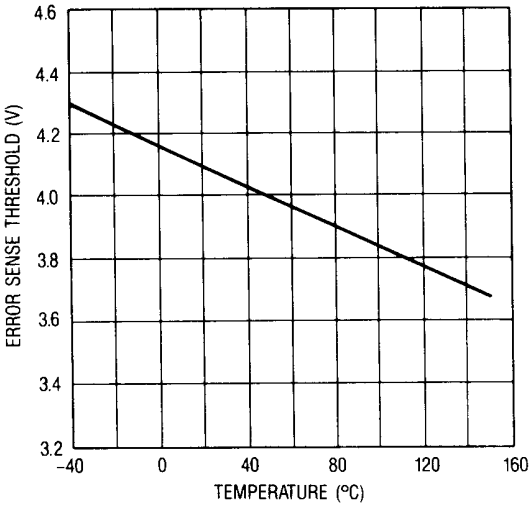


Fig. 5 — Shorted Load Error Threshold Voltage vs. Temperature

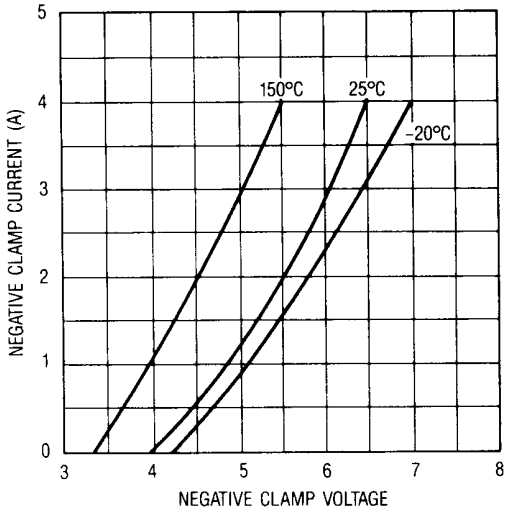


Fig. 6 — Output Voltage Characteristics vs. Temperature

Typical Performance Characteristics (continued)

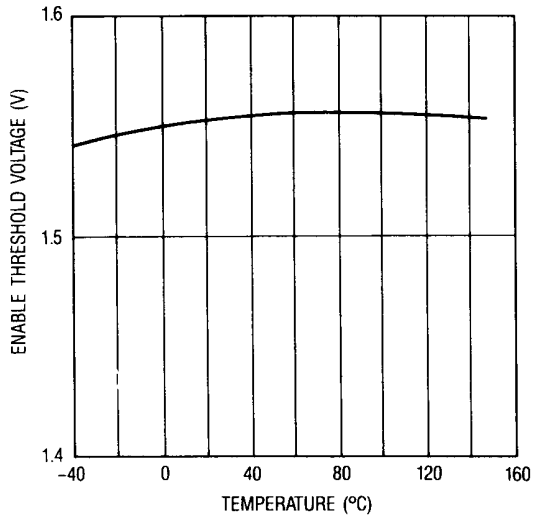


Fig. 7 — Enable Threshold Voltage vs. Temperature

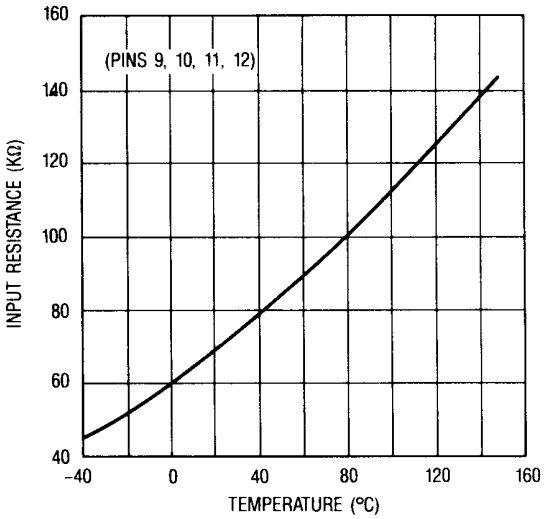


Fig. 8 — Switch Select Logic Input Resistance vs. Temperature

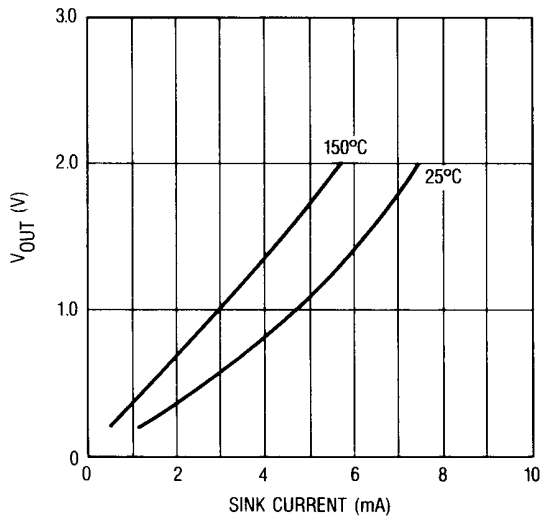


Fig. 9 — Error Flag Voltage vs. Sink Current

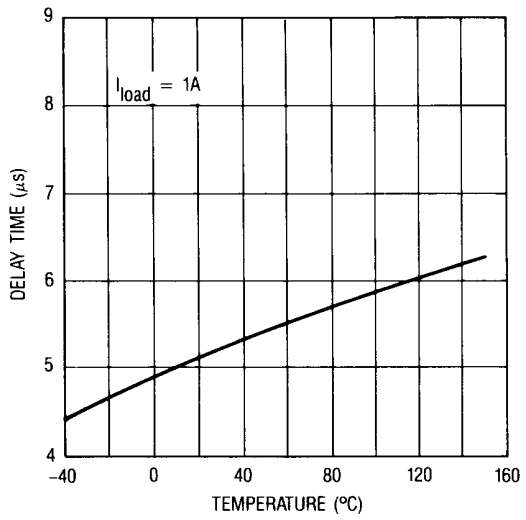


Fig. 10 — Turn ON Delay Time vs. Temperature

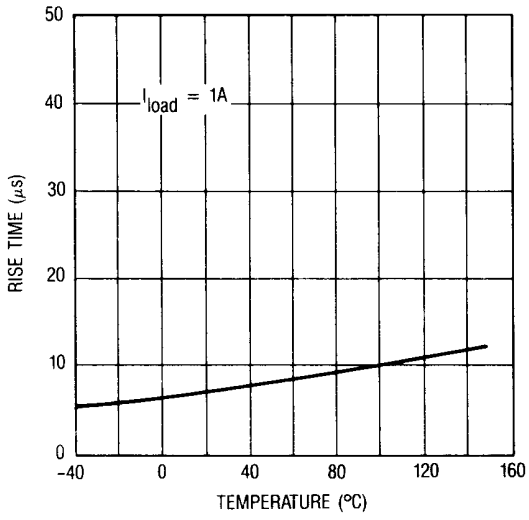


Fig. 11 — Turn ON Rise Time vs. Temperature

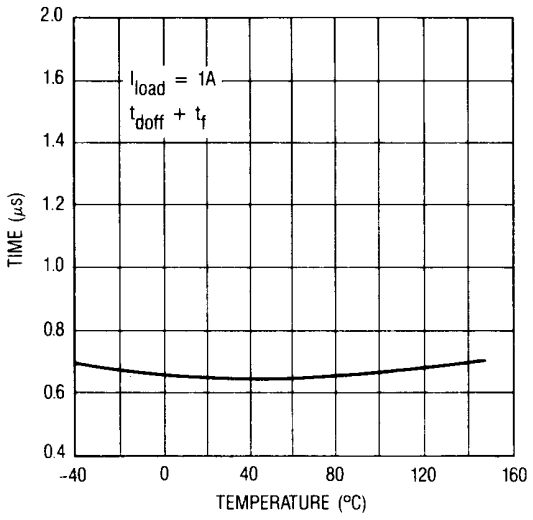


Fig. 12 — Turn OFF Time vs. Temperature

Typical Performance Characteristics (continued)

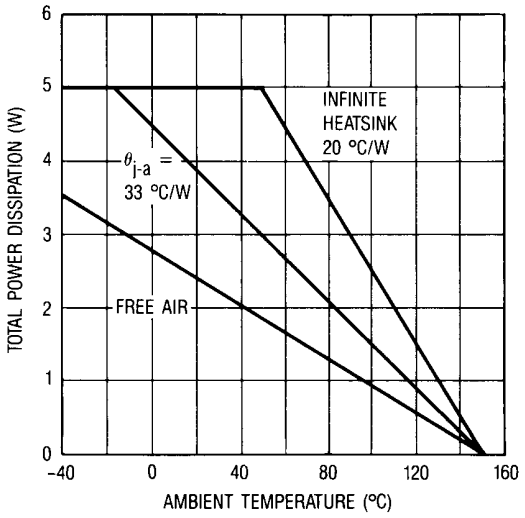


Fig. 13a — Maximum Power Dissipation vs. Ambient Temperature

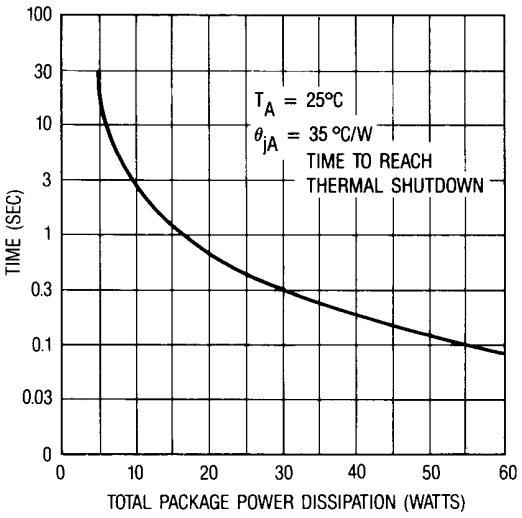


Fig. 13b — Maximum Transient Power Dissipation vs. Time

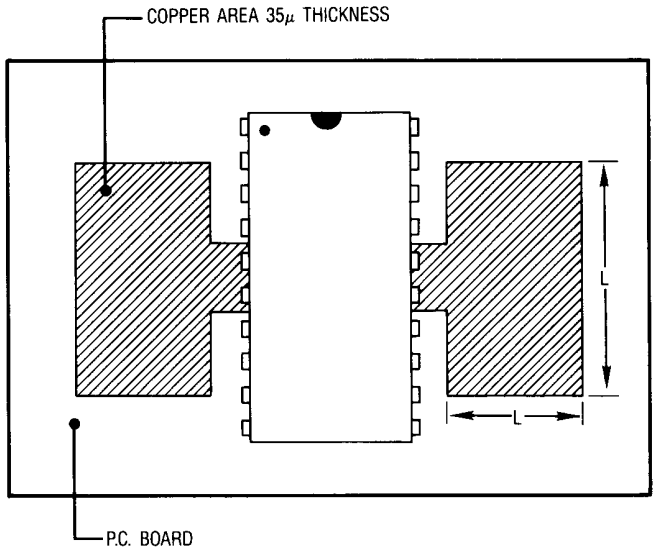


Fig. 14a — Recommended PC Board Layout to Reduce the Thermal Resistance from Junction-to-Ambient

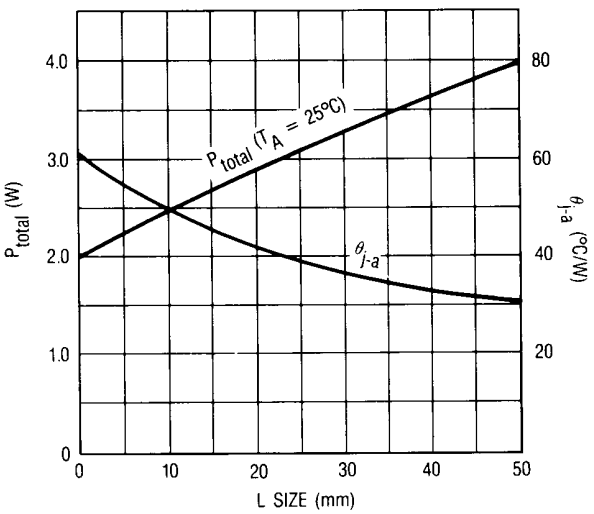


Fig. 14b — Maximum Power Dissipation and Junction to Ambient Thermal Resistance vs. Heatsinking Pad Size

Applications Information

Basic Operation

High-side switches are used extensively in automotive and industrial applications to switch power to ground referenced loads. The major advantage of using a high-side switch, as opposed to low-side switch, is to protect the load from being energized in the event that the load wire is inadvertently shorted to ground as shown in Figure 15. A high-side switch can sense a shorted condition and open the power switch to disable the load and eliminate the excessive current drain on the power supply. The IR8400P can control and protect up to four separate ground referenced loads.

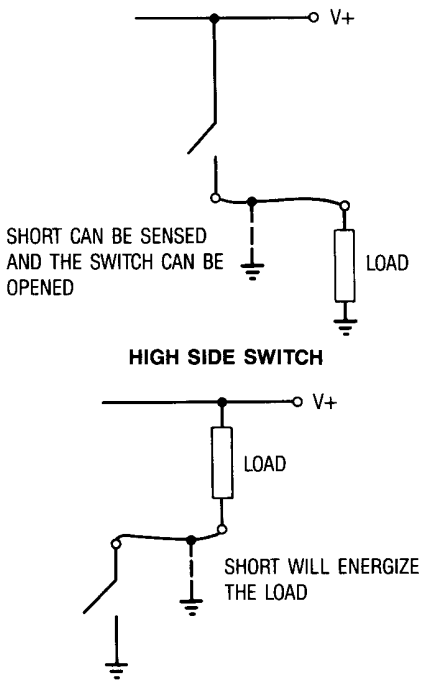


Fig. 15 — High-Side vs. Low-Side Drive Switch

The IR8400P combines low voltage CMOS logic control circuitry with a high voltage DMOS process. Each DMOS power switch has an individual ON/OFF control input. When commanded ON, the output of the switch will connect the load to the V_{CC} supply through a maximum resistance of 1.3Ω (the ON resistance of the DMOS switch). The voltage applied to the load will depend upon the load current and the designed current capability of the IR8400P. When a switch is commanded OFF, the load will be disconnected from the supply except for a small leakage current of typically less than 0.04 μA.

The IR8400P can be continually connected to a live power source, a car battery for example, while drawing less than 10 μA from the power source when put into a 'sleep' condition. This 'sleep' mode is enacted by taking Enable Input (pin 3) low. During this mode the supply current for the device is typically only 0.04 μA. Special low current consumption standby circuitry is used to hold the DMOS switches OFF with good noise immunity. When in the 'sleep' mode, all diagnostic and logic circuitry is inactive. When the Enable Input is taken to a logic 1, the switches become 'armed' and ready to respond to their control input after a short, 30 μs. enable delay time. This delay interval prevents the switches from transient turn-on. Figure 16 shows the switch control logic.

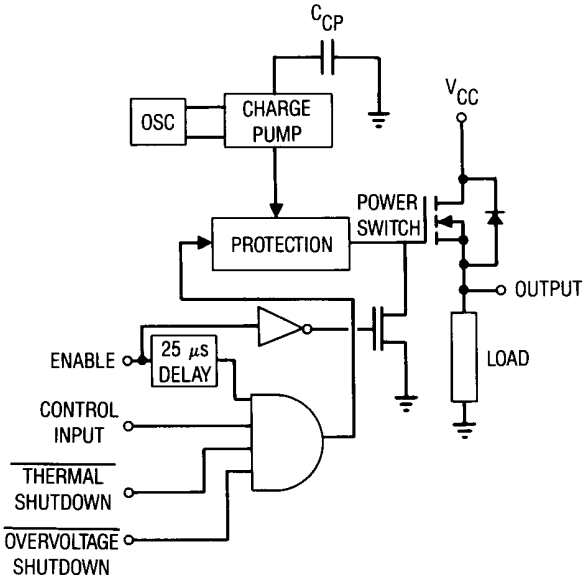


Fig. 16 — Control Logic for each Power Switch

Each DMOS switch is turned ON when its gate is driven approximately 3.5V more positive than its source voltage. Because the source of the switch is the output terminal to the load it can be taken to a voltage very near the V_{CC} supply potential. To ensure that there is sufficient voltage available to drive the gates of the DMOS devices a charge pump circuit is built in. This circuit is controlled by an internal 300 KHz oscillator and using an external 10 nF capacitor connected from pin 14 to ground generates a voltage that is approximately 20V greater than the V_{CC} supply voltage. This provides sufficient gate voltage drive for each of the switches which is applied under command of standard 5V logic input levels.

The turn-on time for each switch is approximately 12 μs when driving a 1A load current. This relatively slow switching time is beneficial in minimizing electromagnetic interference (EMI) related problems created from switching high current levels.

Applications Information (continued)

Protection Circuitry

The IR8400P has extensive protection circuitry built in. With any power device, protection against excessive voltage, current and temperature conditions is essential. To achieve a "fail-safe" system implementation, the loads are deactivated automatically by the IR8400P in the event of any detected overvoltage or over-temperature fault conditions.

Voltage Protection

The V_{CC} supply can range from -0.5V to +60V DC without any damage to the IR8400P. The CMOS logic circuitry is biased from an internal 5.1V regulator which protects these lower voltage transistors from the higher V_{CC} potentials. In order to protect the loads connected to the switch outputs however, an overvoltage shutdown circuit is employed. Should the V_{CC} potential exceed 35 volts all of the switches are turned OFF thereby disconnecting the loads. This 35V threshold has 750 mV of hysteresis to prevent potential oscillations.

Additionally, there is a built in undervoltage lockout feature. With V_{CC} less than 5 volts it becomes uncertain whether the logic circuitry can hold the switches in their commanded state. To avoid this uncertainty, all of the switches are turned OFF when V_{CC} drops below approximately 5V. Figure 17 illustrates the shutoff of an output during a 0 to 80V V_{CC} supply transient.

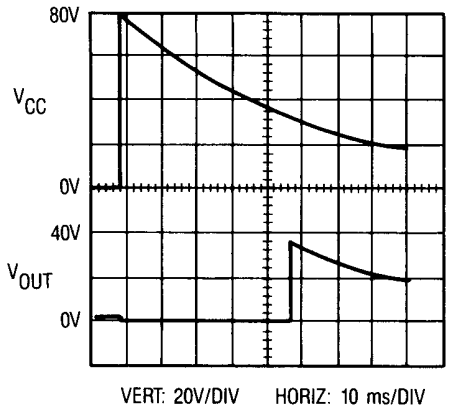


Fig. 17 — Overvoltage/Undervoltage Shutdown

The IR8400P has been designed to switch all types of loads. When driving a ground referenced inductive load such as a relay or solenoid, the voltage across the load will reverse polarity as the field in the inductor collapses when the power switch is turned OFF. This will pull the output pin of the IR8400P below ground. The -5volt clamping function is performed by the momentary conduction of the DMOS switches during the flyback of the inductive current — see Fig. 18.

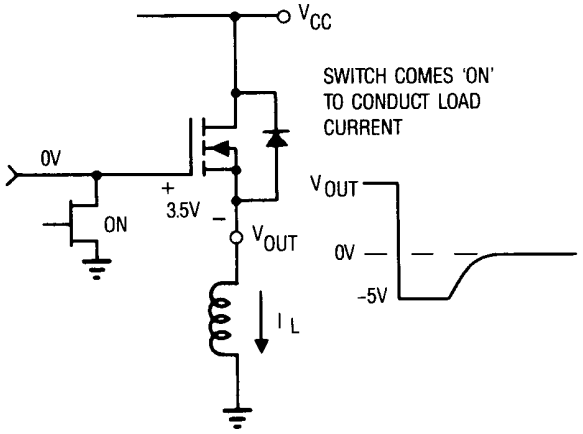


Fig. 18 — Turn-OFF Conditions With an Inductive Load

When the output inductance produces a negative voltage, the gate of the DMOS transistor is clamped at 0V. At -3.5V, the source of the power device is less than the gate by enough to cause the switch to turn ON again. During this negative transient condition the power limiting circuitry to protect the switch is disabled due to the gate being held at 0V. The maximum current during this clamping interval, which is equal to the steady state ON current through the inductor, should be kept less than 1A. The magnitude of the inductive flyback energy is also of concern. With larger inductors it may be possible for the additional power dissipation to cause the die temperature to exceed the thermal shutdown limit. If this occurs all of the other switches will turn OFF momentarily (see section on Thermal Management).

Power Limiting

The IR8400P utilizes a true instantaneous power limit circuit rather than simple current limiting to protect each switch. This provides a higher transient current capability while still maintaining a safe power dissipation level. The power dissipation in each switch (the product of the Drain-to-Source voltage and the output current, $V_{ds} \times I_{out}$) is continually monitored and limited to 15 Watts by varying the gate voltage and therefore the ON resistance of the switch. Basically the ON resistance will be as low as possible until 15 Watts is being dissipated. To maintain 15 Watts, the ON resistance increases to reduce the load current. This results in a

Applications Information (continued)

decrease of the output voltage. For resistive loads, the output voltage when in power limit will be:

$$V_{out}\ (\text{in Power Limit}) = \frac{V_{CC} - \sqrt{V_{CC}^2 - 60\ R_L}}{2}$$

This provides a maximum transient current and drain-to-source voltage characteristic as shown in Figure 4 in the Typical Performance Characteristics section.

The steady state current to the load is limited by the package power dissipation, ambient temperature and the ON resistance of the switch which has a positive temperature coefficient as shown in Figure 2 in the Typical Performance Characteristics section.

This dynamic current limiting of the switches is beneficial when driving lamp and large capacitive loads. Incandescent lamps require a large inrush current, on the order of 10 times the normal operating current, when first switched on with a cold filament. The IR8400P will limit this initial current to the level where 15 Watts is dissipated in the switch. As the filament warms up the voltage across the lamp increases thereby decreasing the voltage across the switch which permits more current to fully light the lamp. With limited inrush current the lifetime of a lamp load is increased significantly. Figure 19 illustrates the soft turn-on of a lamp load.

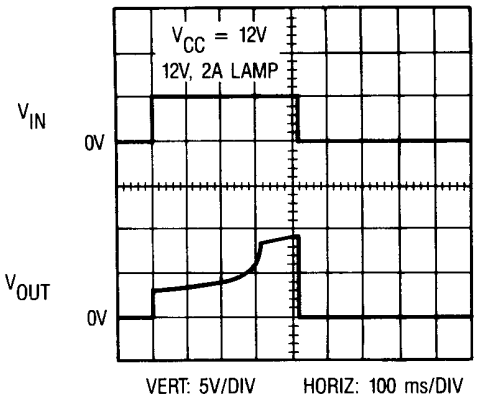


Fig. 19. Soft Turn-On of a Lamp Load

The same principle of increasing output current as the voltage across the load increases allows large capacitive loads to be charged more quickly by the IR8400P switch rather than a fixed 1A current limit protection scheme. Figure 20 shows the output response while driving a large capacitive load.

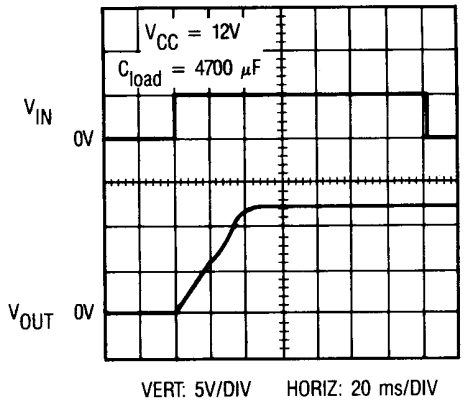


Fig. 20 — Driving a Large Capacitive Load

Thermal Protection

The die temperature of the IR8400 is continually monitored. Should any conditions cause the die temperature to rise to 170°C, all of the power switches are turned OFF automatically to reduce the power dissipation. It is important to realize that the thermal shutdown affects all four of the switches together. That is, if just one switch load is enough to heat the die to the thermal shutdown threshold, all of the other switches, regardless of the power dissipation conditions, will be switched OFF. All of the switches will be re-enabled when the die temperature has cooled to approximately 160°C. Until the high temperature forcing conditions have been removed the switches will cycle ON and OFF thus maintaining an average die temperature of 165°C. The IR8400P will signal that excessive temperatures exist through several diagnostic output signals (see Diagnostics).

Diagnostics

The IR8400 has extensive circuit diagnostic information reporting capability. Use of this information can produce systems with intelligent feedback of switch status as well as load fault conditions for troubleshooting purposes. All of the diagnostic information is contained in an 11-bit word. This data can be clocked out of the IR8400P in a serial fashion as shown in the Serial Diagnostic Data Assignments. The shift register is parallel loaded with the diagnostic data whenever the Chip Select Input is at a Logic 1 and changes to the serial shift mode when Chip Select is taken to a Logic 0. The Data Output line (pin 8) is biased internally from a 5.1V regulator which sets the Logic 1 output voltage. This pin has low current sourcing capability so any load on this pin will reduce the Logic 1 output level which is guaranteed to be at least 2.4V with a 360 μA load.

Applications Information (continued)

The data is clocked out of the IR8400P on the falling edge of the clock, to be clocked into the controlling microprocessor on the rising edge. Any number of devices can share a common data output line because the data output pin is held in a high impedance condition until the device is selected by taking its Chip Select Input low. Following Chip Select going low there is a short data set-up time interval (500 ns max) required. This is necessary to allow the first data bit of information to be established on the data output line prior to the first rising clock edge which will input the data bit into the controller. When all 11 bits of diagnostic data have been shifted out the data output goes to a Logic 1 level until the Chip Select line is returned high.

The first 4 bits indicate an output load error condition, one for each channel in succession (see Load Error Detection). Bits 5 through 8 provide a readback of the commanded ON/OFF status of each switch.

A unique feature of the IR8400P is that it provides an early warning of excessive operating temperature. Should the die temperature exceed 145°C, bit 9 will be set to a Logic 0. Acting on this information a system can be programmed to take corrective action, shutting OFF specific loads perhaps, while the IR8400P is still operating normally (not yet in thermal shutdown). If this early warning is ignored and the device continues to rise in temperature, the thermal shutdown circuitry will come into action at a die temperature of 170°C. Should this occur bit 10 of the diagnostic data stream will be set to a Logic 0 indicating that the device is in thermal shutdown and all of the outputs have been shut OFF.

The final data bit, bit 11, indicates an overvoltage condition on the V_{CC} supply (V_{CC} is greater than 35V) and again indicates that all of the switches are OFF.

The diagnostic data can be read periodically by a controller or only in the event of a general system error indication to determine the cause of any system problem. This general indication of a fault is provided by an Error Flag output (pin 13). This pin goes low whenever any type of error is detected. There is a built-in delay of approximately 75 μs from the time an error is detected until pin 13 is taken low. This is to help mask short duration error conditions such as may be caused by driving highly capacitive loads (>2 μF). A lamp load may generate a shorted load error for several hundred milliseconds as it turns on which should be ignored.

The Error Flag output pin is an open drain transistor which requires a pull-up resistor to a positive voltage of up to 16V. Typically this pull-up is to the same 5V supply which is biasing the Enable input and any other external logic circuitry. The Error Flag pins of several IR8400P packages can be connected together with just one pull up resistor to provide an all-encompassing general system error indication. Upon detection of an error, each device could then be polled for diagnostic information to determine the source of the fault condition.

A second direct output error flag is for an indication of Thermal Shutdown (pin 17). This active low flag provides an immediate indication that the die temperature has reached 170°C and that the drive to all four switches has been removed. This output is pulled up to the internal 5.1V logic regulator through a small (5 μA) current source so use of a buffer on this pin is recommended.

A useful feature of pin 17 is that it can also be used as a shutdown input. Driving this pin low immediately turns all of the switches OFF, just the same as if thermal shutdown temperatures had been reached, yet all of the control logic and diagnostic circuits remain active. This is useful in designing "fail-safe" systems where the loads can be disabled under any sort of externally detected system fault condition. The diagnostic logic however does not distinguish between normal thermal shutdown or the fact that pin 17 has been driven low. As such, various switch errors and an over-temperature indication will be reported in the diagnostic data stream.

Figure 21 illustrates the use of pin 17 as both an output thermal shutdown flag and as an input to shut down only the switches. Directly tying pin 17 to +5V will prevent the internal thermal shutdown circuitry from disabling the switches. For reliability purposes however this is not recommended as there will then be no limit to the maximum die temperature.

Refer to the Truth Table for a summary of the action of these direct-output error flags.

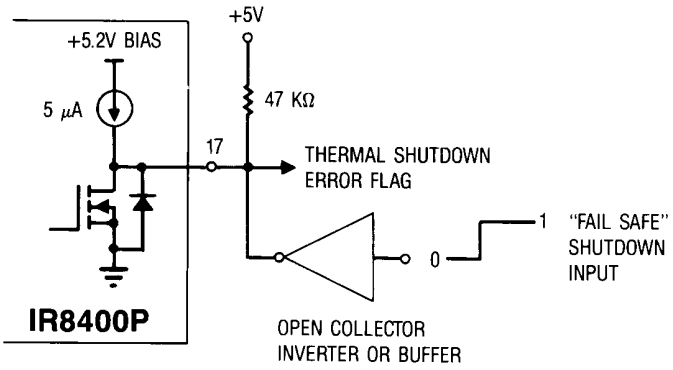


Fig. 21 — Thermal Shutdown Flag and Shutdown Input

Applications Information (continued)

Load Error Detection

An important feature of the IR8400P is the ability to detect opened or shorted load connections. Figure 22 illustrates the detection circuitry used with each of the switches.

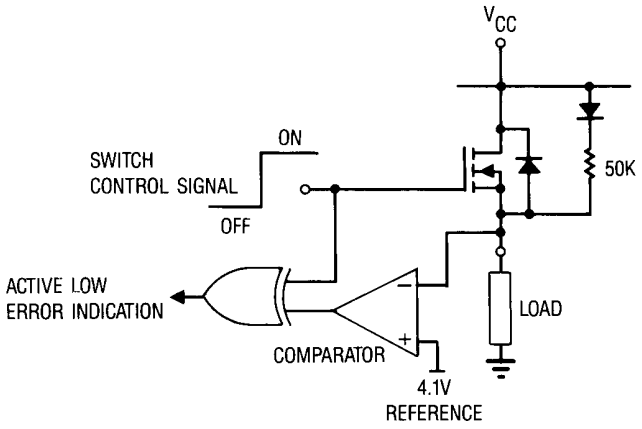


Fig. 22 — Detection Circuitry for Open/Shorted Loads

A voltage comparator monitors the voltage to the load and compares it to a fixed 4.1V reference level. When a switch is OFF, the ground referenced load should have no voltage across it. Under this condition, an internal 50 KΩ resistor connected to V_{CC} will provide a small amount of current to the load. If the load resistance is large enough to create a voltage greater the 4.1V an Open Load Error will be indicated for that switch. The maximum load resistance that will not generate an Open Load Error when a switch is OFF can be found by:

$$R_{max} = \frac{4.1V}{V_{CC} - 4.6V} \times 50\ K\Omega;\ \text{for no Open Load Indication}$$

To make this Open Load Error threshold more sensitive, an external pull-up resistor can be added from the output to the V_{CC} supply.

Also when a switch is commanded OFF, should the load be shorted to the V_{CC} supply, this same circuitry will again indicate an error.

When a switch is commanded ON, the load is expected to have a voltage across it that approaches the V_{CC} potential. If the output voltage is less than the 4.1V threshold an error will again be reported, indicating that the load is either shorted to ground or that the switch is in power limit and not able to pull the output voltage any closer to V_{CC}. The minimum load resistance that will not generate a Shorted Load Error when a switch is ON can be found by:

$$R_{min} = \frac{4.1V\ (V_{CC} - 4.1V)}{15W};\ \text{for no Shorted Load Error}$$

Figure 23 indicates the range of load resistance for normal operation, open load, and shorted load or power limited indication.

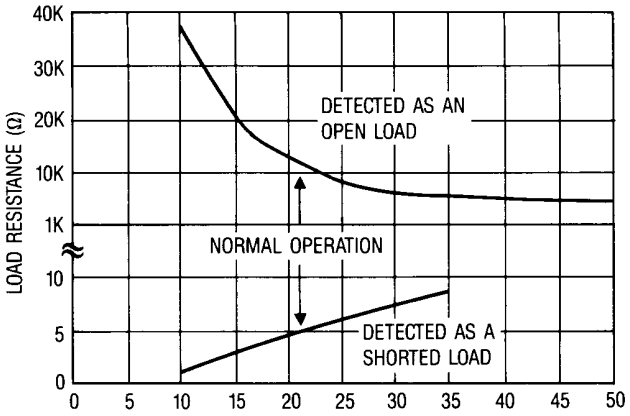


Fig. 23 — Load Resistance Detected as Errors

Thermal Management

It is particularly important to consider the total amount of power being dissipated by all four switches in the IR8400P at all times. Any combination of the switches driving loads will cause an increase in the die temperature. Should the die temperature reach the themal shutdown threshold of 170°C, all of the switches will be disabled. Careful calculation of the worst case total power dissipation required at any point in time, together with providing sufficient heatsinking will prevent this from occuring.

The IR8400P is packaged with a special leadframe that helps dissipate heat through the two ground pins on each side of the package. The thermal resistance from junction-to-case (θ_{jc}) for this package is approximately 20° C/W. The thermal resistance from junction-to-ambient (θ_{ja}), without any heatsinking, is approximately 60° C/W. Figure 14 in Typical Performance Section illustrates how the copper foil of a printed circuit board can be designed to provide heatsinking and reduce the overall junction-to-ambient thermal resistance.

The power dissipation in each switch is equal to:

$$Pd\ (\text{each switch}) = I_{load}^2 \times R_{on}\ \text{or}\ \frac{(V_{cc} - V_{out})^2}{R_{on}}$$

where R_{on} is the ON resistance of the switch (1.3Ω maximum). These equations hold true until the power dissipation reaches the maximum limit of 15 Watts. With resistive loads, the 15 Watts power limit threshold will be reached when:

$$R_L \leq \frac{V_{cc}^2}{60W}$$

Applications Information (continued)

Inductive loads will create additional power dissipation when switched OFF. Figure 24 shows the idealized voltage and current waveforms for an inductive load.

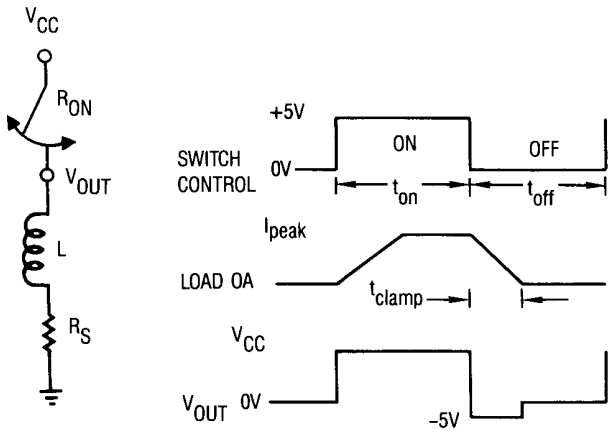


Fig. 24 — Switching an Inductive Load

Losses during the turn-on and conduction interval can be calculated with the following formula:

$$E_{on} = R_{on}\left(\frac{V_{cc}}{R_{on} + R_s}\right)^2 \left(t_{on} + 2\tau e^{-t_{on}/\tau} - \frac{\tau}{2} e^{-2t_{on}/\tau}\right)$$

with $\tau = L/(R_{on} + R_S)$

In most applications the two exponentials are negligible and the expression simplifies into:

$$E_{on} = R_{on}\left(\frac{V_{cc}}{R_{on} + R_s}\right)^2 t_{on}$$

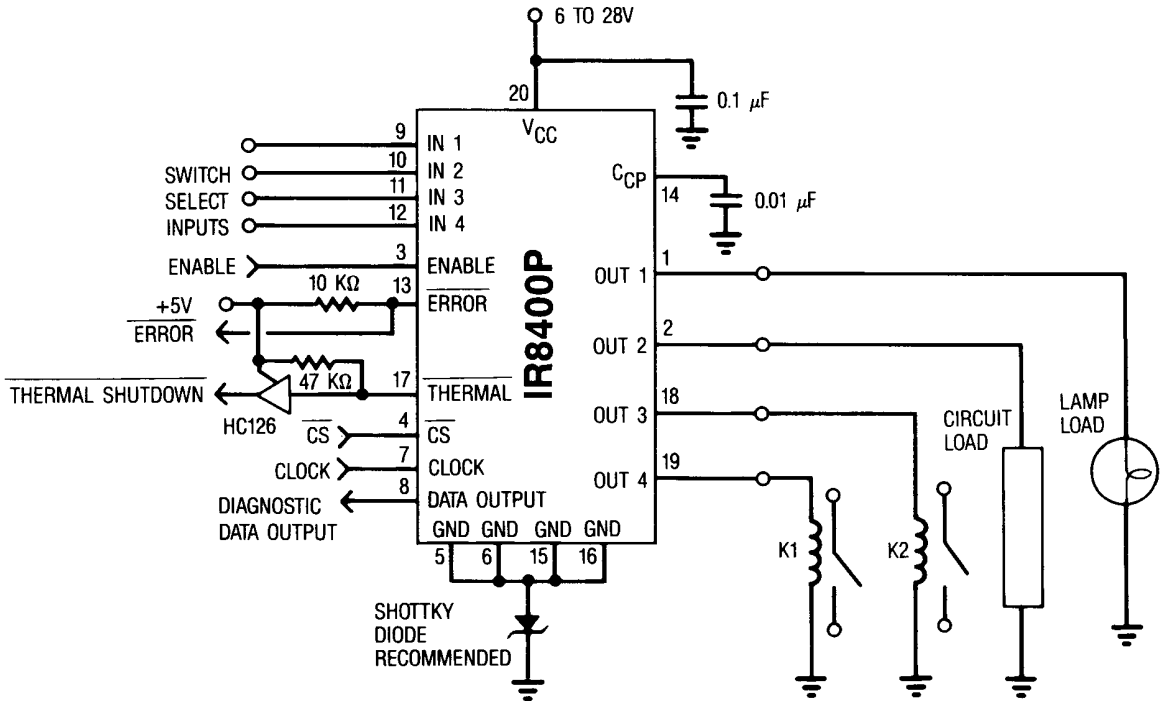
The turn-off losses are

$$E_{off} = \frac{(V_{cc} + 5)}{2} \frac{V_{cc}}{(R_{on} + R_s)}$$

This expression will give conservative results since, in most applications, the negative clamp voltage will be less than 5V.

For repetitive pulses, the average power losses can be obtained by multiplying the total energy by the repetition rate.

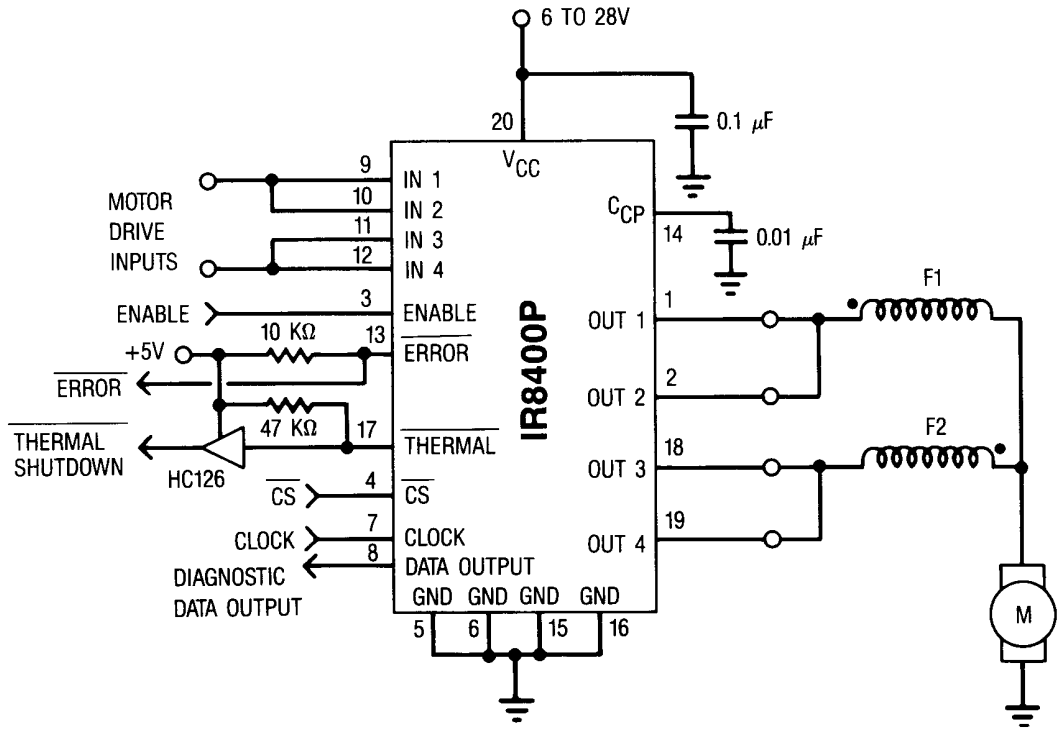
Typical Applications



Basic Application Circuit With Reverse Voltage Withstand Capability

Simple protection of the IR8400 against supply voltage reversal. Loads will be energized through the intrinsic diodes in parallel with the power switches. The schottky diode will add approximately 0.2V to the logic input switching thresholds and the logic output low levels.

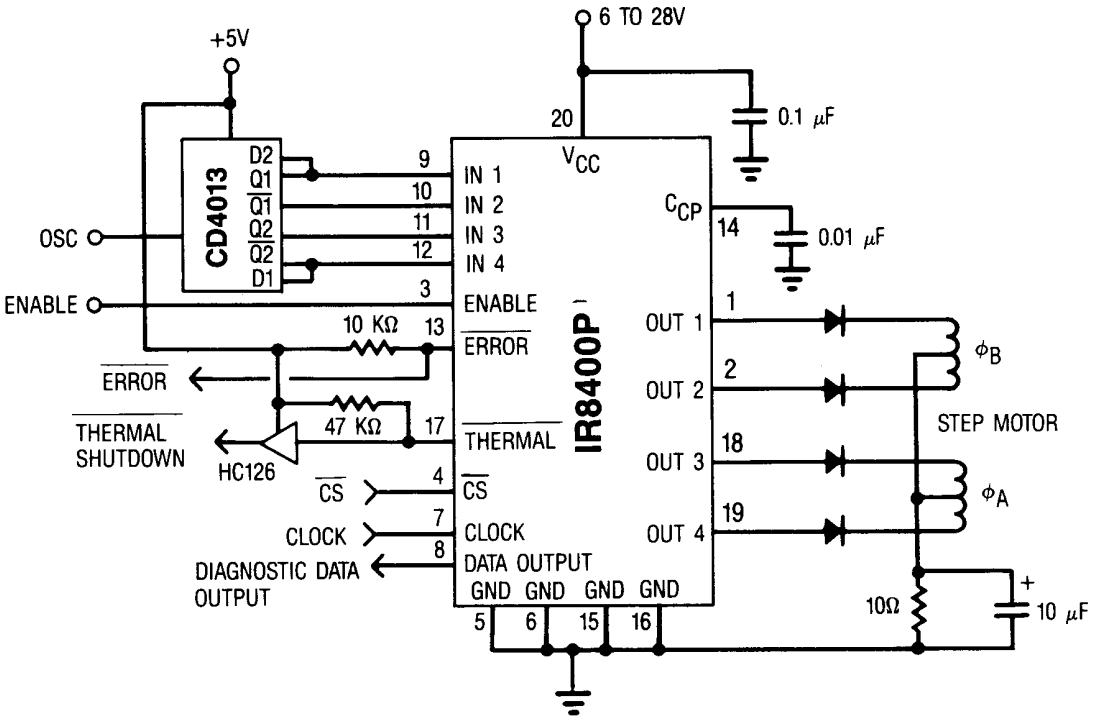
Typical Applications (continued)



Reversable Series DC Motor Drive

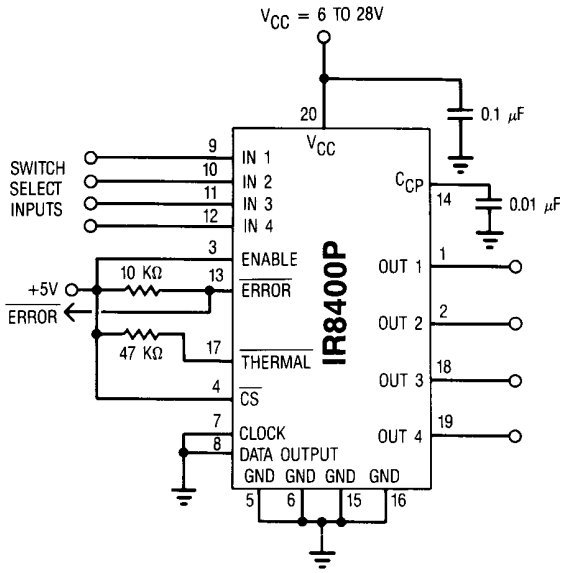
Parallelling switches for higher current capability. Positive temperature coefficient of the switch ON resistance provides ballasting to evenly share the load current between the switches. Any combination of switches can be paralleled. Required peak load current will depend upon the motor load. Motor speed control can be provided by a PWM signal of up to 20 KHz applied to the motor drive input lines.

Series motor can be reversed by using two field windings as shown F_1 and F_2.

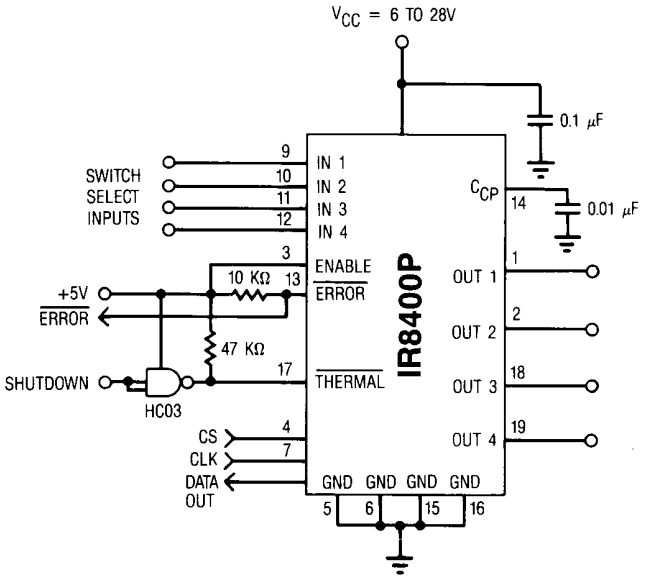


Unipolar Drive for a 2-Phase Stepper Motor

Typical Applications (continued)

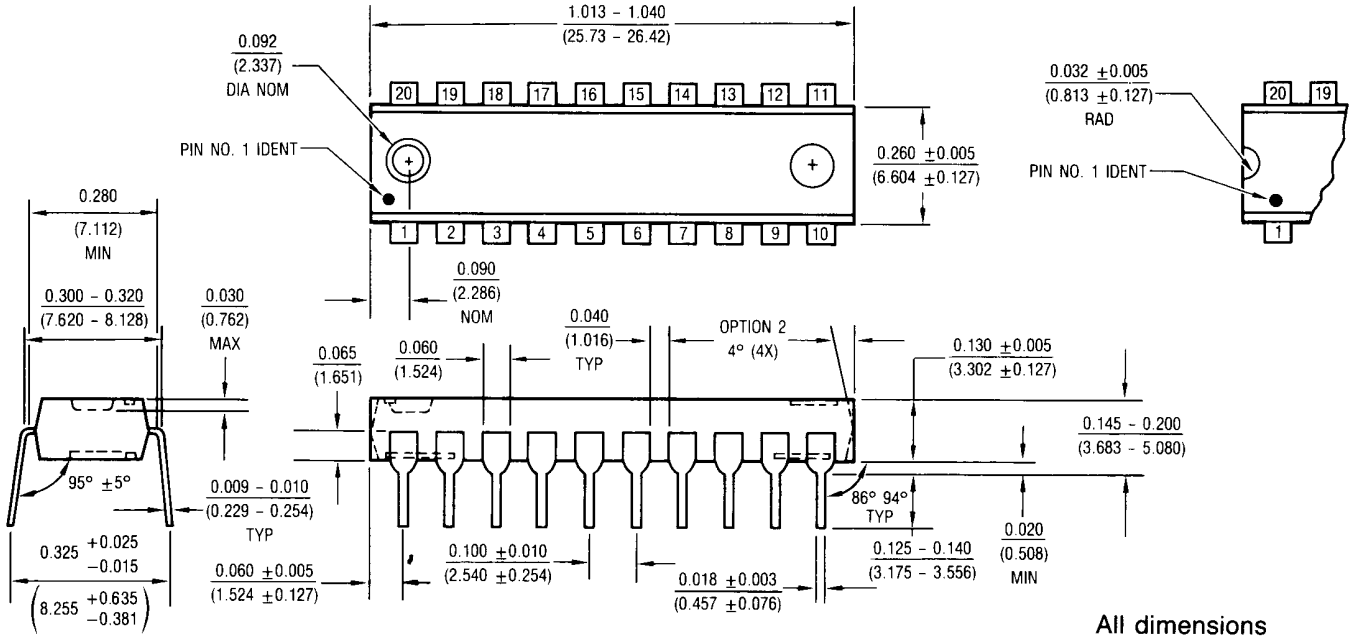


Recommended Connection if No Diagnostics are Required



"Fail-Safe" Fast Shutdown of all Channels

Mechanical Specification



All dimensions in Inches (millimeters)

20-Lead Molded DIP Package

International
IOR Rectifier

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