FTD2012

N- Channel Silicon MOS FET
Load S/W USE

TENTATIVE

Features

- Low ON-state resistance.
- 4V drive.
- Mount height of 1.1mm.
- Complex Type enabling high density mount

Absolute Maximum Ratings / Ta=25°C

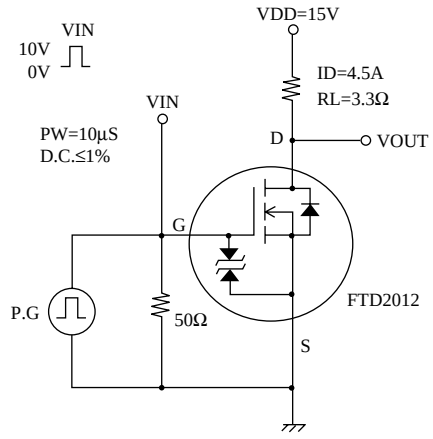
				unit
Drain to Source Voltage	VDSS		30	V
Gate to Source Voltage	VGSS		±20	V
Drain Current(DC)	ID		4.5	A
Drain Current(Pulse)	IDP	PW≤10μS, dutycycle≤1%	20	A
Allowable power Dissipation	PD	Mounted on ceramic board (1000mm² × 0.8mm) 1unit	0.8	W
Total Dissipation	PT	Mounted on ceramic board (1000mm² × 0.8mm)	1.3	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Electrical Characteristics / Ta=25°C

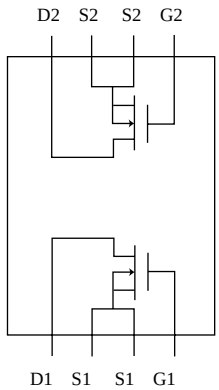
			min	typ	max	unit
Drain to Source Breakdown Voltage	V(BR)DSS	ID=1mA , VGS=0	30			V
Zero Gate Voltage Drain Current	IDSS	VDS=30V , VGS=0			1	μA
Gate to Source Leakage Current	IGSS	VGS=±16V , VDS=0			±10	μA
Cutoff Voltage	VGS(off)	VDS=10V , ID=1mA	1.0		2.4	V
Forward Transfer Admittance	| yfs |	VDS=10V , ID=4.5A	6.3	9		S
Static Drain to Source On State Resistance	RDS(on) 1	ID=4.5A , VGS=10V		26	34	mΩ
	RDS(on) 2	ID=4A , VGS=4V		43	60	mΩ
Input Capacitance	Ciss	VDS=10V , f=1MHz		750		pF
Output Capacitance	Coss	VDS=10V , f=1MHz		170		pF
Reverse Transfer Capacitance	Crss	VDS=10V , f=1MHz		105		pF
Turn-ON Delay Time	td(on)	See Specified Test Circuit		12		ns
Rise Time	tr	"		56		ns
Turn-OFF Delay Time	td(off)	"		73		ns
Fall Time	tf	"		38		ns
Total Gate Charge	Qg	VDS=10V, VGS=10V, ID=4.5A		18		nC
Gate Source Charge	Qgs			2.3		nC
Gate Drain Charge	Qgd			3.2		nC
Diode Forward Voltage	VSD	IS=4.5A , VGS=0		0.8	1.2	V

Marking : D2012

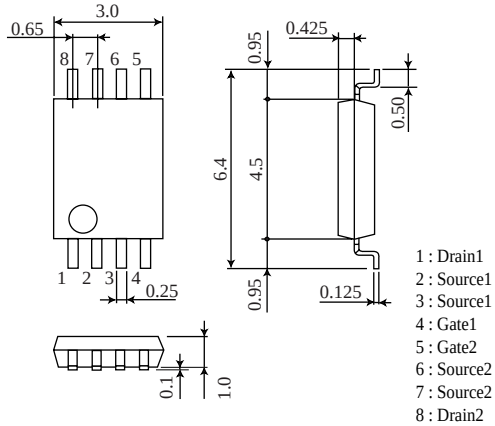
Switching Time Test Circuit



Electrical Connection



Case Outline
TSSOP8(unit:mm)



1 : Drain1
2 : Source1
3 : Source1
4 : Gate1
5 : Gate2
6 : Source2
7 : Source2
8 : Drain2

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