AT91SAM9261-EK Evaluation Board

User Guide

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Section 1

Overview

1.1 Scope

The AT91SAM9261-EK evaluation kit is an effective platform for evaluating chip performance and developing code for applications based on the AT91SAM9261.

This guide is a description of the hardware included in the AT91SAM9261-EK evaluation kit. Software files are available on the DVD-ROM included in the kit and described in "Deliverables" below.

1.2 Deliverables

The AT91SAM9261-EK package contains the following items:

- an AT91SAM9261-EK board
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- one DataFlash® card
- universal input AC/DC power supply with US and EU plug adapter
- one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 The AT91SAM9261-EK Evaluation Board

The board is equipped with an AT91SAM9261 (217-ball LFBGA package) together with the following:

- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory
- one Atmel 32 Mbit serial DataFlash (AT45DB321C-CNC)
- one USB device port interface
- two USB host port interfaces
- one DBGU serial communication port

- JTAG/ICE debug interface
- one Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- one Power LED and two general-purpose LEDs
- four user input pushbuttons
- one wakeup input pushbutton
- one reset pushbutton
- one DataFlash SD/MMC card slot
- two expansion footprint connectors (solder side)
- one Lithium Coin Cell Battery Retainer for 12 mm cell size
- dual pitch prototyping area

Section 2

Setting Up the AT91SAM9261-EK Evaluation Board

2.1 Electrostatic Warning

The AT91SAM9261-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM9261-EK evaluation board, the following items are required:

- the AT91SAM9261-EK evaluation board itself
- AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm

2.3 Layout

Figure 2-1. AT91SAM9261-EK Layout - Top View

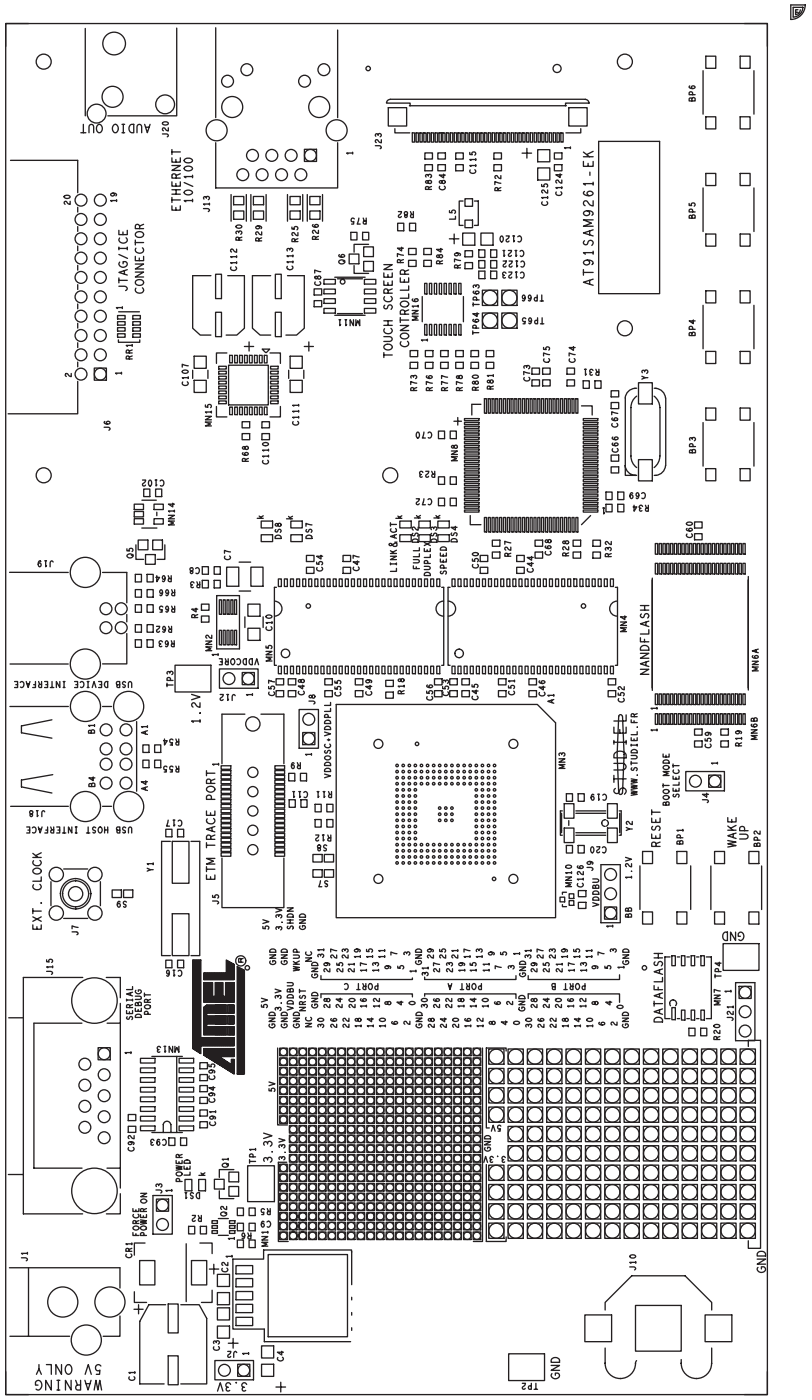
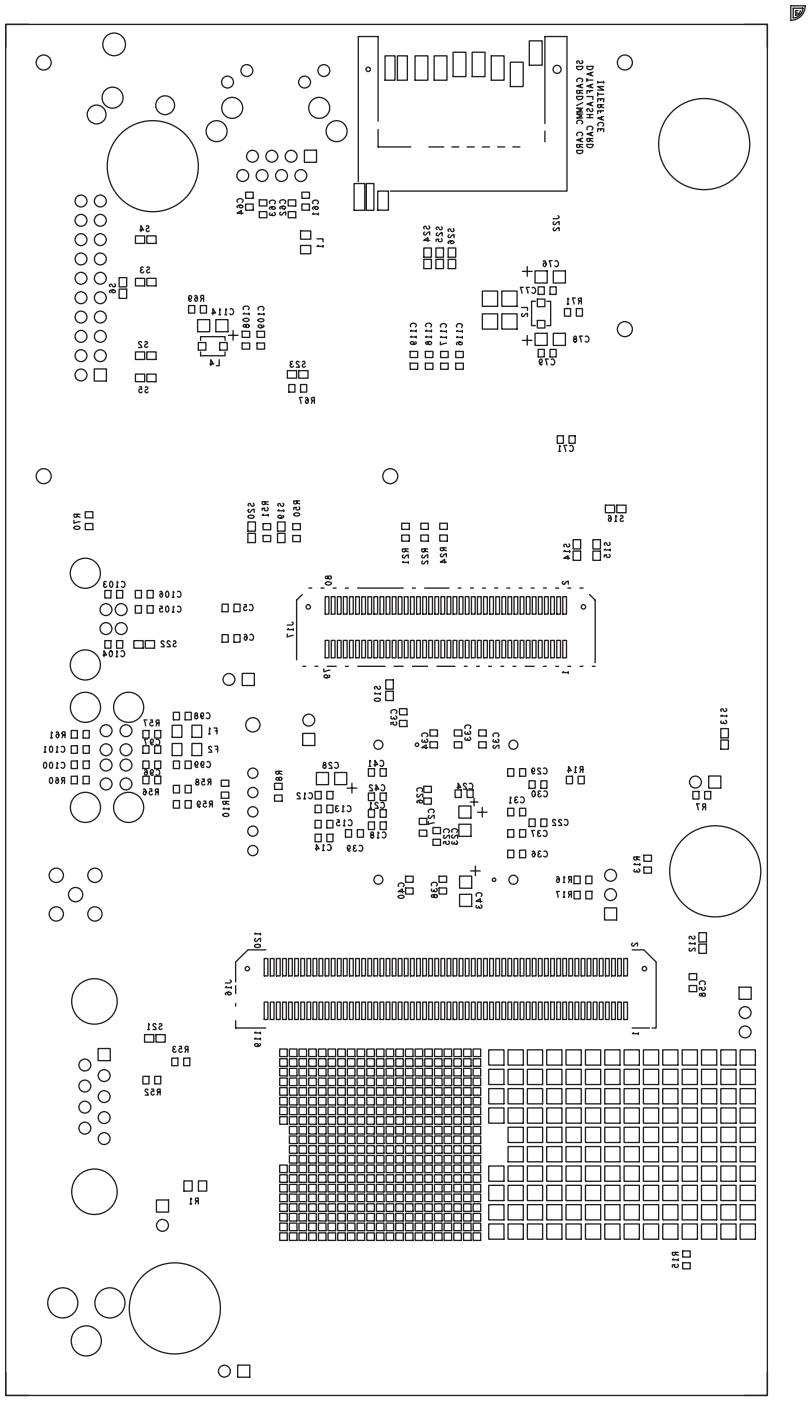


Figure 2-2. AT91SAM9261-EK Layout - Bottom View



2.4 Powering Up the Board

AT91SAM9261-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket (J1). The coaxial power plug center pin is positive polarity .

2.5 Backup Power Supply

The user has the possibility to add a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J9 configuration must to be set in position 1, 2.

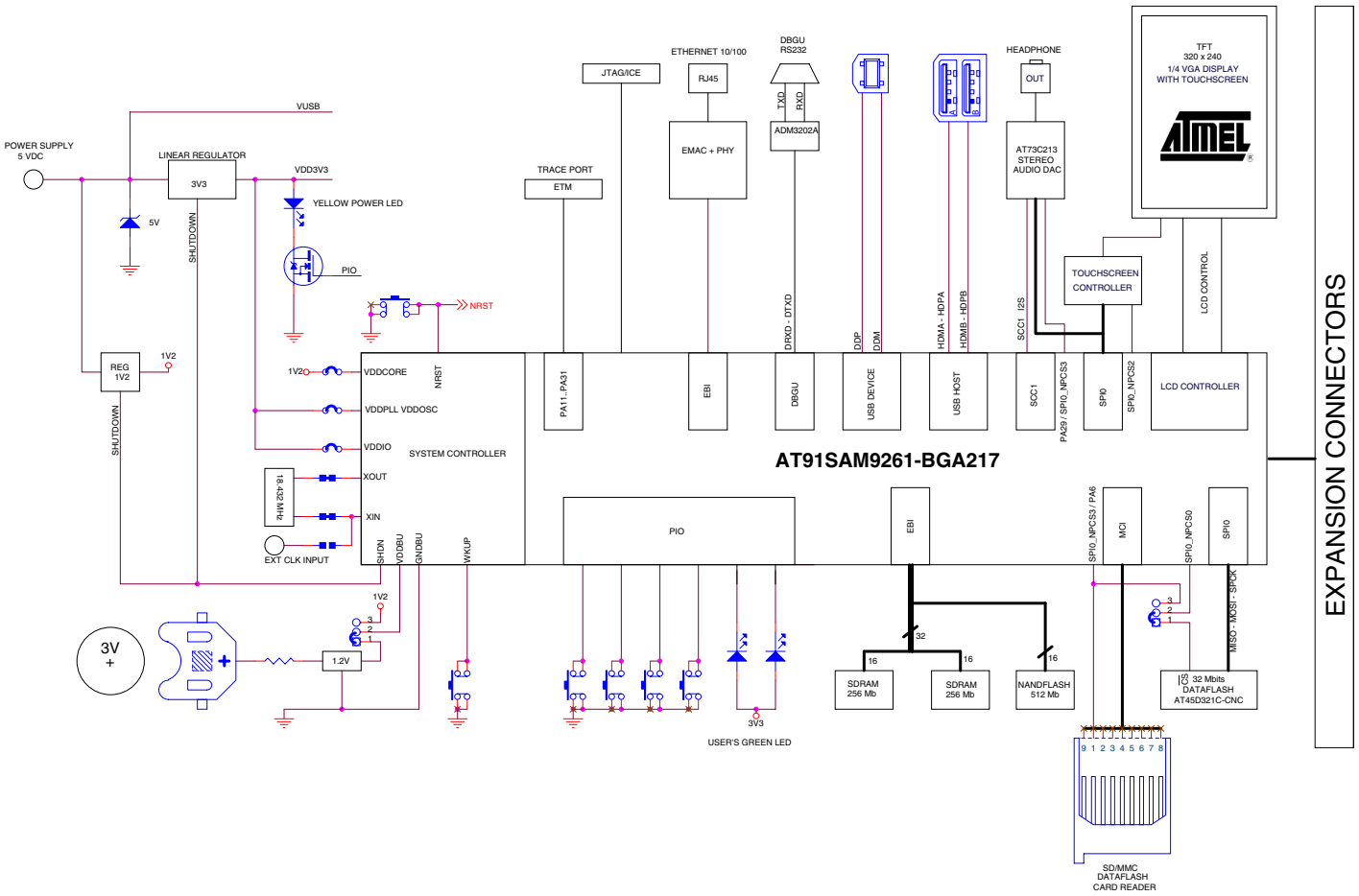
Refer to Table 4-1, “Configuration Jumpers and Straps”.

2.6 Getting Started

The AT91SAM9261-EK evaluation board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9261-EK.

2.7 AT91SAM9261-EK Block Diagram

Figure 2-3. Block Diagram



Section 3

Board Description

3.1 AT91SAM9261 Microcontroller

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions
  - ARM Jazelle® Technology for Java™ Acceleration
  - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
  - Mid-level implementation Embedded Trace Macrocell™
- Additional Embedded Memories
  - 32K Bytes of Internal ROM, Single-cycle Access at Maximum Bus Speed
  - 160K Bytes of Internal SRAM, Single-cycle Access at Maximum Processor or Bus Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, NAND Flash and CompactFlash®
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 16-bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode (24-bit per Pixel), Resolution up to 2048 x 2048
- USB
  - USB 2.0 Full Speed (12 Mbits per second) Host Double Port
    Dual On-chip Transceivers
    Integrated FIFOs and Dedicated DMA Channels
  - USB 2.0 Full Speed (12 Mbits per second) Device Port
    On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
- Bus Matrix
  - Handles Five Masters and Five Slaves
  - Boot Mode Select Option

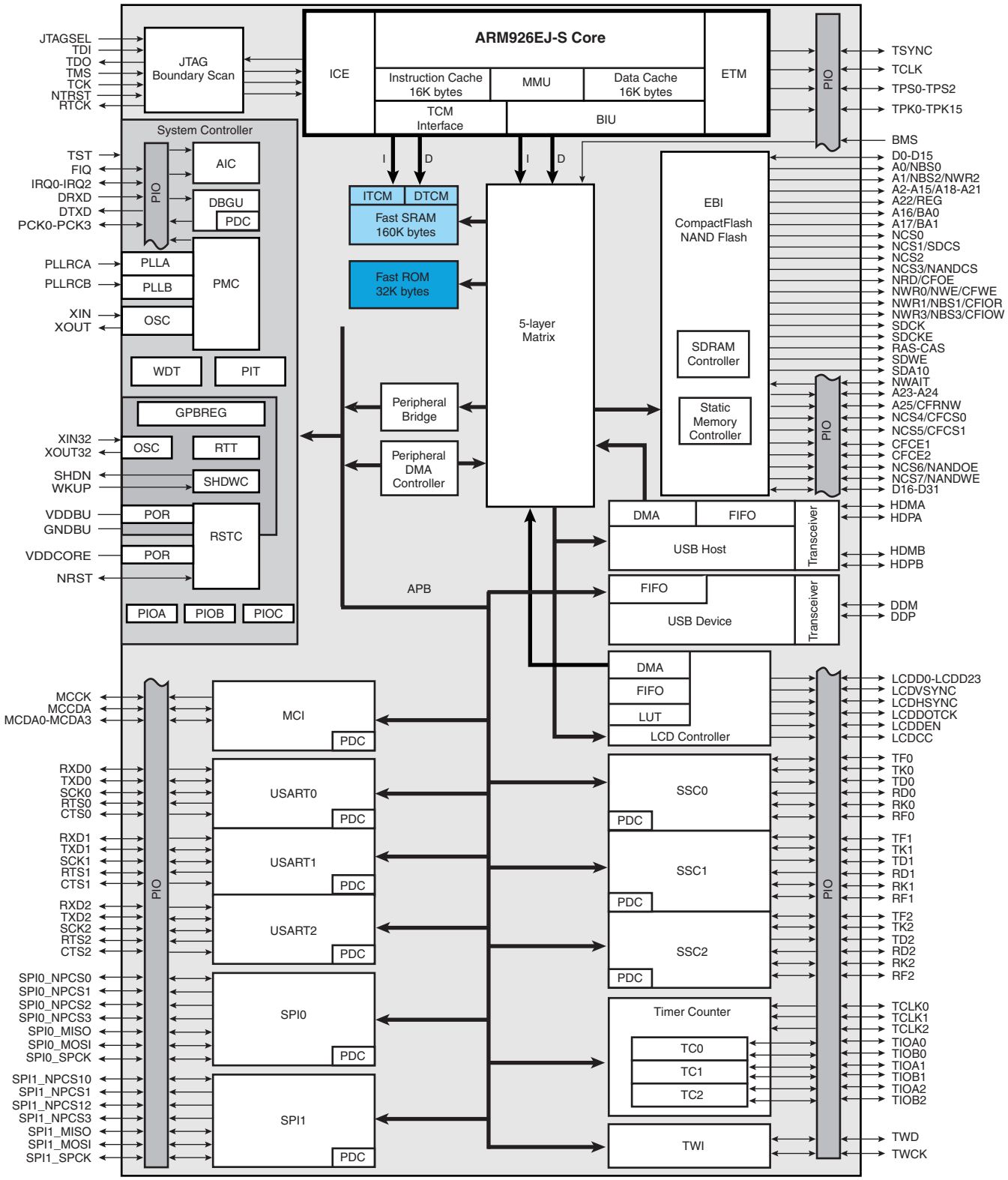
  - Remap Command

- Fully Featured System Controller (SYSC) for Efficient System Management, including
  - Reset Controller, Shutdown Controller, Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
  - Three 32-bit PIO Controllers
- Reset Controller (RSTC)
  - Based on Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32.768 kHz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator and two PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire USART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key Protected, Programmable Only Once, Windowed 12-bit Counter, Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock
- Three 32-bit Parallel Input/Output Controllers (PIO) PIOA, PIOB and PIOC
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Nineteen Peripheral DMA (PDC) Channels

- Multimedia Card Interface (MCI)
  - Compliant with Multimedia Cards and SDCards
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel EEPROMs Supported
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 2.7V to 3.6V for VDDOSC and for VDDPLL
  - 2.7V to 3.6V for VDDIOP (Peripheral I/Os) and for VDDIOM (Memory I/Os)
- Available in a 217-ball LFBGA RoHS-compliant Package

3.2 AT91SAM9261 Block Diagram

Figure 3-1. Block Diagram



3.3 Memory

- 32 Kbytes of Internal ROM
- 160 Kbytes of Internal High-speed SRAM
- Atmel 32 Mbit serial DataFlash
- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory

3.4 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- 32.768 kHz standard crystal for the slow clock oscillator

3.5 Reset Circuitry

- Internal reset controller with a bi-directional reset pin
- External reset push button

3.6 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.7 Power Supply Circuitry

- For dynamic power consumption, the AT91SAM9261 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm
- On-board 1.2V high efficiency step-down charge pump regulator with shutdown control
- On-board 3.3V linear regulator with shutdown control

3.8 Remote Communication

- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
- USB V2.0 Full-speed Compliant, 12 Mbits per second (UDP)
- Two USB Host port V2.0 Full-speed Compliant, 12 Mbits per second (UHP)
- One Ethernet 100-base TX with three status LEDs

3.9 Audio Stereo Interface

- One Atmel stereo audio DAC AT73C213
- One 32 Ohm/20 mW Stereo Headset output (J20) with Master Volume and Mute Controls

3.10 User Interface

- Four user input pushbuttons
- Two user green LEDs
- One yellow power LED (can be also software controlled)

- One ¼ VGA display LCD with Touchscreen and white LED backlight

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM Port

3.12 Expansion Slot

- One DataFlash, SD/MMC card slot
- All I/Os of the AT91SAM9261 are routed to peripheral extension footprint connectors (J16 and J17). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1 gives details on configuration straps on the AT91SAM9261-EK evaluation board and their default settings.

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper (1) This jumper footprint is provided for 3.3V power consumption measurement use. By default, it is closed. To use this feature, the user has to open the strap by cutting it before soldering a jumper.
J3	Closed	Forces power on. To use the software shutdown control, J3 must be opened.
J4	Opened	Enables Boot on the internal ROM
	Closed	Enables Boot on the NCS0
J8	Closed	VDDPLL Jumper (1)
J9	2-3	VDDBU Jumper select (1) 1-2 : Lithium 3V Battery 2-3 : 1.2V from VDDCORE
J12	Closed	VDDCORE Jumper (1)
J21	1-2	NPCS0 select 1-2 : AT45DB321C (MN7) 2-3 : Dataflash card interface (J22). **Warning: In this case NPCS03 must be configured as input.**
S2	Opened	Disables the ICE NTRST input
S3	Closed	Enables the ICE RTCK return. S6 must be opened
S4	Closed	Enables the ICE NRST input
S5	Opened	Selects ICE mode or JTAG mode (Closed)
S6	Opened	Disables TCK <-> RTCK local loop. If S6 is closed, S3 must be opened.

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
S7-S8 S9	Closed Opened	Enables the use of 18.432 MHz crystal. If external clock used, S7-S8 must be opened and S9 closed.
S10	Closed	Enables the use of SDRAM (NCS1_SDCS)
S12	Opened	Disables Serial DataFlash write protect.
S13	Closed	Disables NAND FLASH write protect.
S14	Closed	Enables the use of interrupt ETHERNET MAC (PC11_FIQ).
S15	Closed	Enables the use of ETHERNET MAC (NCS2).
S16	Opened	Disables the use of NWAIT ETHERNET MAC signal (PC2_NWAIT)
S19	Closed	Enables the use of the User LED DS7 (PA14)
S20	Closed	Enables the use of the User LED DS8 (PA13)
S21	Closed	Enables the use of the DBGU RXD signal (PA9)
S22	Closed	Enables the use of the USB CNX detection (PB29)
S23	Closed	Enables the use of AUDIO DAC INTERFACE (NPCS03)
S24	Closed	Enables the use of TOUCH SCEEN CONTROLLER (NPCS02)
S25	Closed	Enables the use of TOUCH SCEEN CONTROLLER BUSY signal (PA11)
S26	Closed	Enables the use of TOUCH SCEEN CONTROLLER PENIRQ (PC2_IRQ0)
TP1	N.A	3.3V Test point.
TP2	N.A	GND Test point.
TP3	N.A	1.2V Test point.
TP4	N.A	GND Test point.
TP63	N.A	0 to 3.3V analog user's input
TP64	N.A	0 to 3.3V analog user's input
TP65	N.A	AGND of TP63
TP66	N.A	AGND of TP64

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.

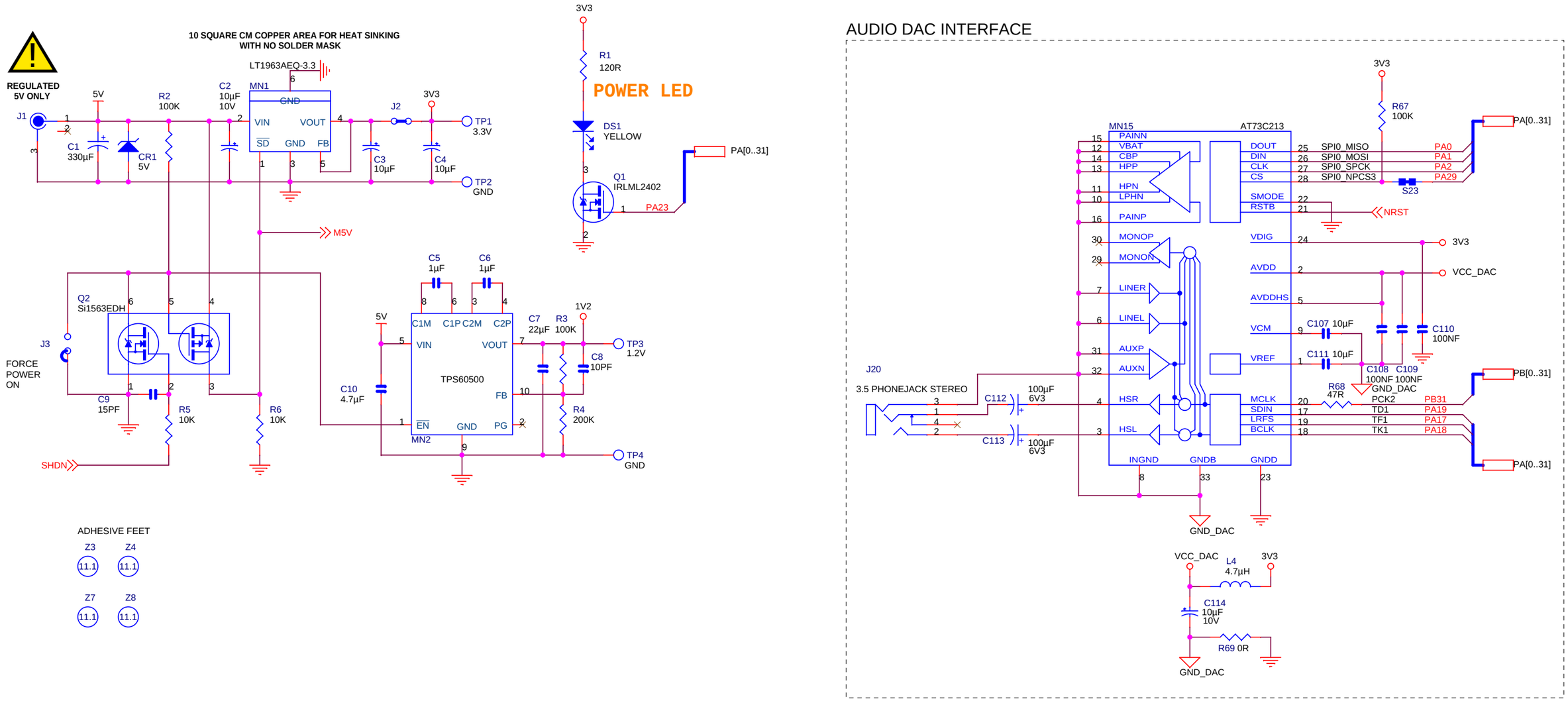
Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Power Supply and Audio
- AT91SAM9261
- SDRAM and NAND Flash
- Ethernet
- LCD and User Interface
- Serial and I/O Expansion



Wednesday, September 14, 2005

REV	MODIF.	DES.	DATE	VER.	DATE
C		JPG	14/09/05		
B		JPG	04/20/05		
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05

AT91SAM9261-EK

POWER SUPPLY & AUDIO

SCALE 1/1

REV. C

SHEET 1/6

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AT91SAM9261

PC[0..15]
PB[0..31]
PA[0..31]

D[0..31]
A[0..22]

BOOT MODE SELECT

PB3 BMS
R7 1K
J4

ETM TRACE PORT

PA13	PIPESTAT[0]	38	37	TRACEPKT[8]	PA24
PA14	PIPESTAT[1]	36	35	TRACEPKT[9]	PA25
PA15	PIPESTAT[2]	34	33	TRACEPKT[10]	PA26
PA11	TRACESYNC	32	31	TRACEPKT[11]	PA27
PA16	TRACEPKT[0]	30	29	TRACEPKT[12]	PA28
PA17	TRACEPKT[1]	28	27	TRACEPKT[13]	PA29
PA18	TRACEPKT[2]	26	25	TRACEPKT[14]	PA30
PA19	TRACEPKT[3]	24	23	TRACEPKT[15]	PA31
PA20	TRACEPKT[4]	22	21	ICE_NTRST	
PA21	TRACEPKT[5]	20	19	TDI	
PA22	TRACEPKT[6]	18	17	TMS	
PA23	TRACEPKT[7]	16	15	TCK	
	VSUPPLY	14	13	ICE_RTCK	
	EXTTRIG	12	11	TDO	
PA12	TRACECLK	10	9	ICE_NRST	
		8	7	DBGRQ	
		6	5	GND	
		4	3		
		2	1		

3V3
R8 10K
R9 0R
C11 100NF
R10 10K
G1 G2 G3 G4 G5
J5
DNP

ICE INTERFACE

3V3
RR1 100K
J6
ICE_NTRST S2
TDI
TMS
TCK
ICE_RTCK S3
TDO
ICE_NRST S4 NRST
S6
S5

MN3

PA0	R11	PA0/SPI0_MISO/MCDA0	LCDVSYNC/PB0
PA1	T12	PA1/SPI0_MOSI/MCCDA	LCDHSYNK/PB1
PA2	U13	PA2/SPI0_SPCK/MCCK	LCDDOTCK/PCK0/PB2
PA3	P10	PA3/SPI0_NPCS0	BMSLCDDENJ/PB3
PA4	T13	PA4/SPI0_NPCS1/MCDA1	LCDCC/LCDD2/PB4
PA5	U14	PA5/SPI0_NPCS2/MCDA2	LCDD0/LCDD3/PB5
PA6	T14	PA6/SPI0_NPCS3/MCDA3	LCDD1/LCDD4/PB6
PA7	R12	PA7/TWD/PCK0	LCDD2/LCDD5/PB7
PA8	T15	PA8/TWCK/PCK1	LCDD3/LCDD6/PB8
PA9	U16	PA9/DRXD/PCK2	LCDD4/LCDD7/PB9
PA10	R13	PA10/DTXD/PCK3	LCDD5/LCDD10/PB10
PA11	T16	PA11/TSYNK/SCK1	LCDD6/LCDD11/PB11
PA12	U15	PA12/TCLK/RTS1	LCDD7/LCDD12/PB12
PA13	R14	PA13/TPS0/CTS1	LCDD8/LCDD13/PB13
PA14	T17	PA14/TPS1/SCK2	LCDD9/LCDD14/PB14
PA15	P13	PA15/TPS2/RTS2	LCDD10/LCDD15/PB15
PA16	P14	PA16/TPK0/CTS2	LCDD11/LCDD19/PB16
PA17	R15	PA17/TPK1/TF1	LCDD12/LCDD20/PB17
PA18	R17	PA18/TPK2/TK1	LCDD13/LCDD21/PB18
PA19	P16	PA19/TPK3/TD1	LCDD14/LCDD22/PB19
PA20	P17	PA20/TPK4/RD1	LCDD15/LCDD23/PB20
PA21	N15	PA21/TPK5/RK1	TF0/LCDD16/PB21
PA22	N14	PA22/TPK6/RF1	TK0/LCDD17/PB22
PA23	N16	PA23/TPK7/RTS0	TD0/LCDD18/PB23
PA24	N17	PA24/TPK8/SPI1_NPCS1	RD0/LCDD19/PB24
PA25	M14	PA25/TPK9/SPI1_NPCS2	RK0/LCDD20/PB25
PA26	M15	PA26/TPK10/SPI1_NPCS3	RF0/LCDD21/PB26
PA27	L15	PA27/TPK11/SPI0_NPCS1	SPI1_NPCS1/LCDD22/PB27
PA28	M16	PA28/TPK12/SPI0_NPCS2	SPI1_NPCS0/LCDD23/PB28
PA29	M17	PA29/TPK13/SPI0_NPCS3	SPI1_SPCK/IRQ2/PB29
PA30	L14	PA30/TPK14/A23	SPI1_MISO/IRQ1/PB30
PA31	L16	PA31/TPK15/A24	SPI1_MOSI/PCK2/PB31

DDP	A12	DDP	
DDM	B12	DDM	
HDPA	C12	HDPA	
HDMA	B14	HDMA	
HDPB	A13	HDPB	
HDMB	A14	HDMB	
	E17	TDI	
	C17	TMS	
	D17	TCK	
	U17	RTCK	
	F16	TDO	
	B10	JTAGSEL	
	F17	NTRST	
	U9	PLLRCB	
	U10	PLLRCA	
	U12	XOUT	
	U11	XIN	
	T10	VDDOSC	
	T11	GNDOSC	
	A10	XOUT32	
	A11	XIN32	
	R10	VDDPLL	
	P9	GNDPLL	

PC0	U2	NANDOE/NCS6/PC0	
PC1	P6	NANDWE/NCS7/PC1	
PC2	T4	NWAIT/IRQ0/PC2	
PC3	U3	A25/CFRNW/PC3	
PC4	R6	NCS4/CFCS0/PC4	
PC5	T6	NCS5/CFCS1/PC5	
PC6	U5	CFCE1/PC6	
PC7	P7	CFCE2/PC7	
PC8	R7	TXD0/PCK2/PC8	
PC9	T7	RXD0/PCK3/PC9	
PC10	T8	RTS0/SCK0/PC10	
PC11	P8	CTS0/FIQ/PC11	
PC12	R8	TXD1/NCS6/PC12	
PC13	U8	RXD1/NCS7/PC13	
PC14	R9	TXD2/SPI1_NPCS2/PC14	
PC15	T9	RXD2/SPI1_NPCS3/PC15	
D16	P1	D16/TCLK0/PC16	
D17	N2	D17/TCLK1/PC17	
D18	M3	D18/TCLK2/PC18	
D19	R1	D19/TIOA0/PC19	
D20	T1	D20/TIOB0/PC20	
D21	R2	D21/TIOA1/PC21	
D22	P3	D22/TIOB1/PC22	
D23	T2	D23/TIOA2/PC23	
D24	P4	D24/TIOB2/PC24	
D25	U1	D25/TF2/PC25	
D26	T3	D26/TK2/PC26	
D27	R4	D27/TD2/PC27	
D28	P5	D28/RD2/PC28	
D29	R5	D29/RK2/PC29	
D30	P2	D30/RF2/PC30	
D31	N3	D31/PCK1/PC31	

D0	G1	D0	
D1	G2	D1	
D2	H1	D2	
D3	H2	D3	
D4	J1	D4	
D5	J2	D5	
D6	K1	D6	
D7	K4	D7	
D8	K2	D8	
D9	L1	D9	
D10	K3	D10	
D11	L2	D11	
D12	L3	D12	
D13	M1	D13	
D14	N1	D14	
D15	M2	D15	
		D8	A0
NBS0/A0		B8	A1
NWR2/NBS2/A1		A8	A2
A2		A7	A3
A3		B7	A4
A4		D7	A5
A5		A6	A6
A6		B6	A7
A7		C6	A8
A8		A5	A9
A9		D6	A10
A10		B5	A11
A11		A4	A12
A12		B4	A13
A13		A3	A14
A14		B3	A15
A15		A2	A16
BA0/A16		C4	A17
BA1/A17		B2	A18
A18		A1	A19
A19		B1	A20
A20		C2	A21
A21		C1	A22
A22			
RAS		F2	RAS
CAS		J4	CAS
SDWE		G3	SDWE
SDA10		F4	SDA10
SDCKE		F1	SDCKE
SDCK		H4	SDCK
NCS0		F4	NCS0
SDCS/NCS1		D2	SDCS_NCS1
NCS2		D1	NCS2
NANDCS/NCS3		G4	SMCS_NCS3
CFOE/NRD		E3	CFOE_NOE_NRD
CFWE/NWE/NWR0		E2	CFWE_NWE_NWR0
CFIOR/NBS1/NWR1		E1	CFIOR_NBS1_NWR1
CFIOW/NBS3/NWR3		F3	CFIOW_NBS3_NWR3
NRST		F15	NRST
TST		C10	
NC		A9	
NC		C14	
NC		D10	

3V3
R13 1K
R14 1K
BP1
RESET

DNP J7

SMB MALE

VDDOSC + VDDPLL CURRENT MEASURE

3V3 J8

C12 4.7NF R11 1,96K 1%
C13 470pF
C14 4.7NF R12 1,5K 1%
C15 470pF
C16 10PF S7
Y1 18.4320MHz
C17 10PF S8 S9
C18 100NF
C19 10PF
32.768 kHz Y2
C20 10PF
C21 100NF

Z14

CR1225
3V

MN10

R1100D121C
VDD GND OUT

J10
R15 1K
C126 100NF

WAKE UP

BP2

J9
1V2
R16 1,50M DNP
R17 100K

VDDBU
SHDN
WKUP

C22 100NF
C24 100NF
C26 100NF
C23 10µF 10V
C25 100NF
C27 100NF

J12
1V2
VDDCORE CURRENT MEASURE

C28 10µF 10V
C29 100NF
C31 100NF
C33 100NF
C35 100NF
C30 100NF
C32 100NF
C34 100NF

C36 100NF
C38 100NF
C40 100NF
C42 100NF
C37 100NF
C39 100NF
C41 100NF

3V3
C43 10µF 10V

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AT91SAM9261-EK
AT91SAM9261
SCALE 1/1
REV. C
SHEET 2/6

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EBI SDRAM INTERFACE

A[0..22]
D[0..31]
RAS
CAS
SDWE
SDA10
SDCKE
SDCK
CFIOR_NBS1_NWR1
CFIOW_NBS3_NWR3
SDCS_NCS1

MN4 MT48LC16M16A2 — 256 Mbits
MN5 MT48LC16M16A2 — 256 Mbits
3V3
R18 100K
S10
C50 100NF
C51 100NF
C52 100NF
C53 100NF
C44 100NF
C45 100NF
C46 100NF

DUAL FOOTPRINT

D[0..31]
PC[0..15]
3V3
R19 100K
S13
MN6A MT29F2G16AABWP — 2 Gbits
MN6B K9F1208U0A-Y — 512 Mbits
C60 100NF
C59 100NF

PA[0..31]
MN7 AT45DB321C-CNC
SPI0_MISO
SPI0_MOSI
SPI0_SPCK
SPI0_NPCS0
R20 100K
NRST
C58 100NF
S12
WRITE PROTECT NORMALLY OPEN
PA3
J21
R72 10K
SD CARD / MMC CARD DATAFLASH CARD INTERFACE
J22
MCDA1
SPI0_MISO MCDA0
SPI0_SPCK MCCK
SPI0_MOSI MCCDA
SPI0_NPCS3 MCDA3
MCDA2
FPS009
C115 100NF

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AT91SAM9261-EK
SDRAM & NANDFLASH
SCALE 1/1
REV. C
SHEET 3/6

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Note1: 8/16 bit DataBus selection; Removed R27 when using 16-bit mode; otherwise is 8-bit mode.

DM9000

MN8

DS2 GREEN LINK&ACT R21 1K
DS3 YELLOW FULL DUPLEX R22 1K
DS4 GREEN SPEED 100 R24 1K
R23 4,7K
R27 DNP 4,7K
R28 4,7K
R31 6,80K 1%
R32 100K
R34 4,7K

D[0..15]
A[0..22]
PC[0..15]
NRST
D15 D14 D13 D12 D11 D10 D9 D8
A2
PC11 FIQ S14
CFOE_NOE_NRD
CFWE_NWE_NWR0
NCS2 S15
D0 D1 D2 D3 D4 D5 D6 D7
PC10 RST
PC2 NWAIT S16
NOT USED

Y3 25MHz
C66 22PF
C67 22PF

VCCA
L1 742792093
C61 100NF
R25 49R9 1%
R26 49R9 1%
C62 100NF
C63 100NF
R29 49R9 1%
R30 49R9 1%
C64 100NF

J13 J0026D21
TD+ CT TD- RD+ CT RD-
TX+ TX- RX+ RX-
75 75 75 75
1nF

L2 4.7µH
C76 10µF 10V
C77 100NF
C78 10µF 10V
C79 100NF
R70 0R
R71 0R

C68 C69 C70 C71 C72 C73 100NF
C74 C75 100NF

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ROUSSET

AT91SAM9261-EK

ETHERNET

SCALE 1/1

REV. C

SHEET 4/6

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Z17 TX09D71VM1CCA

54132-4097

J23

X_RIGHT
Y_LOW
X_LEFT
Y_UP
Vctrl
PCI
VCTRL

B0 LCDD18 PB23
B1 LCDD19 PB24
B2 LCDD20 PB25
B3 LCDD21 PB26
B4 LCDD22 PB27
B5 LCDD23 PB28
G0 LCDD10 PB15
G1 LCDD11 PB16
G2 LCDD12 PB17
G3 LCDD13 PB18
G4 LCDD14 PB19
G5 LCDD15 PB20
R0 LCDD2 PB7
R1 LCDD3 PB8
R2 LCDD4 PB9
R3 LCDD5 PB10
R4 LCDD6 PB11
R5 LCDD7 PB12
DTMG LCDDEN PB3
HSYNC LCDHSYNC PB1
DCLK LCDDOTCK PB2

3V3
R75 10K
M5V
MN11
RST N.C
IN N.C
N.C N.C
GND N.C
MC34064D
C87 4.7NF
PA12 POWER CONTROL IN
Q6 IRLML2402
PB4 LCDCC
R83 10K
VCTRL
C84 100NF
PB[0..31]
C124 100NF
C125 10V 10µF

TOUCH SCREEN CONTROLLER

X_LEFT R73 0R
Y_UP R76 0R
X_RIGHT R77 0R
Y_LOW R78 0R
C116 10NF
C117 10NF
C118 10NF
C119 10NF
DNP
R80 100K
R81 100K
TP63
TP64
AGND
TP65
TP66
MN16
XP
YP
XM
YM
IN3
IN4
ADS7843E
DCLK
DIN
DOUT
CS
BUSY
PENIRQ
VREF
VCC
VCC
GND
3V3
R84 100K
R74 47R
PA12
PA2
PA1
PA0
PA28
PA11
PC2
S24
S25
S26
SPI0_SPCK
SPI0_MOSI
SPI0_MISO
SPI0_NPCS2
BUSY
IRQ0
PA[0..31]
PC[0..15]
R79 0R
L5 4.7µH
C120 10µF 10V
R82 0R
C122 100NF
C121 100NF
C123 100NF
TWO USER'S ANALOG INPUTS
Full-Scale Input Span 0 to VREF

PA[0..31]
PA27
BP3
PA26
BP4
PA25
BP5
PA24
BP6
3V3
GREEN
R50 220R
S19
PA14
DS7
GREEN
R51 220R
S20
PA13
DS8

USER INTERFACE

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ATMEL ROUSSET

AT91SAM9261-EK

LCD & USER'S INTERFACE

SCALE 1/1

REV. C

SHEET 5/6

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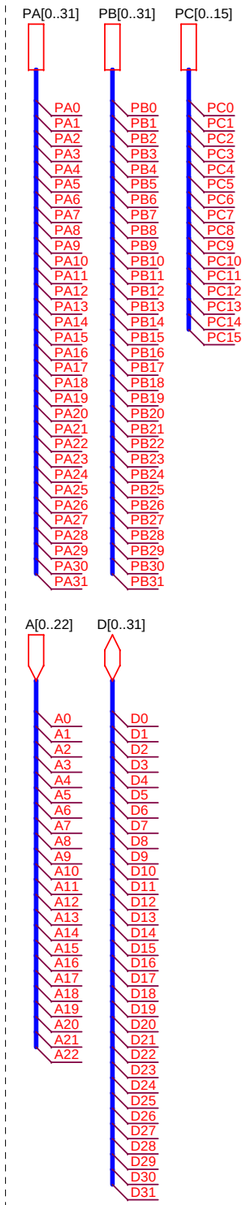
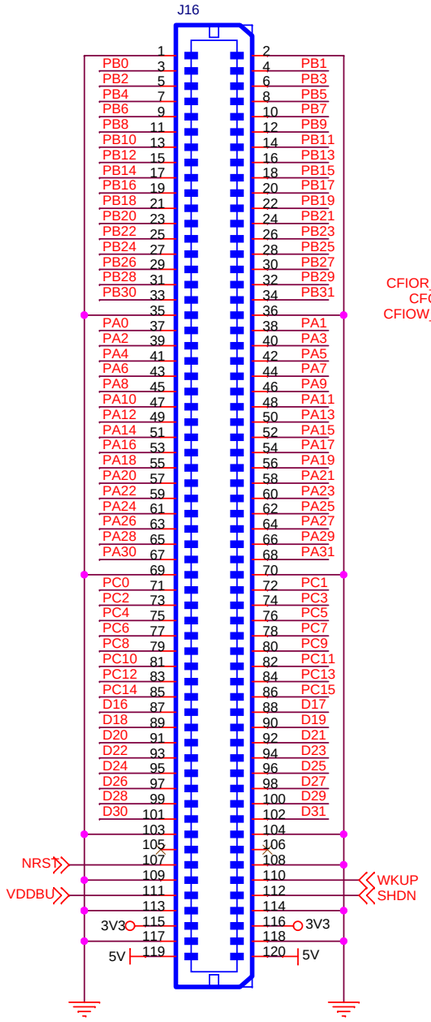
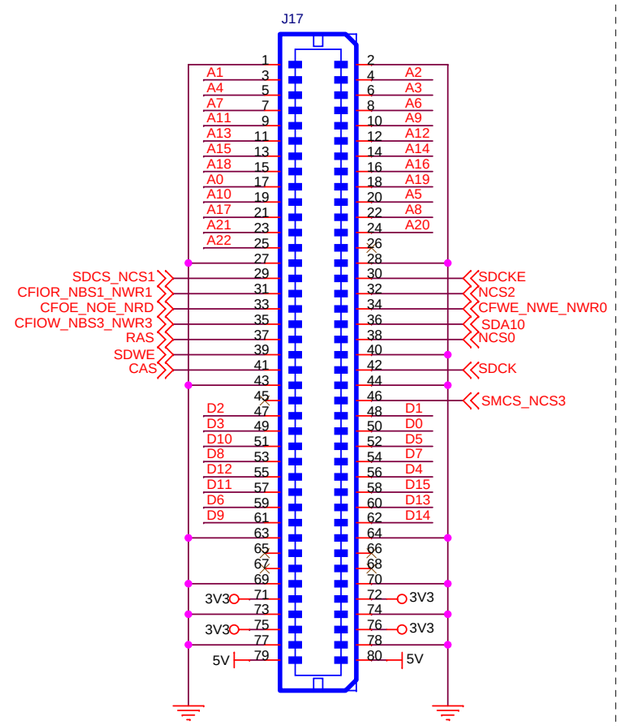
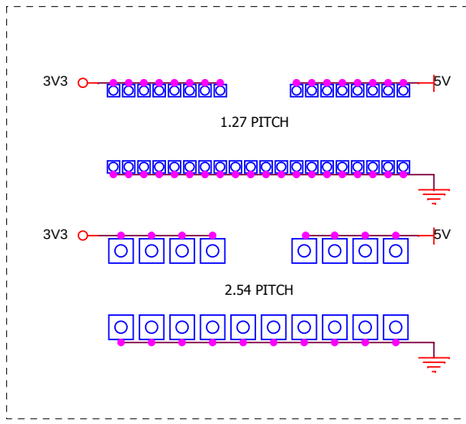
EXPANSION CONNECTORS

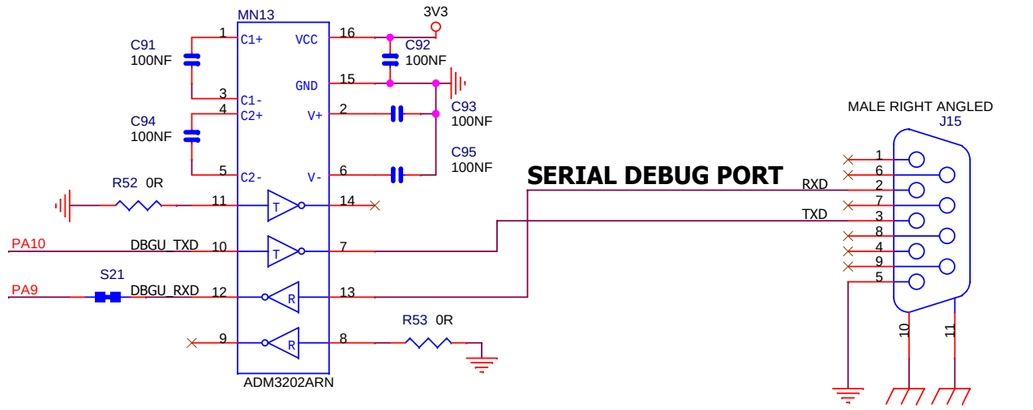


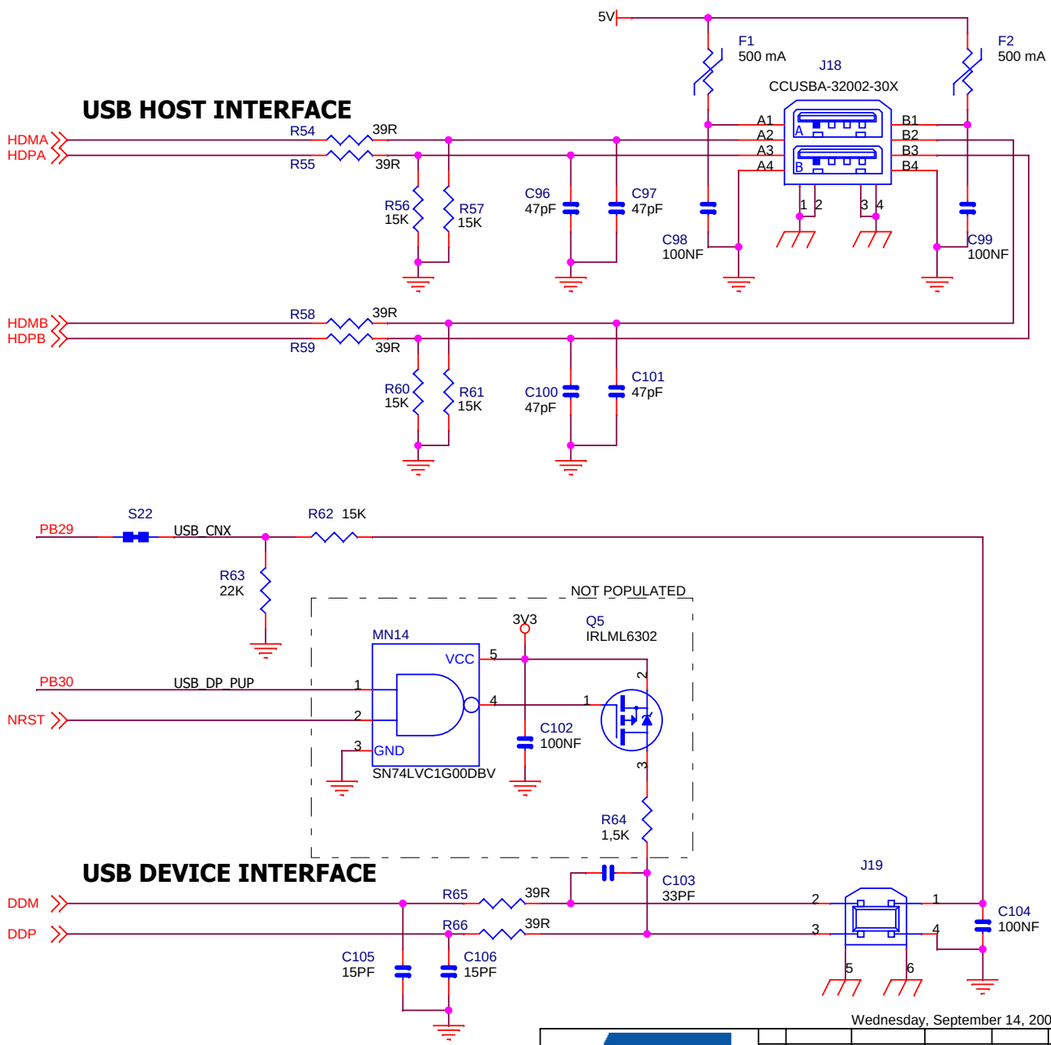




USER'S GRID AERA







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ATMEL ROUSSET

AT91SAM9261-EK

SERIAL & I/O EXPANSION

SCALE 1/1

REV. C

SHEET 6/6

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