ANALOG DEVICES

12 V/15 V, Serial Input Voltage Output, 16 Bit DAC

Preliminary Technical Data AD5570

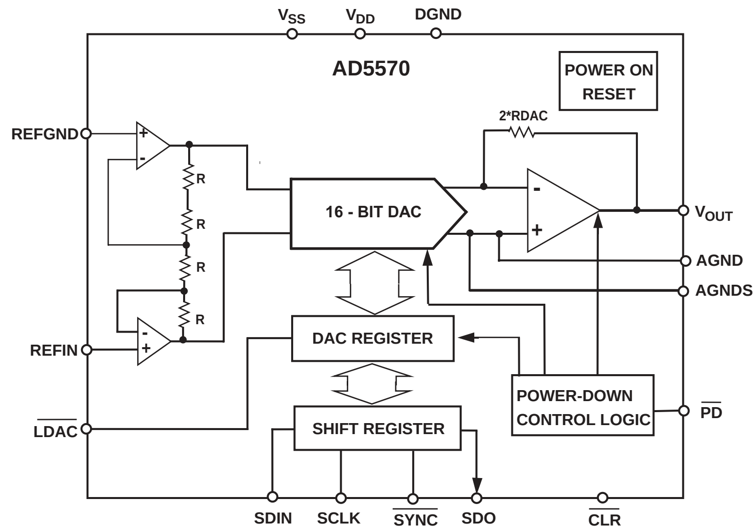
FEATURES

- Full 16-Bit Performance
- 1 LSB Max INL and DNL
- Maximum Output Voltage Range of ±10V
- Settling Time of 10μs max at 16 bits
- Clear Function to 0 V
- Asynchronous Update of Outputs (LDAC pin)
- Power On Reset
- Serial Data Output for Daisy Chaining
- Data Readback Facility
- Temperature Range -40°C to +125°C

APPLICATIONS

- Industrial Automation
- Automatic Test Equipment
- Process Control
- Data Acquisition Systems
- General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5570 is a single 16-bit serial input, voltage output DAC that operates from supply voltages of ±12 V up to ±15 V. INL and DNL are accurate to 1LSB (max) over the full temperature range of -40°C to +125°C.

The AD5570 utilizes a versatile three-wire interface that is compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards. Data is presented to the part in the format of a sixteen bit serial word. Serial Data is available on the SDO pin for daisy chaining purposes. Data Readback allows the user to read the contents of the DAC register via the SDO pin.

During power-up and power-down sequences (when the supply voltages are changing), V_{OUT} is clamped to 0 V via a low impedence path.

$\overline{\text{LDAC}}$ may be used to update the output of the DAC. A Power Down ($\overline{\text{PD}}$) pin allows the DAC to be put into a low power state, and a $\overline{\text{CLR}}$ pin allows the output to be cleared to 0 V.

The AD5570 is available in a 16-pin SSOP package.

PRODUCT HIGHLIGHTS

1. Buffered Voltage Output up to ±10V.
2. 1 LSB max INL and DNL
3. Wide Temperature Range of -40°C to +125°C.

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MICROWIRE is a trademark of National Semiconductor Corporation.

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AD5570–SPECIFICATIONS[1]

(V_{DD} = +11.4 V to +16.5 V ; V_{SS} = -11.4 V to -16.5 V; V_{REF} = 5V; GND = 0 V; R_L = 5 kΩ and C_L = 200 pF to GND. All specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A Grade	Units	Test Conditions/Comments
ACCURACY			
Resolution	16		Bits
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic Over Temperature
Zero-Scale Error	16	LSB max	
Full-Scale Error	16	LSB max	
Bipolar Zero Error	16	LSB max	
Gain Temperature Coefficient[2]	1	ppm FSR/°C typ	
	3	ppm FSR/°C max	
REFERENCE INPUT			
Reference Input Range	5	V max	
Input Current	1	μA max	
O/P CHARACTERISTICS			
Output Voltage Range	V_{DD} - 1.4 V	V max	
	V_{SS} + 1.4 V	V min	
Output Voltage Settling Time	10	μs max	At 16 bits to 0.5 LSB
Slew Rate	10	V/μs typ	Measured from 10% to 90%
Digital-to-Analog Glitch Impulse	12	nV-s typ	1 LSB Change around the Major Carry
DAC Output Impedance[2]	0.3	Ω max	
Digital Feedthrough	5	nV-s typ	
Power Supply Rejection Ratio	75	dB min	
LOGIC INPUTS			
Input Current	±1	μA max	
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.8	V max	
C_{IN}, Input Capacitance[2]	44	pF max	
Hysteresis Voltage	0.15	V typ	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1 mA
Floating-State Leakage Current	±1	μA max	
Floating-State O/P Capacitance	3	pF typ	
POWER REQUIREMENTS			
V_{DD}/V_{SS}	±11.4	V min	
	±16.5	V max	
I_{DD}	5	mA max	V_{OUT} Unloaded
I_{SS}	5	mA max	
Power-down Current	20	μA max	
Power Supply Sensitivity[3]	1	LSB/V max	
Power Dissipation	100	mW typ	V_{OUT} Unloaded

NOTES
[1]Temperature range: –40°C to +125°C.
[2]Guaranteed by design.
[3]Sensitivity of Gain Error and Bipolar Zero Error to V_{DD}, V_{SS} variations
Specifications subject to change without notice.

STANDALONE TIMING CHARACTERISTICS[1,2]

(V_{DD} = +12 V ±10%, V_{SS} = -12 V ±10% or V_{DD} = +15 V ±10%, V_{SS} =-15 V ±10%; V_{REF} = 5V; GND = 0 V; R_L = 5 kΩ and C_L = 200 pF to GND. All specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
f_{MAX}	8	MHz max	SCLK Frequency
t_1	125	ns min	SCLK cycle time
t_2	50	ns min	SCLK high time
t_3	50	ns min	SCLK low time
t_4	40	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	30	ns min	Data setup time
t_6	10	ns min	Data hold time
t_7	40	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	40	ns min	Min $\overline{SYNC}$ high time
t_9	0	ns min	$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge
t_{10}	40	ns min	$\overline{LDAC}$ Pulsewidth
t_{11}	0	ns min	$\overline{LDAC}$ Rising Edge to $\overline{SYNC}$ Falling Edge
t_{12}	20	ns min	SCLK Falling Edge to $\overline{LDAC}$ Rising Edge
t_{13}	0	ns min	SCLK Falling Edge to $\overline{LDAC}$ Falling Edge
t_{14}	40	ns min	$\overline{CLR}$ pulse width

[1] Guaranteed by design and characterization. Not production tested.
[2] All input signals are measured with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
Specifications subject to change without notice.

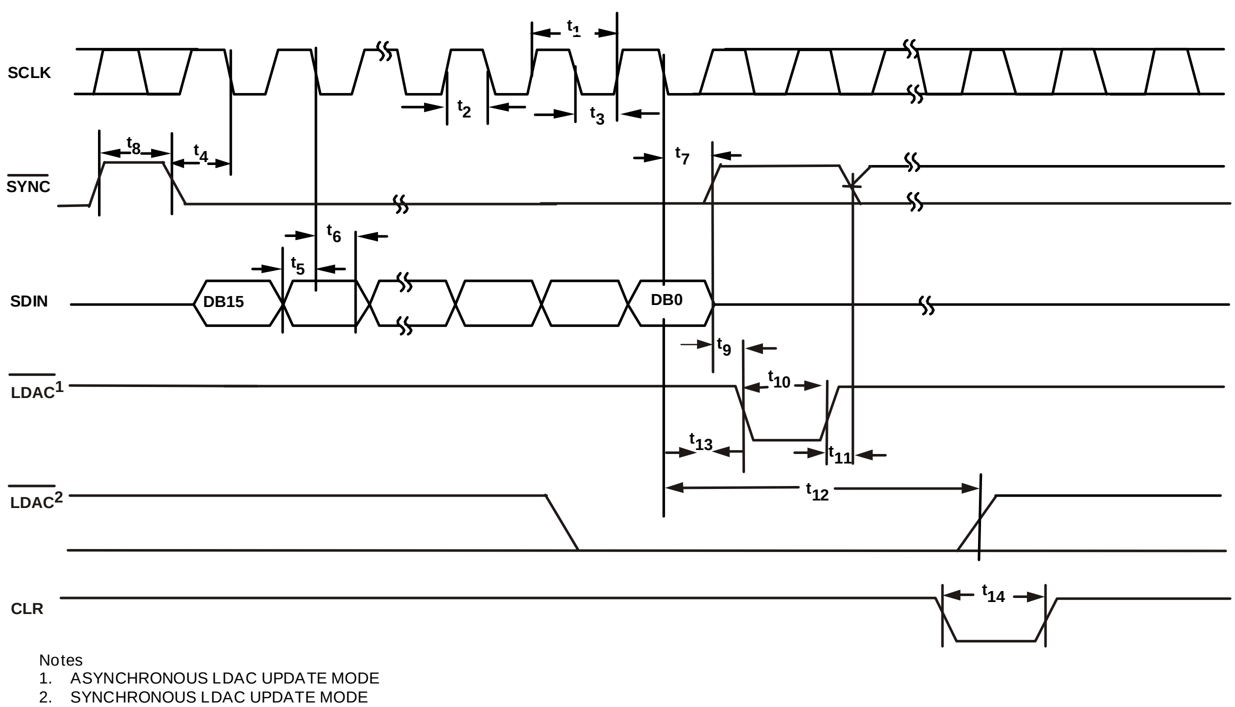


Figure 1. Serial Interface Timing Diagram

DAISY CHAINING AND READBACK TIMING CHARACTERISTICS[1,2,3]

(V_{DD} = +12 V ±10%, V_{SS} = -12 V ±10% or V_{DD} = +15 V ±10%, V_{SS} =-15 V ±10%; V_{REF} = 5V; GND = 0 V; R_L = 5 kΩ and C_L = 200 pF to GND. All specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
f_{MAX}	2	MHz max	SCLK Frequency
t_1	500	ns min	SCLK cycle time
t_2	200	ns min	SCLK high time
t_3	200	ns min	SCLK low time
t_4	40	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	30	ns min	Data setup time
t_6	10	ns min	Data hold time
t_7	40	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	40	ns min	Min $\overline{SYNC}$ high time
t_9	0	ns min	$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge
t_{10}	20	ns min	$\overline{LDAC}$ Pulsewidth
t_{11}	0	ns min	$\overline{LDAC}$ Rising Edge to $\overline{SYNC}$ Falling Edge
t_{15}	40	ns min	Data delay on $\overline{SDO}$

[1] Guaranteed by design and characterization. Not production tested.
[2] All input signals are measured with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] SDO; R_{PULLUP} = 5kΩ, C_L = 15pF.
Specifications subject to change without notice.

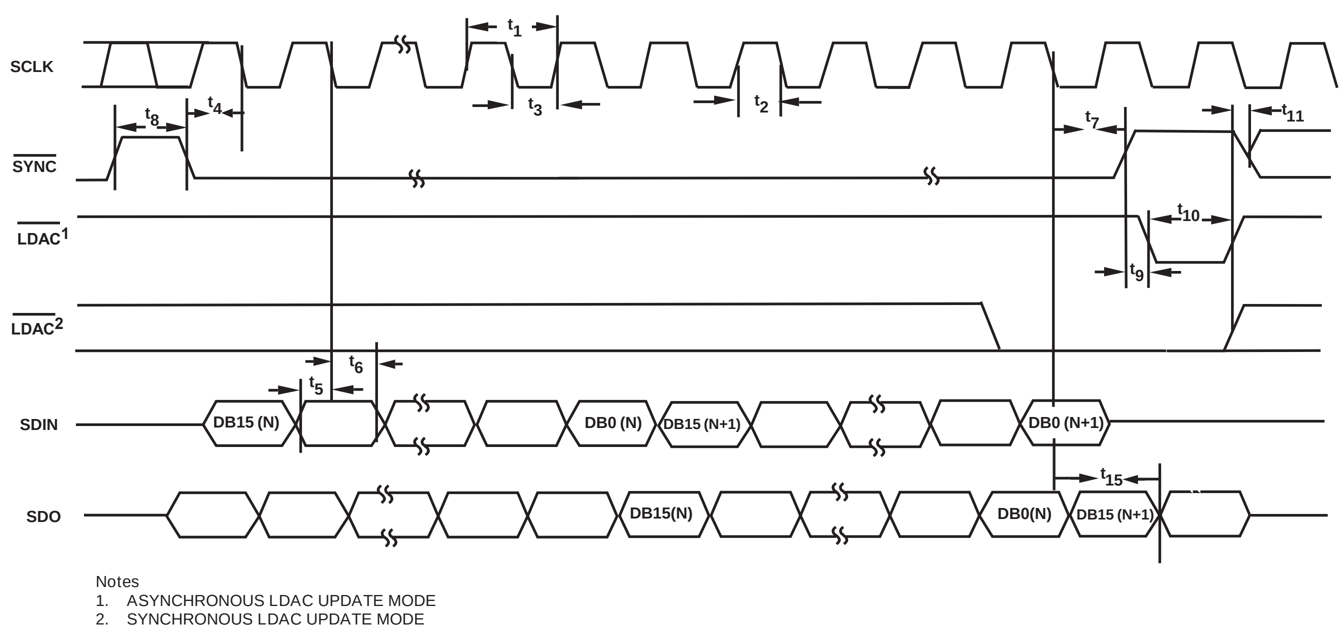


Figure 2. Daisy Chaining Timing Diagram

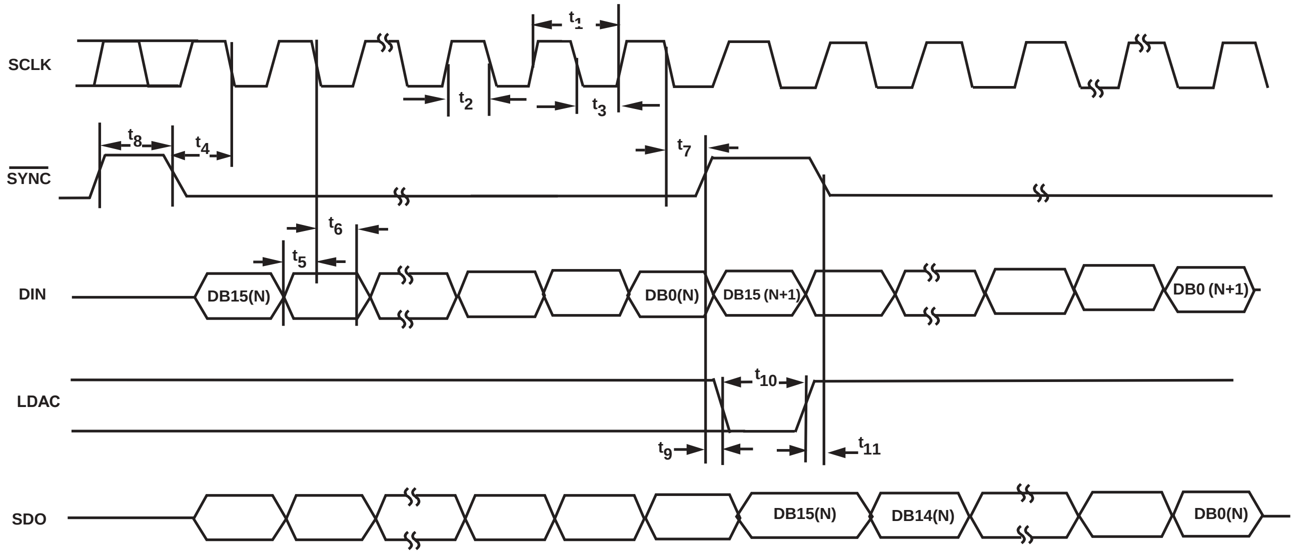


Figure 3. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND, DGND .... -0.3 V, +17 V
V_{SS} to AGND, DGND.............................+0.3 V, -17 V
AGND to DGND ....-0.3 V to V_{DD} to +0.3 V
REFOUT to AGND ....0 V to V_{DD}
REFIN to AGND ....-0.3 V to V_{DD} to +0.3 V
Digital Inputs to DGND.................-0.3V to V_{DD} +0.3 V
SDO to DGND .... -0.3V to +6.5 V
Operating Temperature Range .... –40°C to +125°C
Storage Temperature Range .... –65°C to +150°C
Maximum Junction Temperature, (T_J max) ....+150°C
16-Lead SSOP Package
  Power Dissipation .... (T_J max – T_A)/θ_{JA}
  θ_{JA} Thermal Impedance .... 139°C/W

Lead Temperature (Soldering 10s) ....300°C
IR Reflow, Peak Temperature ....+220°C

NOTES

[1]Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

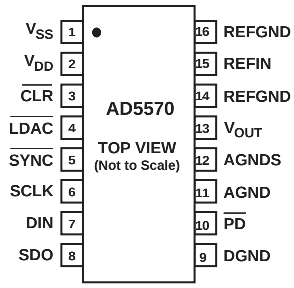
ORDERING GUIDE

Model	Temperature Range	Description	Package
AD5570YRS	-40 °C to +125 °C	Shrink SO package	RS-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5570 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESDprecautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
16 Lead SSOP
RS-16



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	VSS	Negative analog Supply Voltage, -12 V ±5% to -15 V ±10% for specified performance.
2	VDD	Positive analog Supply Voltage, +12 V ±5% to +15 V ±10% for specified performance.
3	$\overline{CLR}$	Level Sensitive, active low input. A falling edge of $\overline{CLR}$ resets V_{OUT} to AGND. The contents of the registers are untouched.
4	$\overline{LDAC}$	Active low control input that transfers the contents of the input register to the DAC register. $\overline{LDAC}$ may be tied permanently low enabling the outputs to be updated on the rising edge of $\overline{SYNC}$.
5	$\overline{SYNC}$	Active Low Control input. This is the frame synchronisation signal for the data. When $\overline{SYNC}$ goes low, it powers on the SCLK and SDIN buffers and enables the input shift register. Data is transfered in on the falling edges of the following 16 clocks.
6	SCLK	Serial Clock Input. Data is clocked into the input register on the falling edge of the serial clock input. Data can be transfered at rates up to 8 MHz.
7	SDIN	Serial Data input. This device has a 16-bit register. Data is clocked into the register on the falling edge of the serial clock input.
8	SDO	Serial Data Output that can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. This is an open-drain output; it should be pulled high with an external pull-up resistor.
9	DGND	Digital Ground. Ground reference for all digital circuitry.
10	$\overline{PD}$	Active low control input that allows the DAC to be put in a powerdown state.
11	AGND	Analog Ground. Ground reference for all analog circuitry.
12	AGNDS	Analog Ground Sense. This is normally tied to AGND.
13	VOUT	Analog output Voltage.
14	REFGND	This pin should be tied to 0 V.
15	REFIN	Voltage Reference Input. It is internally buffered before being applied to the DAC. For bipolar ±10 V output range, REFIN is 5 V.
16	REFGND	This pin should be tied to 0 V.

TERMINOLOGY

Relative Accuracy

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Monotonicity

A DAC is monotonic if the ouput either increases or remains constant for increasing digital inputs. The AD5570 is monotonic over its full operating temperature range.

Differential Non-Linearity

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Gain Error

Gain Error is the difference between the actual ans ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient

This is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero Scale Error

Zero Scale Error is the error in the DAC output voltage when all 0s are loaded into the DAC latch. Ideally, the output voltage, with all 0s in the DAC latch, should be equal to -2 V_{REF}. Zero-scale error is mainly due to offsets in the output amplifier.

Full Scale Error

This is the error in the DAC output voltage when all 1s are loaded to the DAC latch. Ideally the output voltage, with all 1s loaded into the DAC latch, should be 2 V_{REF} - 1 LSB.

Bipolar Zero Error

The deviation of the analog input from the ideal half-scale output of 0.0000V when the inputs are loaded with 8000H is called Bipolar Zero Error.

Output Voltage Settling Time

This is the amout of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the input code in the DAC register changes state. It is specified as the area of the glitch in nV-s and is measured when the digital input code changes by 1 LSB at the major carry transition.

Digital Feedthrough

Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{SYNC}$ is held high, while the CLK and SDIN signals are toggled. It is specified in nV-s and is measured with a full scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

Power Supply Rejection Ratio

This specification indicates how the output of the DAC is affected by changes in the power supply voltage.

GENERAL DESCRIPTION

The AD5570 is a single 16-bit, serial input, voltage output DAC. It operates from supply voltages of ±12 V to ±15 V, and has a buffered voltage output of up to ±10 V. Data is written to the AD5570 in a 16-bit word format, via a 3-wire serial interface. It also has an SDO pin which is available for daisy-chaining or readback.

The AD5570 incorporates a power-on-reset circuit which ensures that the DAC output powers up to 0V. The device also has a power-down pin which reduces the current consumption to 20 μA.

DAC Architecture

The DAC architecture of the AD5570 consists of a 16-bit current-mode segmented R-2R DAC. The simplified circuit diagram for the DAC section is shown in Figure 4. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of the 15 matched resistors to either AGND or IOUT. The remaining 12 bits of the data word drive switches S0 to S11 of the 12-bit R-2R ladder network.

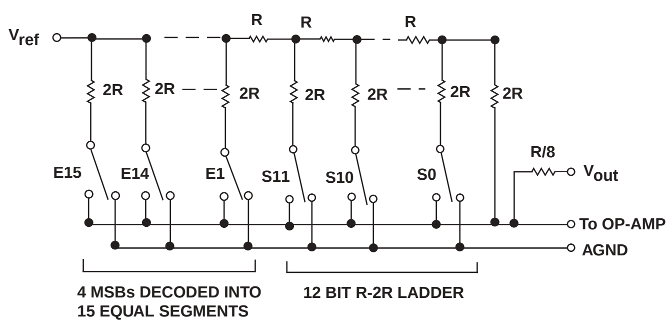


Figure 4. DAC Ladder Structure

Reference Buffers

The AD5570 operates with an external reference. The reference input (REFIN) has an input range of up to 5V. This input voltage is then used to provide a buffered positive and negative reference for the DAC core. The positive reference is given by

$$+V_{REF} = 2 \times V_{REFIN}$$

while the negative reference to the DAC core is

$$-V_{REF} = -2 \times V_{REFIN}$$

The reference buffers are shown in Figure 5 below.

SERIAL INTERFACE

The AD5570 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE and DSP interface standards.

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is shown in Figure 1.

Upon power-up, the input shift register and DAC register are loaded with midscale (8000H). The DAC coding is straight binary; all 0s produces an output of -2 V_{REF}; all 1s produces an output of +2 V_{REF} - 1 LSB.

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame synchronisation signal and chip enable. $\overline{SYNC}$ must frame the serial word being loaded into the device. Data can only be transfered into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low, observing the minimum $\overline{SYNC}$ to SCLK falling edge setup time, t4. After $\overline{SYNC}$ goes low, serial data on SDIN will be shifted into the device's input shift register on the falling edges of SCLK. $\overline{SYNC}$ may be taken high after the falling edge of the sixteenth SCLK pulse, observing the minimum SCLK falling edge to $\overline{SYNC}$ rising edge time, t7.

After the end of the serial data transfer, data will automatically be transferred from the input shift register to the input register of the DAC.

When data has been transfered into the input register of the DAC, the DAC register and DAC output can be updated by taking LDAC low while SYNC is high.

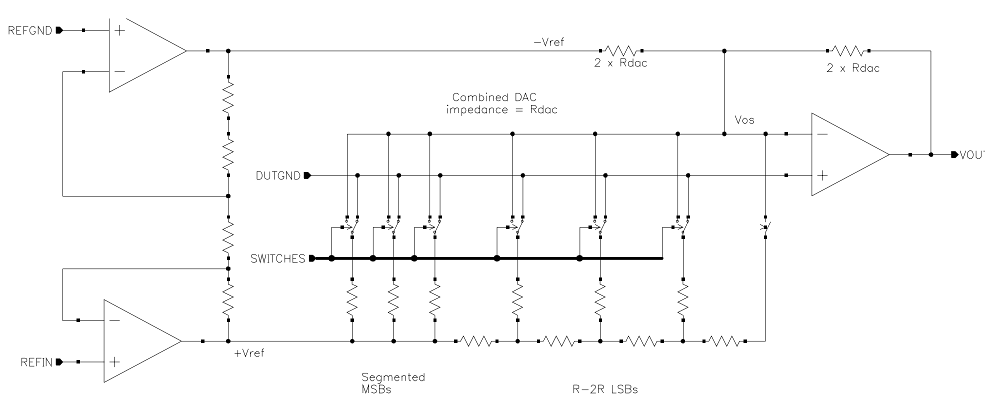


Figure 5. The voltage at VREFIN provides a buffered positive and negaitve reference for the DAC core

Load DAC Input (LDAC)

When data has been transfered into the input register of the DAC, there are two ways in which the corresponding DAC register and DAC output can be updated. Depending on the status of both SYNC and LDAC, one of two update modes is selected.

Synchronous LDAC: Here, LDAC is low while data is being clocked into the input shift register. The DAC output is updated when SYNC is taken high. The update here occurs on the rising edge of SYNC.

Asychronous LDAC: In this case, LDAC is high while data is being clocked in. The DAC output is updated by taking LDAC low any time after SYNC has been taken high. The update now occurs on the falling edge of LDAC.

Figure 6 shows a simplified block diagram of the input loading circuitry.

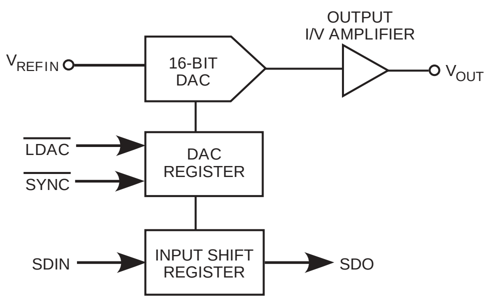


Figure 6. Simplified Serial Interface

Daisy Chaining

This mode of operation is designed for multi-DAC systems where several AD5570s may be connected in cascade as shown in figure 7. This is done by connecting the control inputs in parallel, and then daisy-chaining the SDIN and SDO I/O's of each device. Also, an external pull-up resistor of ~5 kΩ on SDO is required when using the part in daisy-chain mode.

As before, when SYNC goes low, serial data on SDIN will be shifted into the input shift register on the rising edge of SCLK. If more than 16 clock pulses are applied, the data ripples out of the shift resister and appears on the SDO line. By connecting this line to the SDIN input on the next AD5570 in the chain, a multi-DAC interface may be constructed.

One data transfer cycle of sixteen SCLK pulses is required for each DAC in the system. Therefore, the total number of clock cycles must equal 16N where N is the total number of devices in the chain. The first data transfer cycle written into the chain will appear at the last DAC in the system on the final data transfer cycle.

When the serial transfer to all devices is complete, SYNC should be taken high. This prevents any further data being clocked into the device.

A continuous SCLK source may be used if it can be arranged that SYNC is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and SYNC taken high some time later.

The outputs of all the DACs in the system can be updated simultaneously using the LDAC signal.

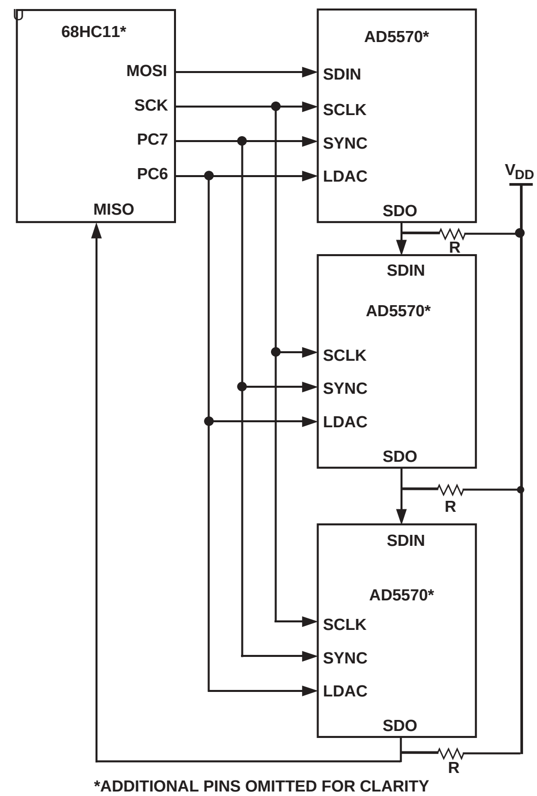


Figure 7. Daisy-chaining using the AD5570

Readback

The AD5570 allows the data contained in the DAC resigter to be readback if required. As with daisy-chaining, an external pull-up resistor of ~5 KΩ on SDO is required. The data in the DAC register is available on SDO on the falling edges of SCLK when SYNC is low. On the 16th SCLK edge, SDO is updated to repeat SDIN with a delay of 16 clock cycles.

In order to readback the contents of the DAC register without writing to the part, SYNC should be taken low while LDAC is held high.

Daisy-chaining readback is also possible, since SDO containing the DAC data passes through the DAC chain with the appropriate latency.

Power-on Reset

The AD5570 contains a power-on-Reset circuit that controls the output during power-up and power-down. This is useful in applications where the known state of the output of the DAC during power up is important. On power up and powerdown, the output of the DAC, V_{OUT}, is held at AGND.

TRANSFER FUNCTION

Table 1 below shows the ideal input code to output voltage relationship for the AD5570.

Binary Code Table

Digital Input MSB			LSB	Analog Output V_{OUT}
1111	1111	1111	1111	$+2V_{REF}$ x (32,767/32,768)
1000	0000	0000	0001	$+2V_{REF}$ x (1/32,768)
1000	0000	0000	0000	0 V
0111	1111	1111	1111	$-2V_{REF}$ x (1/32,768)
0000	0000	0000	0000	$-2V_{REF}$

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).