

System Reset

Monolithic IC PST591~595 Series

Outline

These ICs function in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted, and has a built-in fixed delay time generating circuit. This series has been represented in the past by PST574/PST575, but these new low reset type system reset ICs expand the delay time series with a counter timer using an analog/digital hybrid circuit.

Features

- | | | |
|---|--|--|
| 1. Fixed delay time setting by counter timer | Excellent delay time temperature characteristics | $\pm 800\text{ppm}/^{\circ}\text{C}$ |
| 2. Low operating limit voltage | | 0.65V typ. |
| 3. Hysteresis voltage provided in detection voltage | | 50mV typ. |
| 4. Current consumption for no-load | | $I_{\text{OCL}}=300\mu\text{A typ.}$ $I_{\text{OCH}}=200\mu\text{A typ.}$ |
| 5. 5 delay time products available | | <div> <div>PST591 50mS</div> <div>PST592 100mS</div> <div>PST593 200mS</div> </div> <div> <div>PST594 400mS</div> <div>PST595 800mS</div> </div> |
| 6. Each product has 9 detection voltage ranks. | | <div> <div>C : 4.5V typ.</div> <div>D : 4.2V typ.</div> <div>E : 3.9V typ.</div> <div>F : 3.6V typ.</div> <div>G : 3.3V typ.</div> </div> <div> <div>H : 3.1V typ.</div> <div>I : 2.9V typ.</div> <div>J : 2.7V typ.</div> <div>K : 2.5V typ.</div> </div> |

Package

MMP-4A (PST59×□M)

TO-92A (PST59×□)

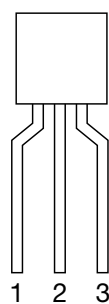
*□ contains detection voltage rank.

(MMP-4A has a manual reset pin, which should be set at GND or NC during normal operation.)

Applications

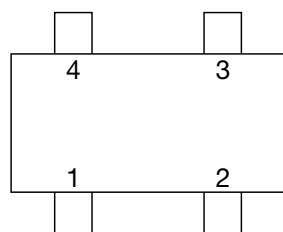
- Reset circuits in microcomputers, CPUs and MPUs
- Logic circuit reset circuits.
- Battery voltage check circuits.
- Back-up power supply switching circuits.
- Level detection circuits.
- Mechanical reset circuits

Pin Assignment



TO-92A

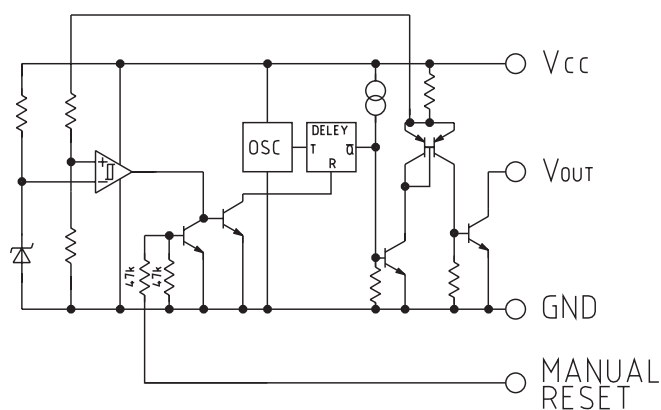
1	V _{CC}
2	GND
3	V _{OUT}



MMP-4A

1	V _{OUT}
2	Manual Reset
3	V _{CC}
4	GND

Equivalent Circuit Diagram



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC} max.	-0.3~10	V
Manual reset input voltage	V _{RES} max.	-0.3~10	V
Allowable loss	P _d	200 (MMP-4P) 300 (TO-92)	mW

Electrical Characteristics (Ta=25°C) (Except where noted otherwise, resistance unit isΩ)

Item	Symbol	Measuring circuit	Measurement conditions	Min.	Typ.	Max.	Unit
Detection voltage	Vs	1	$R_L=470$ $V_{OL} \leq 0.4V$ $V_{CC}=H \rightarrow L$	C	4.3	4.5	4.7
				D	4.0	4.2	4.4
				E	3.7	3.9	4.1
				F	3.4	3.6	3.8
				G	3.1	3.3	3.5
				H	2.9	3.1	3.3
				I	2.75	2.90	3.05
				J	2.55	2.70	2.85
				K	2.35	2.50	2.65
Hysteresis voltage	ΔV_S	1	$R_L=470, V_{CC}=L \rightarrow H \rightarrow L$	30	50	100	mV
Detection voltage temperature coefficient	$V_S / \Delta T$	1	$R_L=470, T_a=-20^\circ C \sim +75^\circ C$		± 0.01		%/°C
Low-level output voltage	V_{OL}	1	$V_{CC}=V_S \text{ min.} - 0.05V, R_L=470$		0.1	0.4	V
Output leakage current	I_{OH}	1	$V_{CC}=10V$			± 0.1	μA
Circuit current while on	I_{CCL}	1	$V_{CC}=V_S \text{ min.} - 0.05V, R_L=\infty$		300	600	μA
Circuit current while off	I_{CCH}	1	$V_{CC}=V_S \text{ typ.} / 0.85V, R_L=\infty$		200	350	μA
"H" transport delay time	t_{PLH}	2	$R_L=4.7k$ $C_L=100PF \star 1$	PST591	30	50	75
				PST592	60	100	150
				PST593	120	200	300
				PST594	240	400	600
				PST595	480	800	1200
"L" transport delay time	t_{PHL}	2	$R_L=4.7k, C_L=100PF \star 1$		10		μS
Operating power supply voltage	V_{OPL}	1	$R_L=4.7k, V_{OL} \leq 0.4V$		0.65	0.85	V
Output current while on 1	I_{OL1}	1	$V_{CC}=V_S \text{ min.} - 0.05V, R_L=0$	8			mA
Output current while on 2	I_{OL2}	1	$T_a=-20^\circ C \sim +75^\circ C, R_L=0 \star 2$	6			mA
Manual reset pin	Input high voltage	V_{RESH}		2.0			V
	Input high current	V_{RESH}	$V_{RES}=2V$			80	μA
	Input low voltage	V_{RESL}				0.8	V

*1 t_{PLH} : $V_{CC}=(V_S \text{ typ.} - 0.4V) \rightarrow (V_S \text{ typ.} + 0.4V)$, t_{PHL} : $V_{CC}=(V_S \text{ typ.} + 0.4V) \rightarrow (V_S \text{ typ.} - 0.4V)$

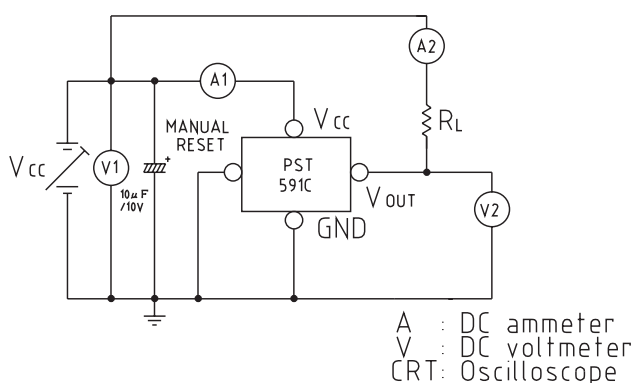
*2 $V_{CC}=V_S \text{ min.} - 0.15V$

Note 3: V_{OUT} pin is low when manual reset pin is high.

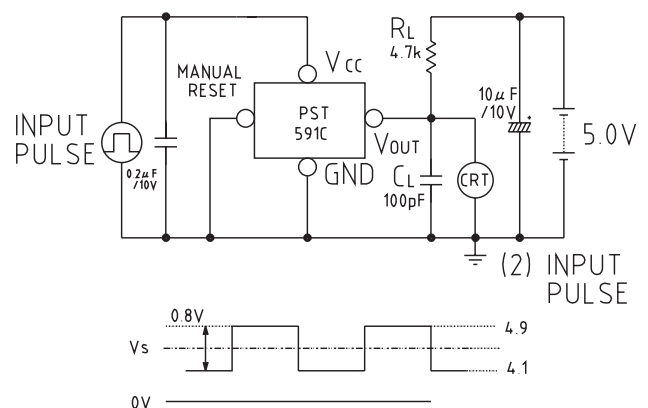
V_{OUT} pin is high when manual reset pin is low.

Measuring Circuit

[1]



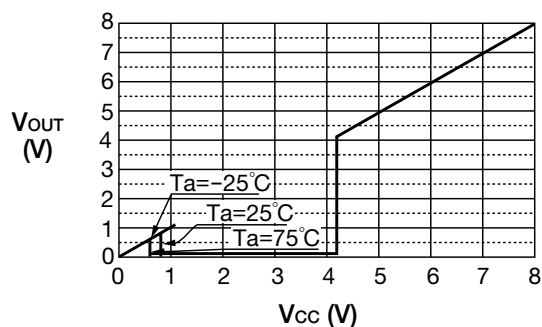
[2]



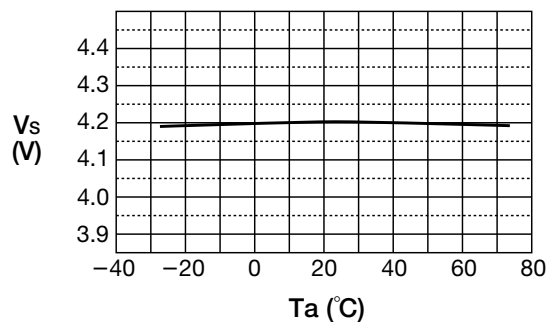
Note: Input model is an example for PST591C.

Characteristics (Example: PST591D)

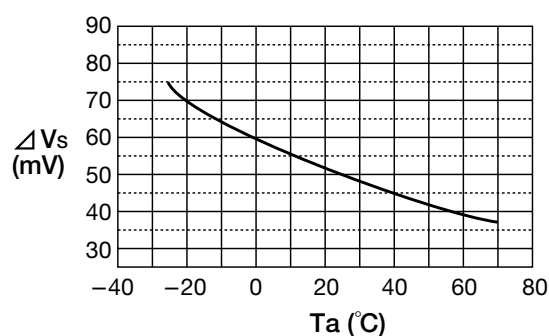
V_{CC} vs. V_{OUT}



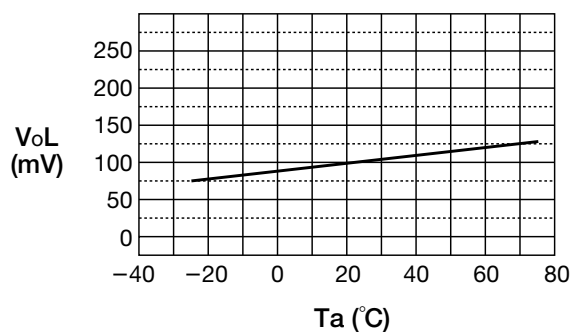
V_S vs. T_a



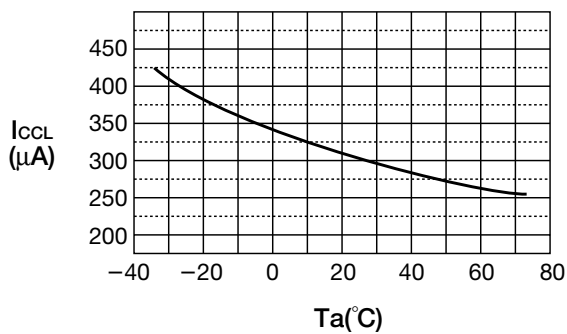
ΔV_S vs. T_a



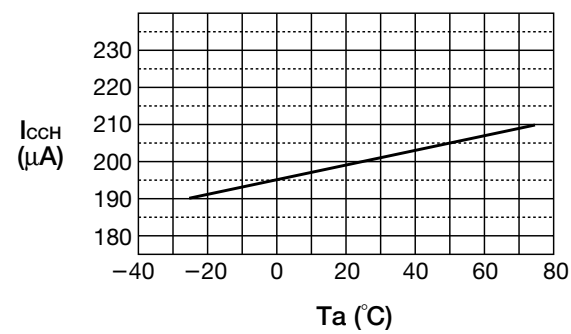
V_{OL} vs. T_a



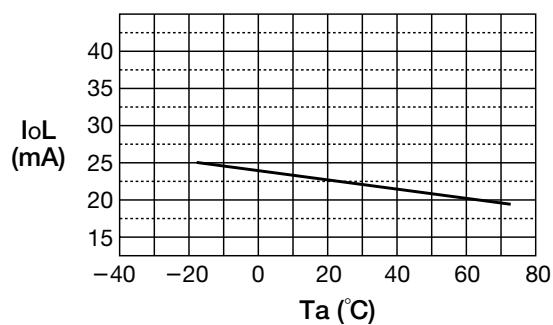
I_{CCL} vs. T_a



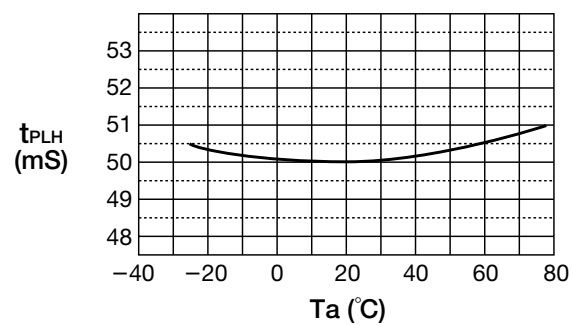
I_{CCH} vs. T_a



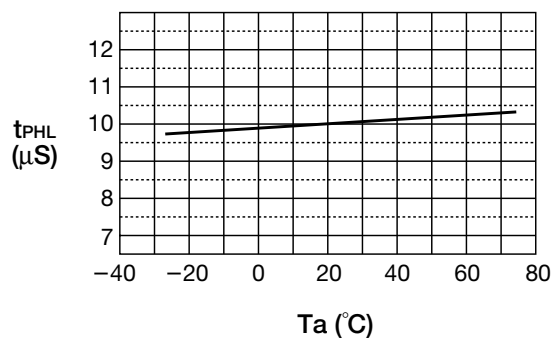
I_{OL} vs. T_a



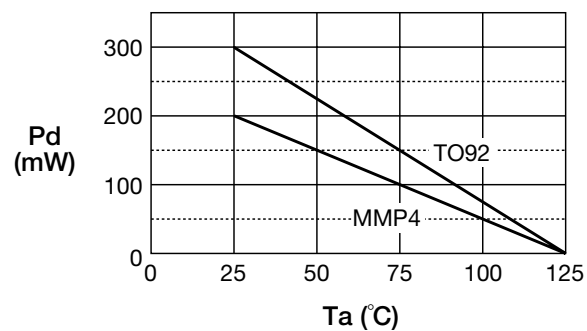
t_{PLH} vs. T_a



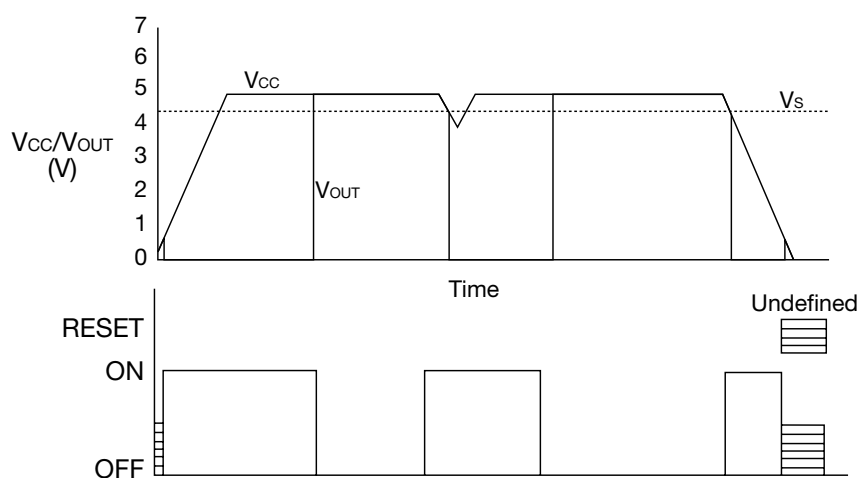
t_{PHL} vs. Ta



Pd vs. Ta

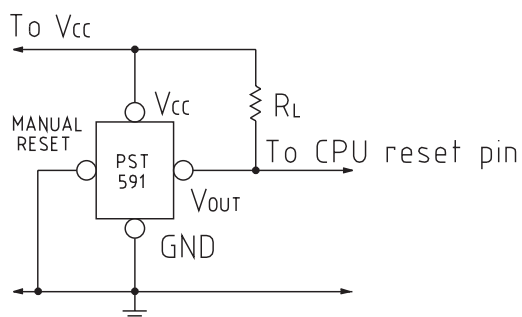


Timing Chart



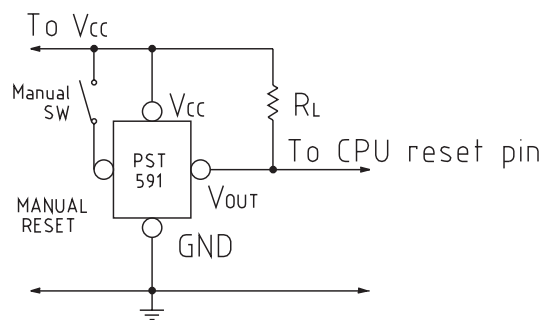
Application circuits

1. Normal hard reset



Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.

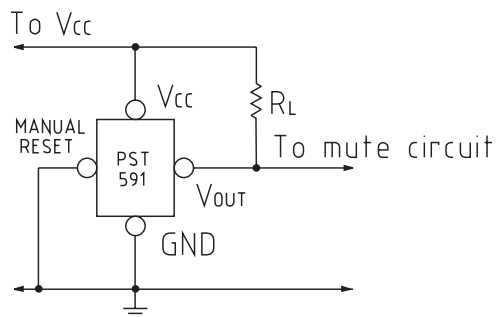
2. Manual reset



V_{OUT} pin low for manual switch ON.
V_{OUT} pin high for manual switch OFF.

Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.

3. Mute circuit



Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.