

## FEATURES

- Readback Capability for all DACs
- On-Chip Latches for All DACs
- Linearity Grades to  $\pm 1/8$  LSB
- Single Supply Voltage (5 Volt)
- DACs Matched to 1%
- Four Quadrant Multiplication
- Microprocessor TTL/CMOS Compatible
- Latch-Up Free
- Dual Version: MP7529B

## APPLICATIONS

- Microprocessor Controlled Gain and Attenuation Circuits
- Microprocessor Controlled/Programmable Power Supplies
- Hardware Redundant Applications Requiring Data Readback

## GENERAL DESCRIPTION

The MP7628 is a quad 8-bit Digital-to-Analog Converter designed using a decoded DAC architecture featuring excellent DAC-to-DAC matching and guaranteed monotonicity.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

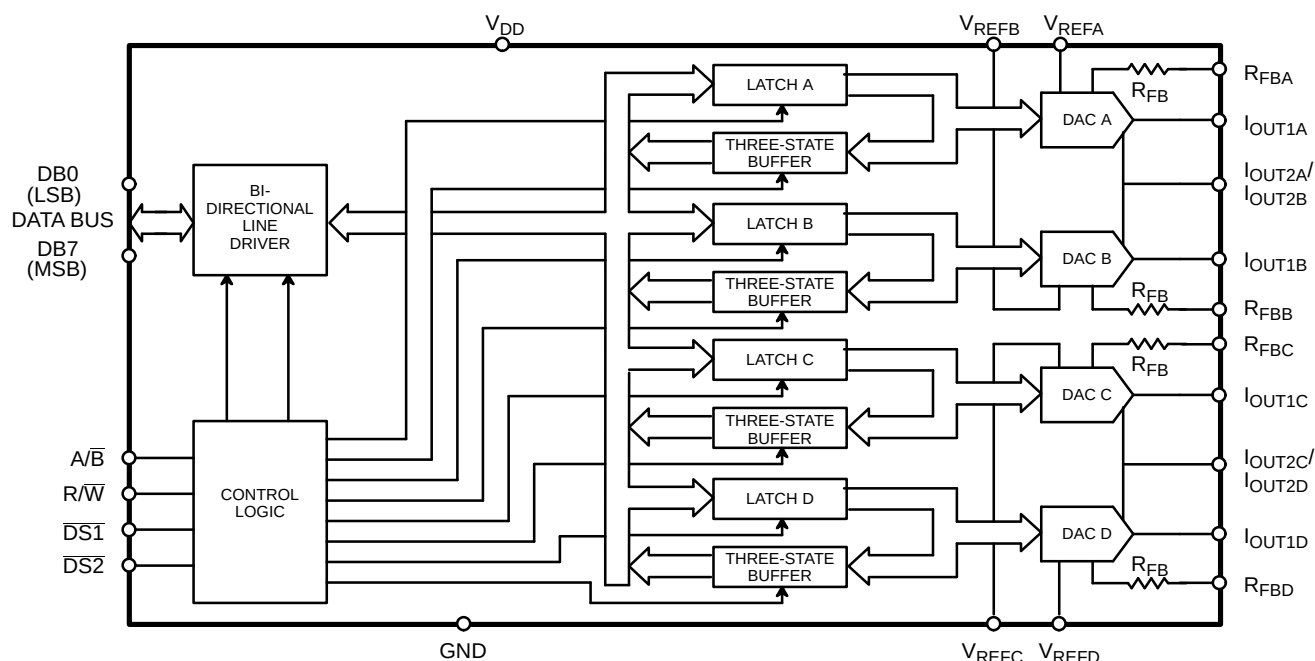
The readback function allows the user to poll or read the data latches, eliminating the need for storing information in RAM. In the event the microprocessor power supply is interrupted, it can poll the DACs to establish the last known system state.

Data is transferred into any of the four DAC data latches via common 8-bit TTL/CMOS compatible input port. Control inputs  $\overline{DS1}$ ,  $\overline{DS2}$  and  $A/\overline{B}$  determine which DAC is to be loaded. The MP7628's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors.

The device operates at +5 V power supply and dissipates less than 5mW.

All DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

## SIMPLIFIED BLOCK DIAGRAM



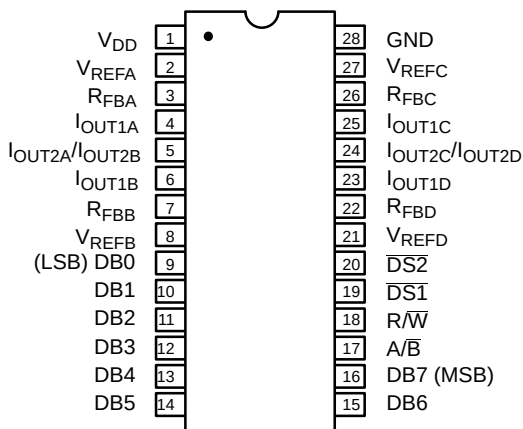
## ORDERING INFORMATION

| Package Type | Temperature Range | Part No.  | INL (LSB) | DNL (LSB) | Gain Error (% FSR) |
|--------------|-------------------|-----------|-----------|-----------|--------------------|
| Plastic Dip  | -40 to +85°C      | MP7628JN  | $\pm 1/2$ | $\pm 1/2$ | $\pm 1.8$          |
| Plastic Dip  | -40 to +85°C      | MP7628KN  | $\pm 1/4$ | $\pm 1/4$ | $\pm 0.9$          |
| SOIC         | -40 to +85°C      | MP7628JS  | $\pm 1/2$ | $\pm 1/2$ | $\pm 1.8$          |
| SOIC         | -40 to +85°C      | MP7628KS  | $\pm 1/4$ | $\pm 1/4$ | $\pm 0.9$          |
| PLCC         | -40 to +85°C      | MP7628JP  | $\pm 1/2$ | $\pm 1/2$ | $\pm 1.8$          |
| PLCC         | -40 to +85°C      | MP7628KP  | $\pm 1/4$ | $\pm 1/4$ | $\pm 0.9$          |
| Ceramic Dip  | -40 to +85°C      | MP7628AD  | $\pm 1/2$ | $\pm 1/2$ | $\pm 1.8$          |
| Ceramic Dip  | -40 to +85°C      | MP7628BD  | $\pm 1/4$ | $\pm 1/4$ | $\pm 0.9$          |
| Ceramic Dip  | -55 to +125°C     | MP7628SD* | $\pm 1/2$ | $\pm 1/2$ | $\pm 1.8$          |
| Ceramic Dip  | -55 to +125°C     | MP7628TD* | $\pm 1/4$ | $\pm 1/4$ | $\pm 0.9$          |

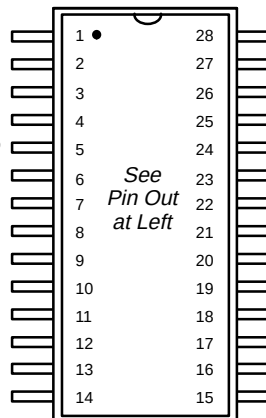
\*Contact factory for non-compliant military processing

## PIN CONFIGURATIONS

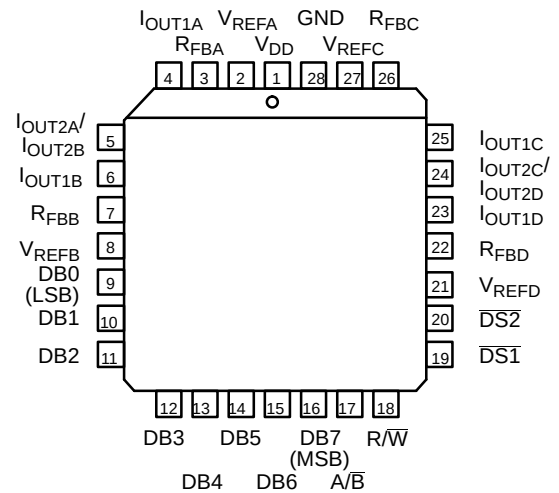
See Packaging Section for  
Package Dimensions



28 Pin CDIP, PDIP (0.600")  
D28, N28



28 Pin SOIC (Jedec, 0.300")  
S28



28 Pin PLCC  
P28

## PIN OUT DEFINITIONS

| PIN NO. | NAME                                       | DESCRIPTION                  |
|---------|--------------------------------------------|------------------------------|
| 1       | V <sub>DD</sub>                            | Power Supply                 |
| 2       | V <sub>REFA</sub>                          | Reference Voltage for DAC A  |
| 3       | R <sub>FBA</sub>                           | Feedback Resistor for DAC A  |
| 4       | I <sub>OUT1A</sub>                         | Current Output 1 DAC A       |
| 5       | I <sub>OUT2A</sub> /<br>I <sub>OUT2B</sub> | Current Output 2 DAC A/DAC B |
| 6       | I <sub>OUT1B</sub>                         | Current Output 1 DAC B       |
| 7       | R <sub>FBB</sub>                           | Feedback Resistor for DAC B  |
| 8       | V <sub>REFB</sub>                          | Reference Voltage for DAC B  |
| 9       | DB0                                        | Data Input Bit 0 (LSB)       |
| 10      | DB1                                        | Data Input Bit 1             |
| 11      | DB2                                        | Data Input Bit 2             |
| 12      | DB3                                        | Data Input Bit 3             |
| 13      | DB4                                        | Data Input Bit 4             |
| 14      | DB5                                        | Data Input Bit 5             |
| 15      | DB6                                        | Data Input Bit 6             |
| 16      | DB7                                        | Data Input Bit 7 (MSB)       |
| 17      | A/ $\overline{B}$                          | DAC Selection                |
| 18      | R/ $\overline{W}$                          | Read/Write                   |
| 19      | $\overline{DS1}$                           | Control 1                    |
| 20      | $\overline{DS2}$                           | Control 2                    |
| 21      | V <sub>REFD</sub>                          | Reference Voltage for DAC D  |
| 22      | R <sub>FBD</sub>                           | Feedback Resistor for DAC D  |
| 23      | I <sub>OUT1D</sub>                         | Current Output 1 DAC D       |
| 24      | I <sub>OUT2C</sub> /<br>I <sub>OUT2D</sub> | Current Output 2 DAC C/DAC D |
| 25      | I <sub>OUT1C</sub>                         | Current Output 1 DAC C       |
| 26      | R <sub>FBC</sub>                           | Feedback Resistor for DAC C  |
| 27      | V <sub>REFC</sub>                          | Reference Voltage for DAC C  |
| 28      | GND                                        | Ground                       |

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = +5\text{ V}$ ,  $V_{REF} = +10\text{ V}$  unless otherwise noted)

| Parameter                                  | Symbol     | 25°C |     |           | Tmin to Tmax |  | Units         | Test Conditions/Comments                                      |
|--------------------------------------------|------------|------|-----|-----------|--------------|--|---------------|---------------------------------------------------------------|
| Min                                        | Typ        | Max  | Min | Max       |              |  |               |                                                               |
| <b>STATIC PERFORMANCE<sup>1</sup></b>      |            |      |     |           |              |  |               |                                                               |
| Resolution (All Grades)                    | N          | 8    |     |           | 8            |  | Bits          | FSR = Full Scale Range                                        |
| Integral Non-Linearity (Relative Accuracy) | INL        |      |     |           |              |  | LSB           | End Point Linearity Spec.                                     |
| J, A, S                                    |            |      |     | $\pm 1/2$ |              |  | $\pm 1/2$     |                                                               |
| K, B, T                                    |            |      |     | $\pm 1/4$ |              |  | $\pm 1/4$     |                                                               |
| Differential Non-Linearity                 | DNL        |      |     |           |              |  | LSB           | All grades monotonic over full temperature range.             |
| J, A, S                                    |            |      |     | $\pm 1/2$ |              |  | $\pm 1/2$     |                                                               |
| K, B, T                                    |            |      |     | $\pm 1/4$ |              |  | $\pm 1/4$     |                                                               |
| Gain Error                                 | GE         |      |     |           |              |  | % FSR         | Using Internal $R_{FB}$                                       |
| J, A, S                                    |            |      |     | $\pm 1.5$ |              |  | $\pm 1.8$     | Digital Inputs = $V_{INH}$                                    |
| K, B, T                                    |            |      |     | $\pm 0.8$ |              |  | $\pm 0.9$     |                                                               |
| Gain Temperature Coefficient <sup>2</sup>  | $TC_{GE}$  |      |     |           |              |  | ppm/°C        | $\Delta\text{Gain}/\Delta\text{Temperature}$                  |
| Power Supply Rejection Ratio               | PSRR       |      |     | $\pm 200$ |              |  | ppm/%         | $ \Delta\text{Gain}/\Delta V_{DD} $ $\Delta V_{DD} = \pm 5\%$ |
|                                            |            |      |     |           |              |  |               | Digital Inputs = $V_{INH}$                                    |
| Output Leakage Current (all)               | $I_{OUT1}$ |      |     | $\pm 50$  |              |  | nA            | Digital Inputs = $V_{INL}$                                    |
| <b>REFERENCE INPUT</b>                     |            |      |     |           |              |  |               |                                                               |
| Voltage Range <sup>2</sup>                 |            |      |     | $\pm 20$  |              |  | V             |                                                               |
| Input Resistance                           | $R_{IN}$   | 12   |     | 28        | 12           |  | k $\Omega$    |                                                               |
| <b>DIGITAL INPUTS<sup>3</sup></b>          |            |      |     |           |              |  |               |                                                               |
| Logic Thresholds                           |            |      |     |           |              |  |               |                                                               |
| $V_{INH}$                                  |            | 2.4  |     |           | 2.4          |  | V             |                                                               |
| $V_{INL}$                                  |            |      |     | 0.8       |              |  | V             |                                                               |
| Input Leakage Current                      | $I_{LKG}$  |      |     | $\pm 1$   |              |  | $\mu\text{A}$ |                                                               |
| Input Capacitance <sup>2</sup>             | $C_{IN}$   |      | 3   |           |              |  | pF            |                                                               |
| <b>DATA BUS OUTPUTS</b>                    |            |      |     |           |              |  |               |                                                               |
| Output Capacitance <sup>2</sup>            | $C_{OUT}$  |      | 7   |           |              |  | pF            |                                                               |
| Input Leakage Current                      | $I_{LKG}$  |      |     | $\pm 1$   |              |  | $\mu\text{A}$ |                                                               |
| <b>ANALOG OUTPUTS</b>                      |            |      |     |           |              |  |               |                                                               |
| Propagation Delay <sup>2</sup>             |            | 500  |     |           | 750          |  | ns            | From digital input to 90% of final analog output current      |
| Output Capacitance <sup>2</sup>            | $C_{OUT}$  |      | 120 |           |              |  | pF            | DAC Inputs all 1's                                            |
|                                            | $C_{OUT}$  |      | 80  |           |              |  | pF            | DAC Inputs all 0's                                            |
| Glitch Energy <sup>2</sup>                 |            | 160  |     |           | 440          |  | nVs           | Typical for code transition from all 0's to all 1's           |

## ELECTRICAL CHARACTERISTICS (CON'T)

| Parameter                                 | Symbol            | 25°C |     |     | Tmin to Tmax |     | Units | Test Conditions/Comments              |
|-------------------------------------------|-------------------|------|-----|-----|--------------|-----|-------|---------------------------------------|
| Min                                       | Typ               | Max  | Min | Max |              |     |       |                                       |
| POWER SUPPLY <sup>5</sup>                 |                   |      |     |     |              |     |       |                                       |
| Functional Voltage Range <sup>2</sup>     | V <sub>DD</sub>   | 4.5  |     | 5.5 | 4.5          | 5.5 | V     | All digital inputs = 0 V or all = 5 V |
| Supply Current                            | I <sub>DD</sub>   |      |     | 50  |              | 50  | μA    |                                       |
| SWITCHING CHARACTERISTICS <sup>2, 4</sup> |                   |      |     |     |              |     |       |                                       |
| Data Write Time                           | t <sub>W</sub>    | 320  |     |     | 400          |     | ns    |                                       |
| Write Strobe Req.                         | t <sub>DSW</sub>  | 200  |     |     | 250          |     | ns    |                                       |
| Data Hold Time                            | t <sub>DHLD</sub> | 40   |     |     | 50           |     | ns    |                                       |
| Data Read Time                            | t <sub>R</sub>    | 480  |     |     | 600          |     | ns    |                                       |
| 3-state Hold Time                         | t <sub>TSHD</sub> | 240  |     |     | 300          |     | ns    |                                       |
| Read Strobe Req.                          | t <sub>DSR</sub>  | 320  |     |     | 400          |     | ns    |                                       |

### NOTES:

- <sup>1</sup> Full Scale Range (FSR) is 10V for unipolar mode.
- <sup>2</sup> Guaranteed but not production tested.
- <sup>3</sup> Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- <sup>4</sup> See timing diagrams.
- <sup>5</sup> Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25°C unless otherwise noted)<sup>1, 2</sup>

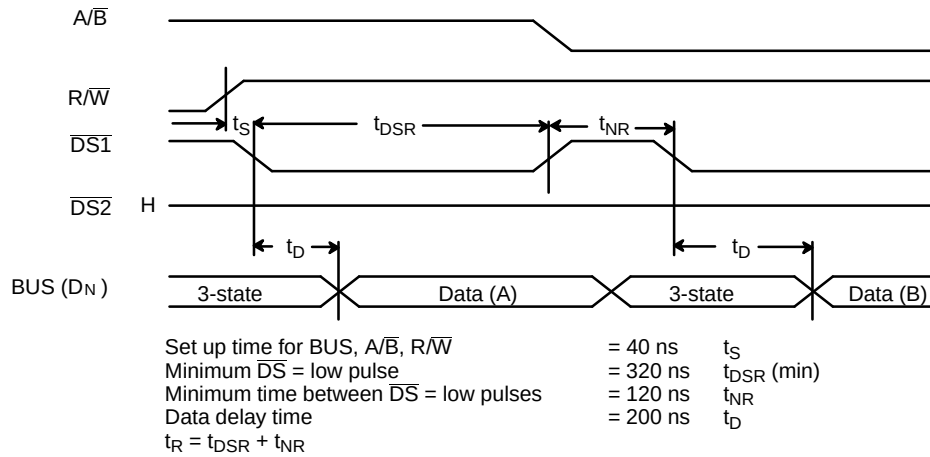
V<sub>DD</sub> to GND ..... +7 V  
 Digital Input Voltage to GND (2) . GND –0.5 to V<sub>DD</sub> +0.5 V  
 I<sub>OUT1</sub>, I<sub>OUT2</sub> to GND (2) ..... GND –0.5 to V<sub>DD</sub> +0.5 V  
 V<sub>REF</sub> to GND ..... ±25 V  
 V<sub>RFB</sub> to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C  
 Lead Temperature (Soldering, 10 seconds) ..... +300°C  
 Package Power Dissipation Rating to 75°C  
 CDIP, PDIP, SOIC, PLCC ..... 1050mW  
 Derates above 75°C ..... 14mW/°C

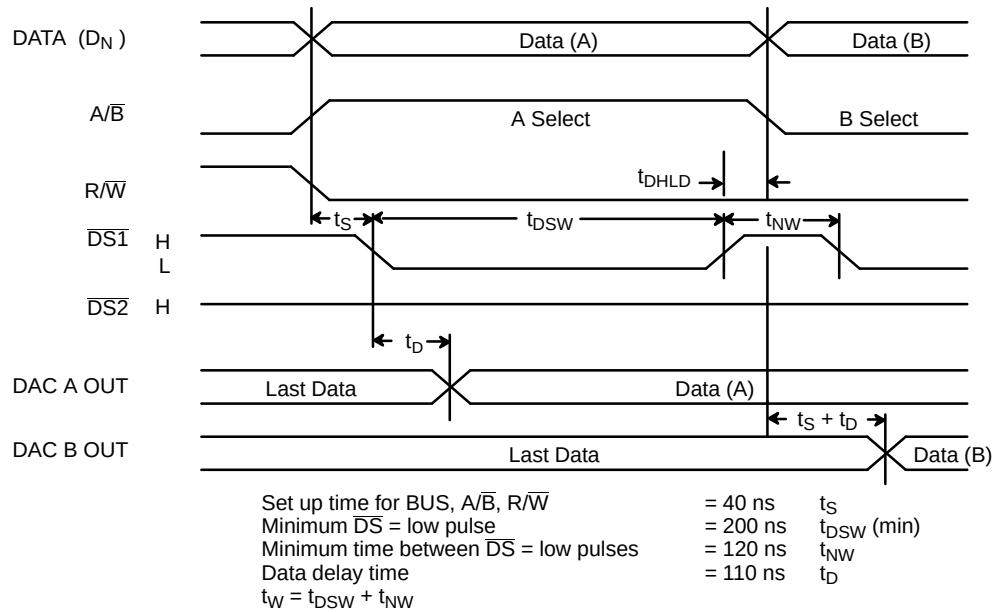
### NOTES:

- <sup>1</sup> Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- <sup>2</sup> Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

## TIMING DIAGRAM READ CYCLE



## TIMING DIAGRAM WRITE CYCLE



## MODE SELECTION TABLE

| DS1 | DS2 | A/B | R/W | MODE  | DAC     |
|-----|-----|-----|-----|-------|---------|
| L   | H   | H   | L   | WRITE | A       |
| L   | H   | L   | L   | WRITE | B       |
| H   | L   | H   | L   | WRITE | C       |
| H   | L   | L   | L   | WRITE | D       |
| L   | H   | H   | H   | READ  | A       |
| L   | H   | L   | H   | READ  | B       |
| H   | L   | H   | H   | READ  | C       |
| H   | L   | L   | H   | READ  | D       |
| L   | L   | H   | L   | WRITE | A & C   |
| L   | L   | L   | L   | WRITE | B & D   |
| H   | H   | X   | X   | HOLD  | A/B/C/D |
| L   | L   | H   | H   | HOLD  | A/B/C/D |
| L   | L   | L   | H   | HOLD  | A/B/C/D |

L = LOW STATE  
 H = HIGH STATE  
 X = DON'T CARE

## INTERFACE LOGIC INFORMATION

DAC Selection: All DAC latches share a common 8-bit input port. The control inputs  $\overline{DS1}$ ,  $\overline{DS2}$ ,  $A/\overline{B}$  select which DAC can accept data from the input port.

Mode Selection: Inputs  $\overline{DS}$  and  $R/\overline{W}$  control the operating mode of the selected DAC. See *Mode Selection Table on the previous page*.

Write Mode: When  $\overline{DS}$  and  $R/\overline{W}$  are both low the selected DAC is in the write mode. The input data latches of the selected

DAC are transparent and its analog output responds to activity on DB0-DB7.

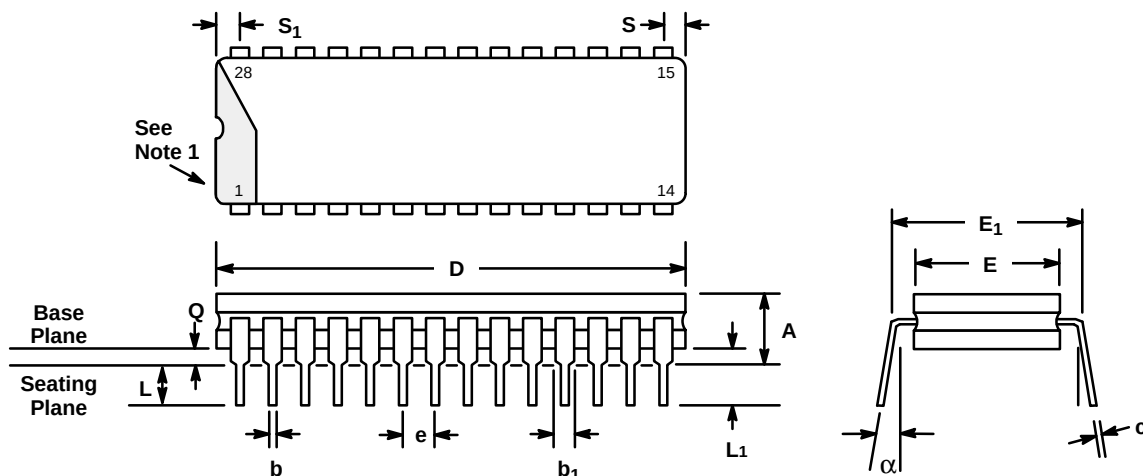
Hold Mode: The selected DAC latch retains the data which was present on DB0-DB7 just prior to  $\overline{DS}$  and  $R/\overline{W}$  assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When  $\overline{DS}$  is low and  $R/\overline{W}$  is high, the selected DAC is in the read mode and the data held in the appropriate latch is outputted to the data bus.

## APPLICATION NOTES

***Refer to Section 8 for Applications Information***

## 28 LEAD CERAMIC DUAL-IN-LINE (600 MIL CDIP) D28



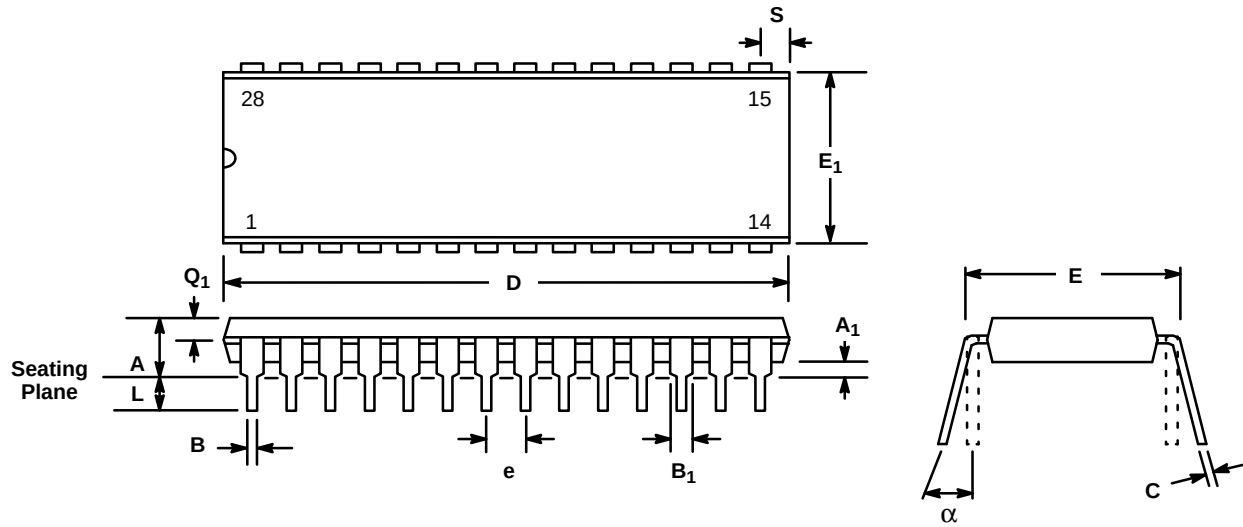
| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN       | MAX   | MIN         | MAX   |       |
| A              | —         | 0.232 | —           | 5.89  | —     |
| b              | 0.014     | 0.023 | 0.356       | 0.584 | —     |
| b <sub>1</sub> | 0.038     | 0.065 | 0.965       | 1.65  | 2     |
| c              | 0.008     | 0.015 | 0.203       | 0.381 | —     |
| D              | —         | 1.490 | —           | 37.85 | 4     |
| E              | 0.500     | 0.610 | 12.70       | 15.49 | 4     |
| E <sub>1</sub> | 0.590     | 0.620 | 14.99       | 15.75 | 7     |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 5     |
| L              | 0.125     | 0.200 | 3.18        | 5.08  | —     |
| L <sub>1</sub> | 0.150     | —     | 3.81        | —     | —     |
| Q              | 0.015     | 0.060 | 0.381       | 1.52  | 3     |
| S              | —         | 0.100 | —           | 2.54  | 6     |
| S <sub>1</sub> | 0.005     | —     | 0.13        | —     | 6     |
| α              | 0°        | 15°   | 0°          | 15°   | —     |

### NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b<sub>1</sub> may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.



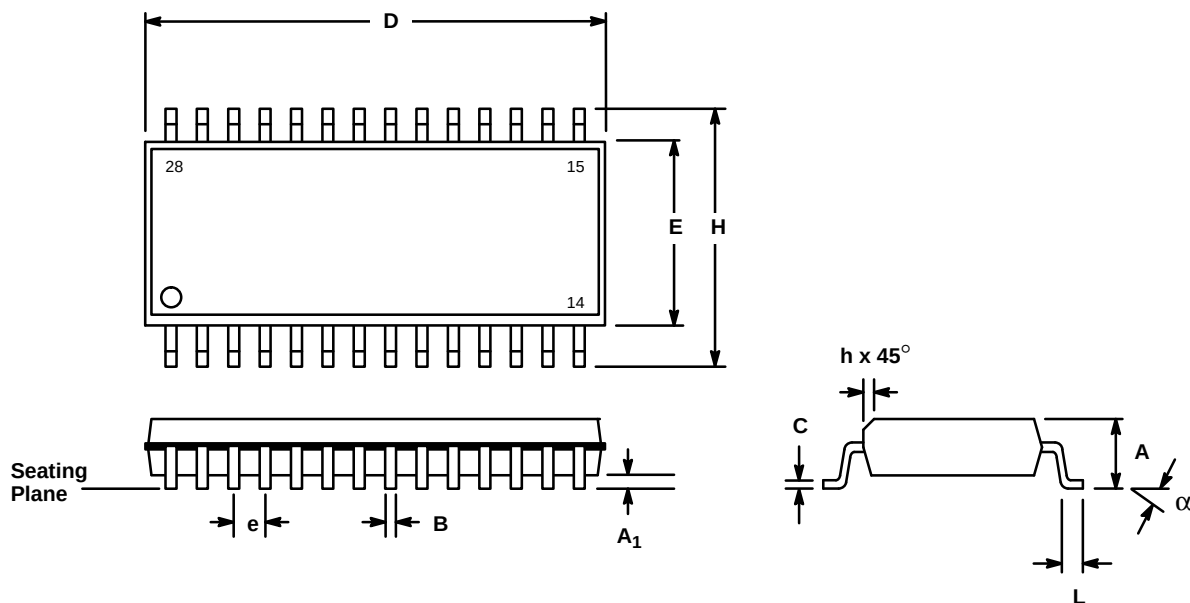
**28 LEAD PLASTIC DUAL-IN-LINE  
(600 MIL PDIP)  
N28**



| SYMBOL             | INCHES    |       | MILLIMETERS |       |
|--------------------|-----------|-------|-------------|-------|
|                    | MIN       | MAX   | MIN         | MAX   |
| A                  | —         | 0.232 | —           | 5.893 |
| A <sub>1</sub>     | 0.015     | —     | 0.381       | —     |
| B                  | 0.014     | 0.023 | 0.356       | 0.584 |
| B <sub>1</sub> (1) | 0.038     | 0.065 | 0.965       | 1.65  |
| C                  | 0.008     | 0.015 | 0.203       | 0.381 |
| D                  | 1.380     | 1.490 | 35.05       | 37.85 |
| E                  | 0.585     | 0.625 | 14.86       | 15.88 |
| E <sub>1</sub>     | 0.500     | 0.610 | 12.70       | 15.49 |
| e                  | 0.100 BSC |       | 2.54 BSC    |       |
| L                  | 0.115     | 0.150 | 2.92        | 3.81  |
| α                  | 0°        | 15°   | 0°          | 15°   |
| Q <sub>1</sub>     | 0.055     | 0.070 | 1.40        | 1.78  |
| S                  | 0.020     | 0.100 | 1.508       | 2.54  |

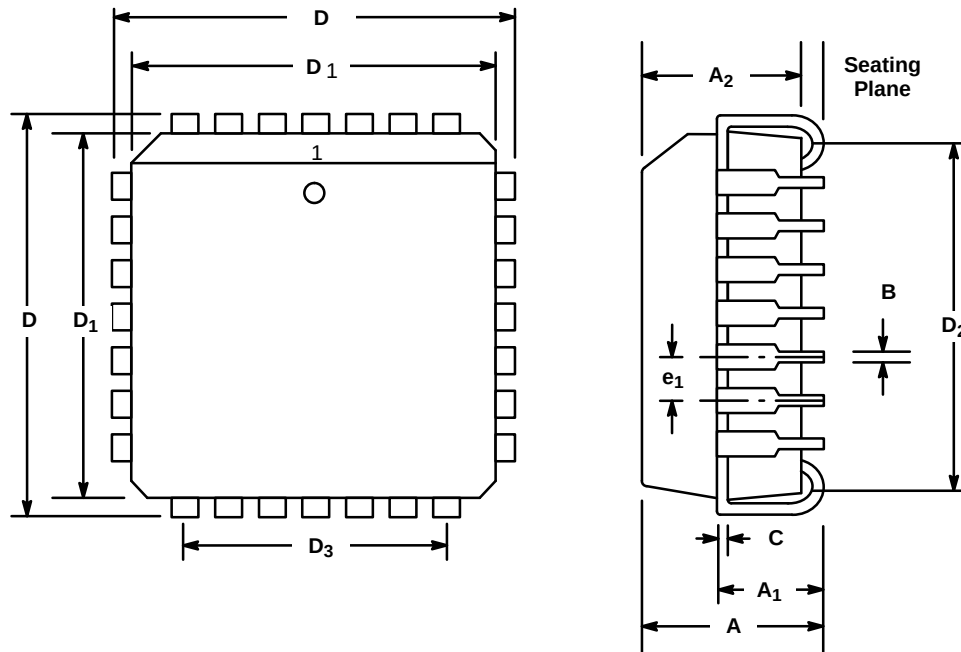
Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

## 28 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC) S28



| SYMBOL | INCHES    |        | MILLIMETERS |       |
|--------|-----------|--------|-------------|-------|
|        | MIN       | MAX    | MIN         | MAX   |
| A      | 0.097     | 0.104  | 2.464       | 2.642 |
| A1     | 0.0050    | 0.0115 | 0.127       | 0.292 |
| B      | 0.014     | 0.019  | 0.356       | 0.483 |
| C      | 0.0091    | 0.0125 | 0.231       | 0.318 |
| D      | 0.701     | 0.711  | 17.81       | 18.06 |
| E      | 0.292     | 0.299  | 7.42        | 7.59  |
| e      | 0.050 BSC |        | 1.27 BSC    |       |
| H      | 0.400     | 0.410  | 10.16       | 10.41 |
| h      | 0.010     | 0.016  | 0.254       | 0.406 |
| L      | 0.016     | 0.035  | 0.406       | 0.889 |
| α      | 0°        | 8°     | 0°          | 8°    |

**28 LEAD PLASTIC LEADED CHIP CARRIER  
(PLCC)  
P28**



| SYMBOL             | INCHES    |       | MILLIMETERS |       |
|--------------------|-----------|-------|-------------|-------|
|                    | MIN       | MAX   | MIN         | MAX   |
| A                  | 0.165     | 0.180 | 4.19        | 4.57  |
| A <sub>1</sub>     | 0.100     | 0.110 | 2.54        | 2.79  |
| A <sub>2</sub>     | 0.148     | 0.156 | 3.76        | 3.96  |
| B                  | 0.013     | 0.021 | 0.330       | 0.533 |
| C                  | 0.008     | 0.012 | 0.203       | 0.305 |
| D                  | 0.485     | 0.495 | 12.32       | 12.57 |
| D <sub>1</sub> (1) | 0.450     | 0.454 | 11.43       | 11.53 |
| D <sub>2</sub>     | 0.390     | 0.430 | 9.91        | 10.92 |
| D <sub>3</sub>     | 0.300 Ref |       | 7.62 Ref.   |       |
| e <sub>1</sub>     | 0.050 BSC |       | 1.27 BSC    |       |

Note: (1) Dimension D<sub>1</sub> does not include mold protrusion.  
Allowed mold protrusion is 0.254 mm/0.010 in.

## NOTICE

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