Dual and Quad 250μA, 3MHz, 200V/μs Operational Amplifiers

FEATURES

- **3MHz Gain Bandwidth**
- **200V/μs Slew Rate**
- **250μA Supply Current per Amplifier**
- C-Load™ Op Amp Drives All Capacitive Loads
- Unity-Gain Stable
- Maximum Input Offset Voltage: 600μV
- Maximum Input Bias Current: 50nA
- Maximum Input Offset Current: 15nA
- Minimum DC Gain, R_L = 2k: 30V/mV
- Input Noise Voltage: $14nV/\sqrt{Hz}$
- Settling Time to 0.1%, 10V Step: 700ns
- Settling Time to 0.01%, 10V Step: 1.25μs
- Minimum Output Swing into 1k: ±13V
- Minimum Output Swing into 500Ω: ±3.4V
- Specified at ±2.5V, ±5V and ±15V

APPLICATIONS

- Battery-Powered Systems
- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

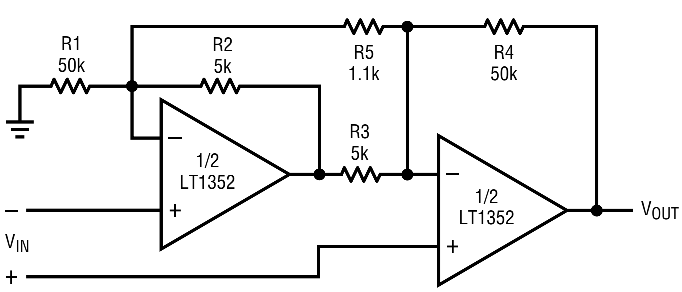
DESCRIPTION

The LT®1352/LT1353 are dual and quad, very low power, high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit combines the slewing performance of a current feedback amplifier in a true operational amplifier with matched high impedance inputs. The high slew rate ensures that the large-signal bandwidth is not degraded. Each output is capable of driving a 1kΩ load to ±13V with ±15V supplies and a 500Ω load to ±3.4V on ±5V supplies.

The LT1352/LT1353 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced complementary bipolar processing. For higher bandwidth devices with higher supply current see the LT1354 through LT1365 data sheets. Bandwidths of 12MHz, 25MHz, 50MHz and 70MHz are available with 1mA, 2mA, 4mA and 6mA of supply current per amplifier. Singles, duals and quads of each amplifier are available.

TYPICAL APPLICATION

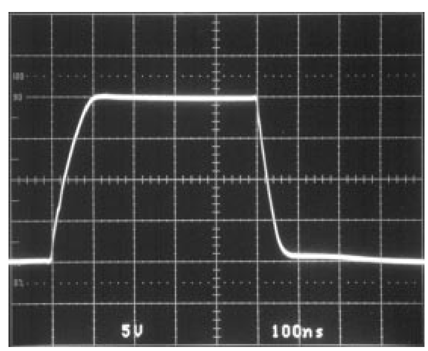
Instrumentation Amplifier



GAIN = [R4/R3][1 + (1/2)(R2/R1 + R3/R4) + (R2 + R3)/R5] = 102
TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 30kHz

1352/53 TA01

Large-Signal Response



$A_V = -1$

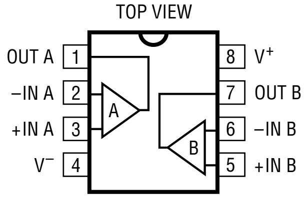
1352/53 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage .... ±10V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range .... –40°C to 85°C
Specified Temperature Range .... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

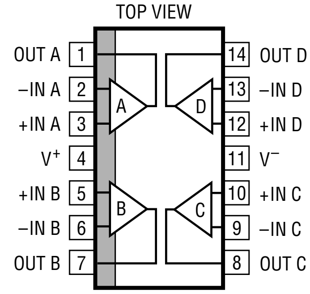


N8 PACKAGE
8-LEAD PDIP
S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER
LT1352CN8 LT1352CS8
S8 PART MARKING
1352

TOP VIEW



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1353CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V		0.2 0.2 0.3	0.6 0.6 0.8	mV mV mV
I_{OS}	Input Offset Current		±2.5V to ±15V		5	15	nA
I_B	Input Bias Current		±2.5V to ±15V		20	50	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		14		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.5		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V Differential	±15V ±15V	300	600 20		MΩ MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Positive Input Voltage Range		±15V ±5V ±2.5V	12.0 2.5 0.5	13.5 3.5 1.0		V V V
	Negative Input Voltage Range		±15V ±5V ±2.5V		–13.5 –3.5 –1.0	–12.0 –2.5 –0.5	V V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V V_{CM} = ±2.5V V_{CM} = ±0.5V	±15V ±5V ±2.5V	80 78 68	94 86 77		dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		90	106		dB

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 5k$	±15V	40	80		V/mV
		$V_{OUT} = \pm10V$, $R_L = 2k$	±15V	30	60		V/mV
		$V_{OUT} = \pm10V$, $R_L = 1k$	±15V	20	40		V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 5k$	±5V	30	60		V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 2k$	±5V	25	50		V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	15	30		V/mV
		$V_{OUT} = \pm1V$, $R_L = 5k$	±2.5V	20	40		V/mV
V_{OUT}	Output Swing	$R_L = 5k$, $V_{IN} = \pm10mV$	±15V	13.5	14.0		±V
		$R_L = 2k$, $V_{IN} = \pm10mV$	±15V	13.4	13.8		±V
		$R_L = 1k$, $V_{IN} = \pm10mV$	±15V	13.0	13.4		±V
		$R_L = 1k$, $V_{IN} = \pm10mV$	±5V	3.5	4.0		±V
		$R_L = 500\Omega$, $V_{IN} = \pm10mV$	±5V	3.4	3.8		±V
		$R_L = 5k$, $V_{IN} = \pm10mV$	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	$V_{OUT} = \pm13V$	±15V	13.0	13.4		mA
		$V_{OUT} = \pm3.4V$	±5V	6.8	7.6		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	30	45		mA
SR	Slew Rate	$A_V = -1$, $R_L = 5k$ (Note 2)	±15V	120	200		V/µs
			±5V	30	50		V/µs
	Full-Power Bandwidth	10V Peak (Note 3)	±15V		3.2		MHz
		3V Peak (Note 3)	±5V		2.6		MHz
GBW	Gain Bandwidth	f = 200kHz, $R_L = 10k$	±15V	2.0	3.0		MHz
			±5V	1.8	2.7		MHz
			±2.5V		2.5		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V	±15V		46		ns
			±5V		53		ns
	Overshoot	$A_V = 1$, 0.1V	±15V		13		%
			±5V		16		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		41		ns
			±5V		52		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	±15V		700		ns
		10V Step, 0.01%, $A_V = -1$	±15V		1250		ns
		5V Step, 0.1%, $A_V = -1$	±5V		950		ns
		5V Step, 0.01%, $A_V = -1$	±5V		1400		ns
R_O	Output Resistance	$A_V = 1$, f = 20kHz	±15V		1.5		Ω
	Channel Separation	$V_{OUT} = \pm10V$, $R_L = 2k$	±15V	101	120		dB
I_S	Supply Current	Each Amplifier	±15V		250	320	µA
		Each Amplifier	±5V		230	300	µA

$0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V			0.8	mV
			±5V			0.8	mV
			±2.5V			1.0	mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V		3	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V			20	nA
I_B	Input Bias Current		±2.5V to ±15V			75	nA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$ $V_{CM} = \pm2.5V$ $V_{CM} = \pm0.5V$	±15V ±5V ±2.5V	78 77 67			dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to $\pm15V$		89			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 5k$ $V_{OUT} = \pm10V$, $R_L = 2k$ $V_{OUT} = \pm2.5V$, $R_L = 5k$ $V_{OUT} = \pm2.5V$, $R_L = 2k$ $V_{OUT} = \pm2.5V$, $R_L = 1k$ $V_{OUT} = \pm1V$, $R_L = 5k$	±15V ±15V ±5V ±5V ±5V ±2.5V	25 20 20 15 10 15			V/mV V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	$R_L = 5k$, $V_{IN} = \pm10mV$ $R_L = 2k$, $V_{IN} = \pm10mV$ $R_L = 1k$, $V_{IN} = \pm10mV$ $R_L = 1k$, $V_{IN} = \pm10mV$ $R_L = 500\Omega$, $V_{IN} = \pm10mV$ $R_L = 5k$, $V_{IN} = \pm10mV$	±15V ±15V ±15V ±5V ±5V ±2.5V	13.4 13.3 12.0 3.4 3.3 1.2			±V ±V ±V ±V ±V ±V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$ $V_{OUT} = \pm3.3V$	±15V ±5V	12.0 6.6			mA mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	24			mA
SR	Slew Rate	$A_V = -1$, $R_L = 5k$ (Note 2)	±15V ±5V	100 21			V/µs V/µs
GBW	Gain Bandwidth	f = 200kHz, $R_L = 10k$	±15V ± 5V	1.8 1.6			MHz MHz
	Channel Separation	$V_{OUT} = \pm10V$, $R_L = 2k$	±15V	100			dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V			350 330	µA µA

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted (Note 5).

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V			1.0 1.0 1.2	mV mV mV
	Input V_{OS} Drift	(Note 4)	±2.5V to ±15V		3	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V			30	nA
I_B	Input Bias Current		±2.5V to ±15V			100	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$ $V_{CM} = \pm2.5V$ $V_{CM} = \pm0.5V$	±15V ±5V ±2.5V	76 76 66			dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to $\pm15V$		87			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 5k$ $V_{OUT} = \pm10V$, $R_L = 2k$ $V_{OUT} = \pm2.5V$, $R_L = 5k$ $V_{OUT} = \pm2.5V$, $R_L = 2k$ $V_{OUT} = \pm2.5V$, $R_L = 1k$ $V_{OUT} = \pm1V$, $R_L = 5k$	±15V ±15V ±5V ±5V ±5V ±2.5V	20 15 15 10 8 10			V/mV V/mV V/mV V/mV V/mV V/mV

ELECTRICAL CHARACTERISTICS
$-40°C \le T_A \le 85°C$, V_{CM} = 0V unless otherwise noted (Note 4).

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	R_L = 5k, V_{IN} = ±10mV	±15V	13.3			±V
		R_L = 2k, V_{IN} = ±10mV	±15V	13.2			±V
		R_L = 1k, V_{IN} = ±10mV	±15V	10.0			±V
		R_L = 1k, V_{IN} = ±10mV	±5V	3.3			±V
		R_L= 500Ω, V_{IN} = ±10mV	±5V	3.2			±V
		R_L = 5k, V_{IN} = ±10mV	±2.5V	1.1			±V
I_{OUT}	Output Current	V_{OUT} = ±10V	±15V	10.0			mA
		V_{OUT} = ±3.2V	±5V	6.4			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	20			mA
SR	Slew Rate	A_V = −1, R_L = 5k (Note 2)	±15V	50			V/µs
			±5V	15			V/µs
GBW	Gain Bandwidth	f = 200kHz, R_L = 10k	±15V	1.6			MHz
			± 5V	1.4			MHz
	Channel Separation	V_{OUT} = ±10V, R_L = 2k	±15V	99			dB
I_S	Supply Current	Each Amplifier	±15V			380	µA
		Each Amplifier	±5V			350	µA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Slew rate is measured between ±8V on the output with ±12V input for ±15V supplies and ±2V on the output with ±3V input for ±5V supplies.

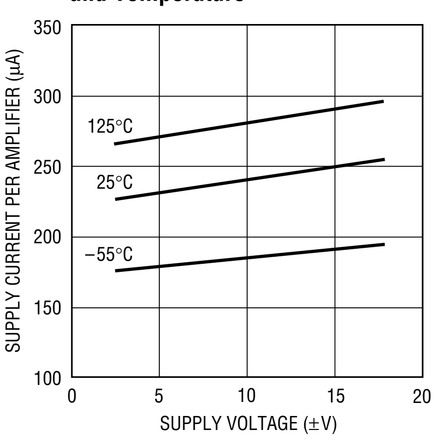
Note 3: Full-power bandwidth is calculated from the slew rate measurement: FPBW = (Slew Rate)/2πV_P.

Note 4: This parameter is not 100% tested.

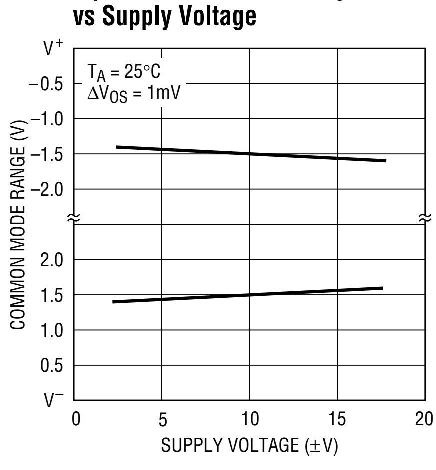
Note 5: The LT1352/LT1353 are designed, characterized and expected to meet these extended temperature limits, but are not tested at −40°C and 85°C. Guaranteed I grade parts are available, consult factory.

TYPICAL PERFORMANCE CHARACTERISTICS

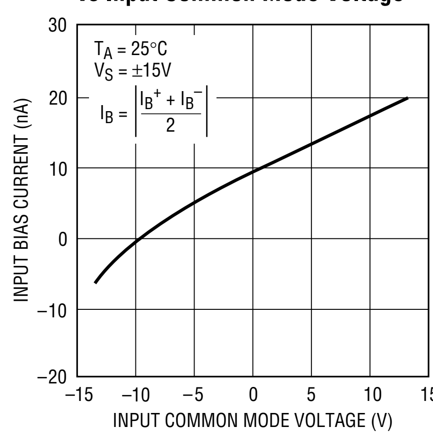
Supply Current vs Supply Voltage and Temperature



Input Common Mode Range vs Supply Voltage

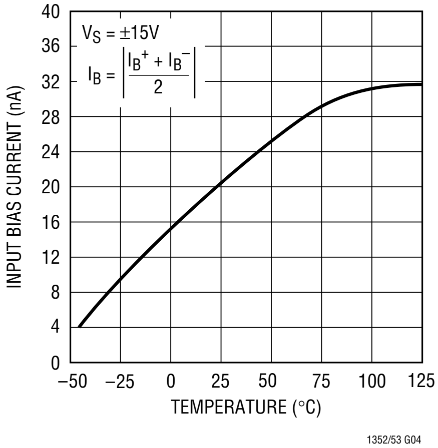


Input Bias Current vs Input Common Mode Voltage

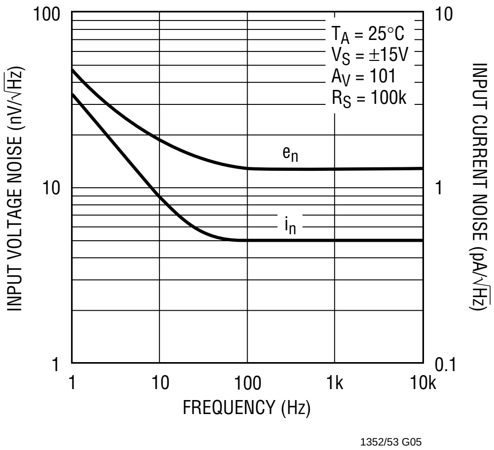


TYPICAL PERFORMANCE CHARACTERISTICS

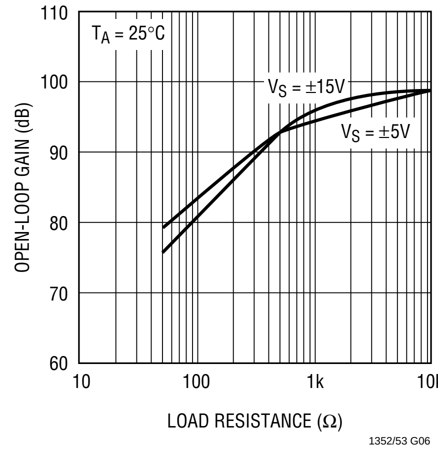
Input Bias Current vs Temperature



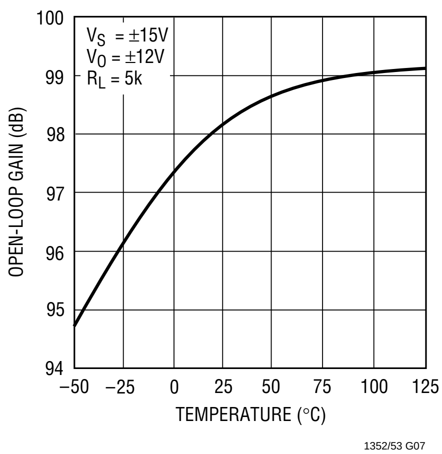
Input Noise Spectral Density



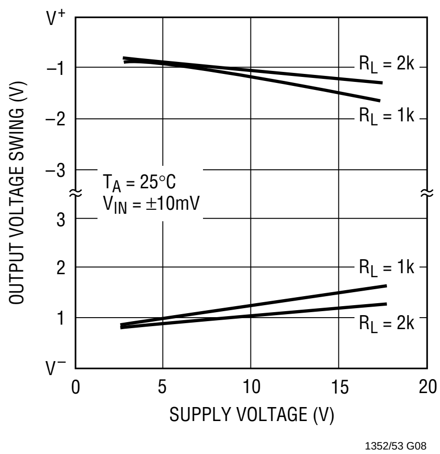
Open-Loop Gain vs Resistive Load



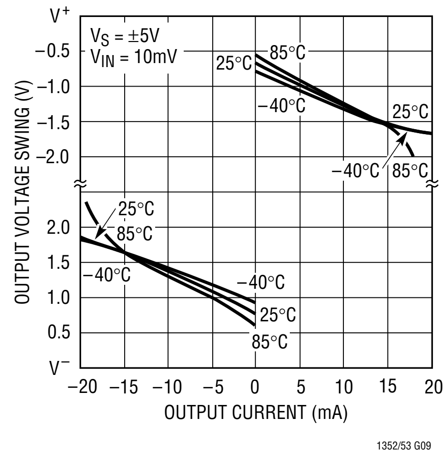
Open-Loop Gain vs Temperature



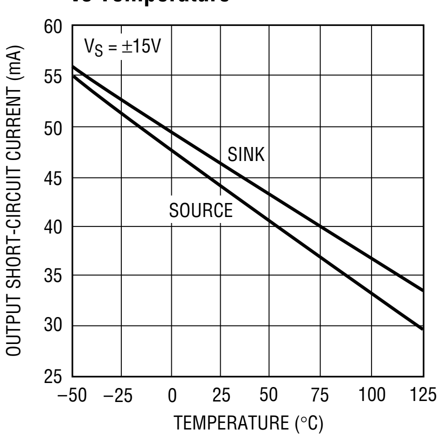
Output Voltage Swing vs Supply Voltage



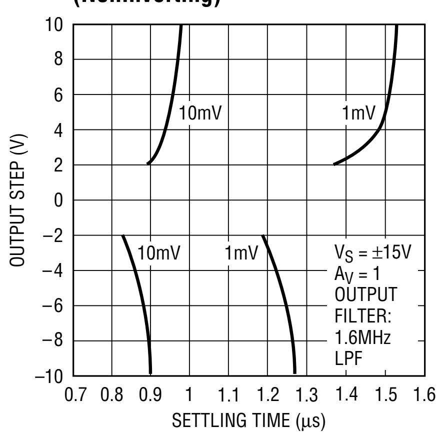
Output Voltage Swing vs Load Current



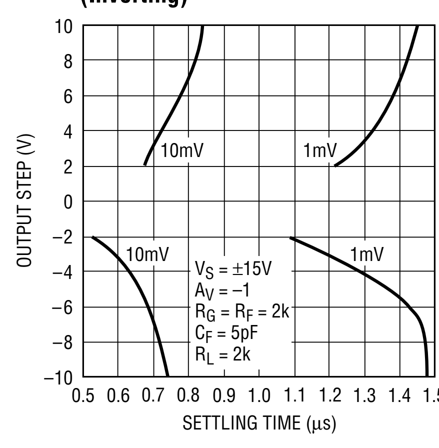
Output Short-Circuit Current vs Temperature



Settling Time vs Output Step (Noninverting)

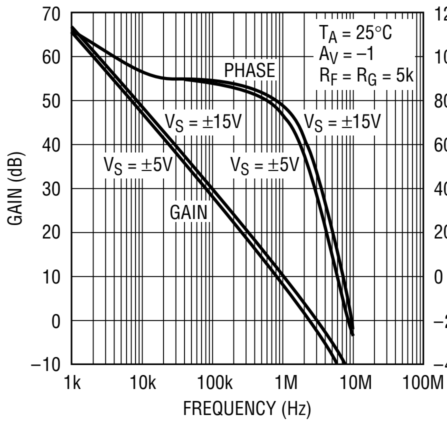


Settling Time vs Output Step (Inverting)



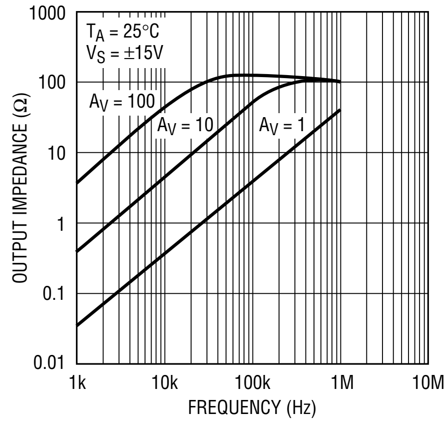
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase vs Frequency



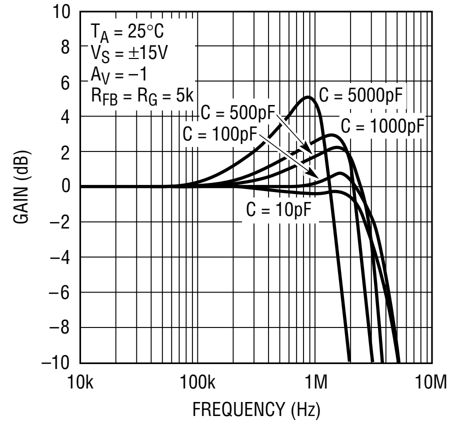
1352/53 G13

Output Impedance vs Frequency



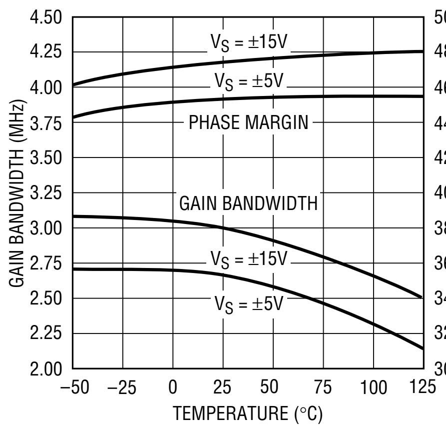
1352/53 G14

Frequency Response vs Capacitive Load



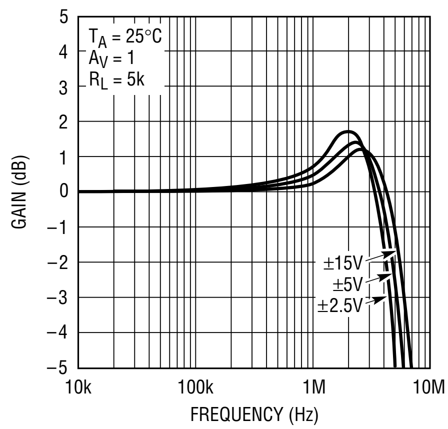
1352/53 G15

Gain Bandwidth and Phase Margin vs Temperature



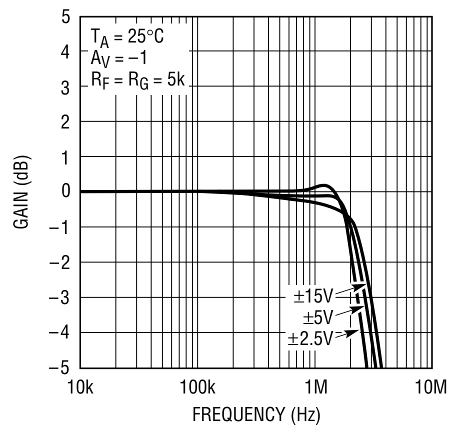
1352/53 G16

Frequency Response vs Supply Voltage ($A_V = 1$)



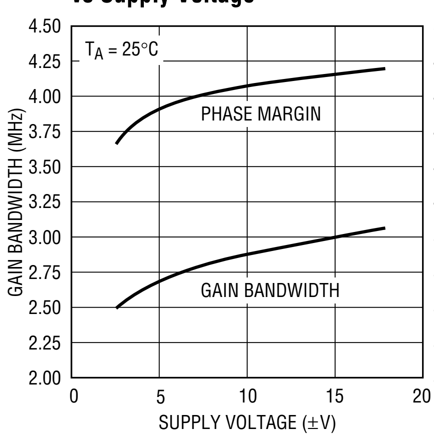
1352/53 G17

Frequency Response vs Supply Voltage ($A_V = -1$)



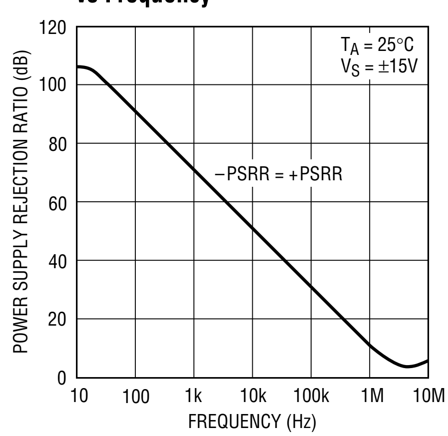
1352/53 G18

Gain Bandwidth and Phase Margin vs Supply Voltage



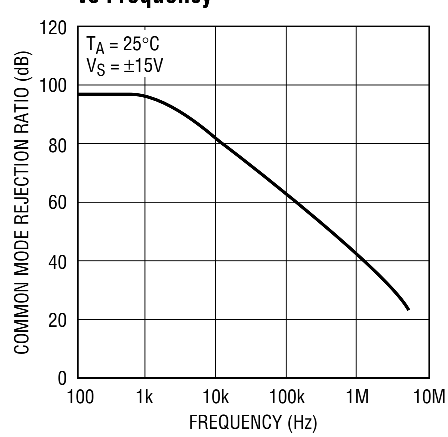
1352/53 G19

Power Supply Rejection Ratio vs Frequency



1352/53 G20

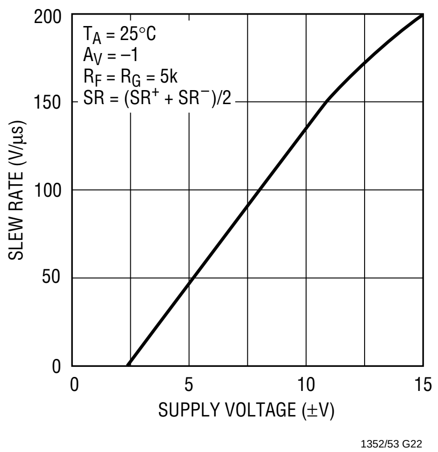
Common Mode Rejection Ratio vs Frequency



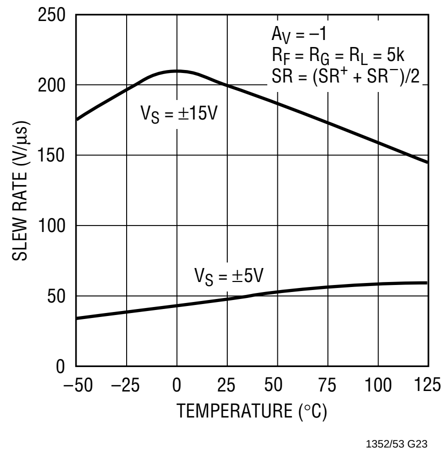
1352/53 G21

TYPICAL PERFORMANCE CHARACTERISTICS

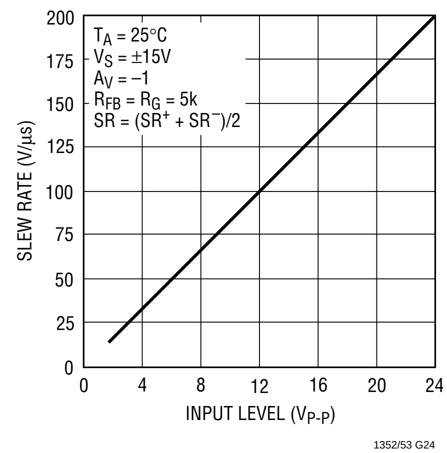
Slew Rate vs Supply Voltage



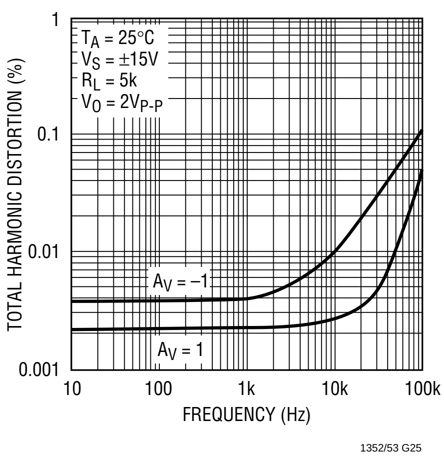
Slew Rate vs Temperature



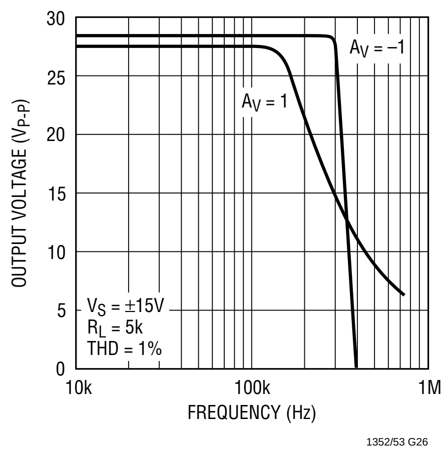
Slew Rate vs Input Level



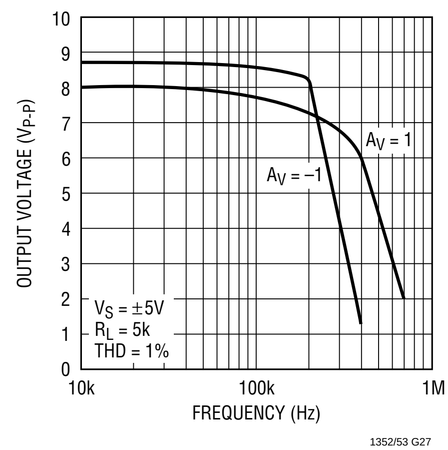
Total Harmonic Distortion vs Frequency



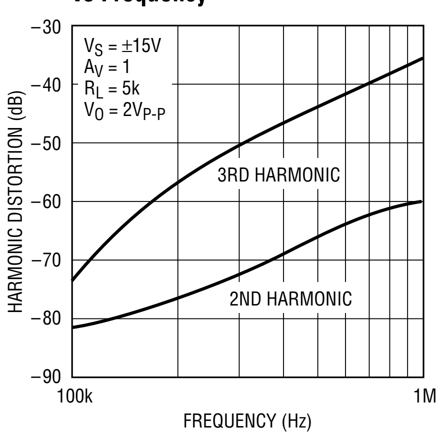
Undistorted Output Swing vs Frequency (±15V)



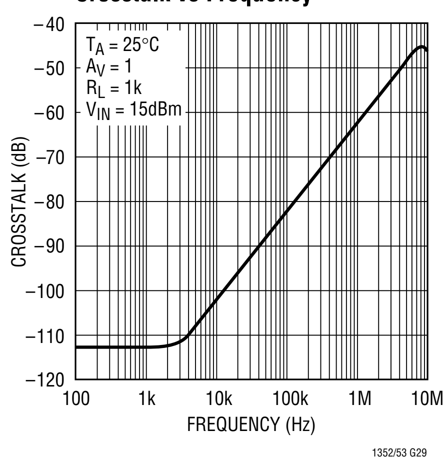
Undistorted Output Swing vs Frequency (±5V)



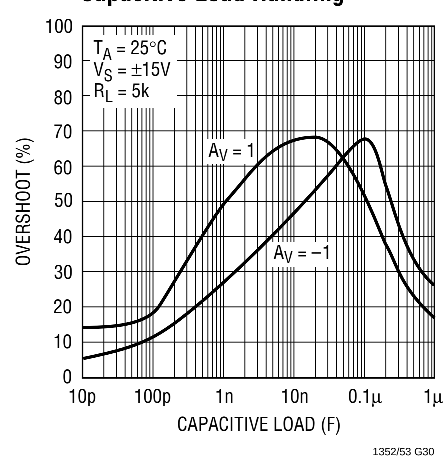
2nd and 3rd Harmonic Distortion vs Frequency



Crosstalk vs Frequency

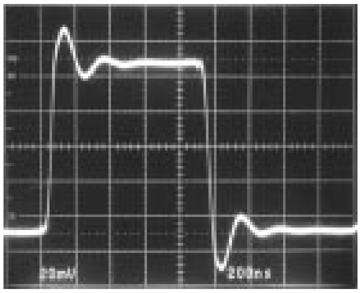


Capacitive Load Handling



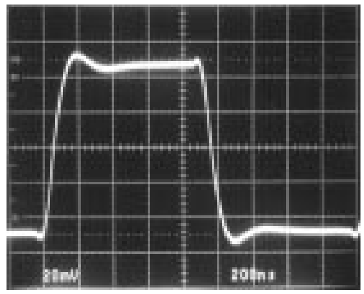
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient (A_V = 1)



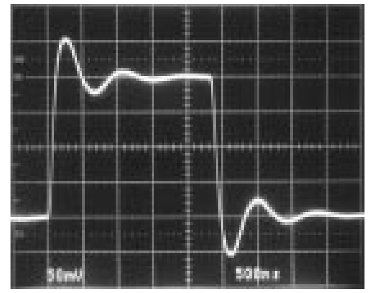
1352/53 G31

Small-Signal Transient (A_V = –1)



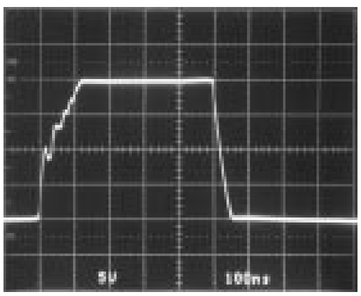
1352/53 G32

Small-Signal Transient (A_V = –1, C_L = 1000pF)



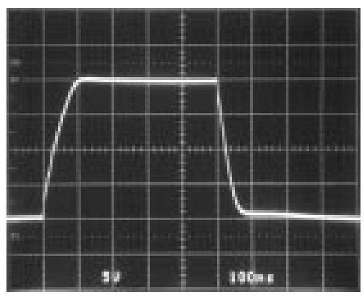
1352/53 G33

Large-Signal Transient (A_V = 1)



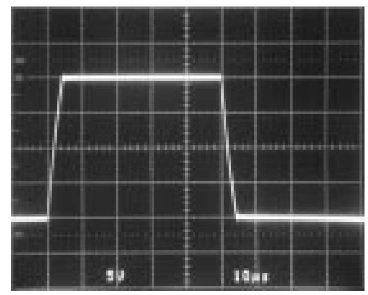
1352/53 G34

Large-Signal Transient (A_V = –1)



1352/53 G35

Large-Signal Transient (A_V = 1, C_L = 10,000pF)



1352/53 G36

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1352/LT1353 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. If feedback resistors greater than 10k are used, a parallel capacitor of value, $C_F > (R_G)(C_{IN}/R_F)$, should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be an I-to-V converter as shown in the Typical Applications section.

Capacitive Loading

The LT1352/LT1353 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Graphs of Frequency Response vs Capacitive Load, Capacitive Load Handling and the transient response photos clearly show these effects.

Input Considerations

Each of the LT1352/LT1353 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input current can be positive or negative. The offset current does not depend on NPN to PNP beta matching and is well controlled. The use of balanced source resistance at each input is recom-

APPLICATIONS INFORMATION

mended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection. Differential inputs generate large supply currents (up to 40mA) as required for high slew rates. Typically power dissipation does not significantly increase because of the low duty cycle of the transient inputs. If the device is used as a comparator with sustained differential inputs, excessive power dissipation may result.

Circuit Operation

The LT1352/LT1353 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic.

The inputs are buffered by complementary NPN and PNP emitter followers which drive R1, a 1k resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node and compensation capacitor C_T. Complementary followers form an output stage which buffers the gain node from the load. The output devices Q19 and Q22 are connected to form a composite PNP and a composite NPN.

The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the high impedance node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step whereas the same output step in unity gain has a 10 times greater input step. The graph Slew Rate vs Input Level illustrates this relationship. In higher gain configurations the large-signal performance and the small-signal performance both look like a single pole response.

Capacitive load compensation is provided by the R_C, C_C network which is bootstrapped across the output stage. When the amplifier is driving a light load the network has no effect. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier and a zero is created by the RC combination, both of which improve the phase margin. The design ensures that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1352/LT1353 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature of 150°C under certain conditions. Maximum junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LT1352CN8: $T_J = T_A + (P_D)(130°C/W)$
LT1352CS8: $T_J = T_A + (P_D)(190°C/W)$
LT1353CS: $T_J = T_A + (P_D)(150°C/W)$

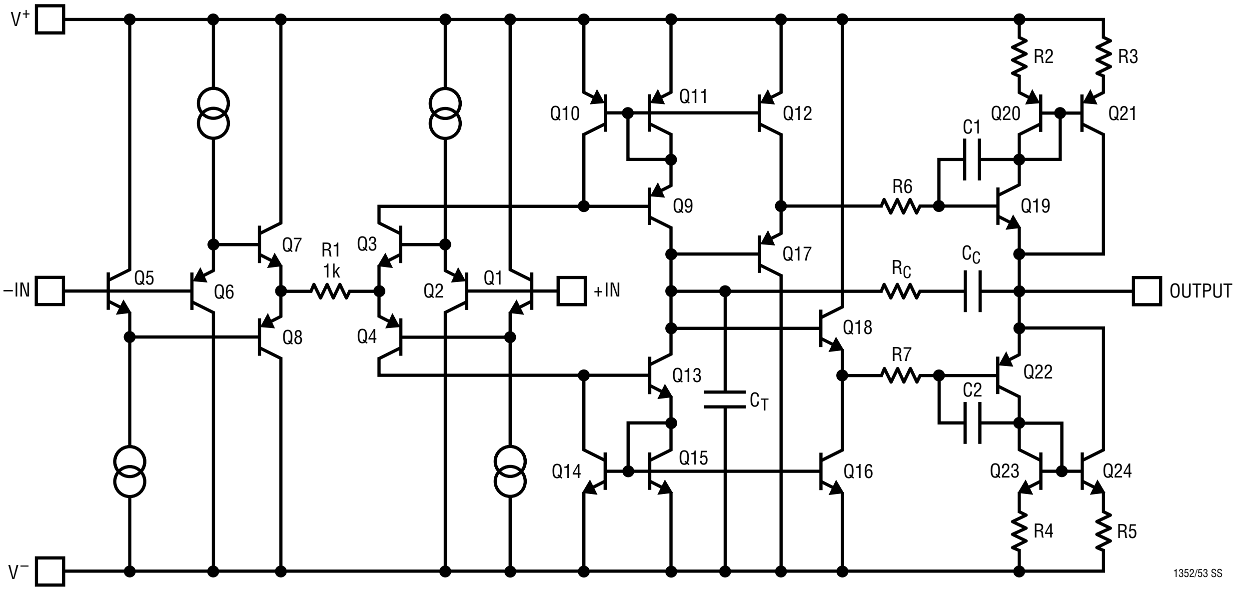
Worst-case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier $P_{D(MAX)}$ is:

$$P_{D(MAX)} = (V^+ - V^-)(I_{S(MAX)}) + (V^+/2)^2/R_L \text{ or}$$
$$(V^+ - V^-)(I_{S(MAX)}) + (V^+ - V_{MAX})(I_{MAX})$$

Example: LT1353 in S14 at 85°C, $V_S = \pm15V$, $R_L = 500\Omega$, $V_{OUT} = \pm5V$ ($\pm10mA$)

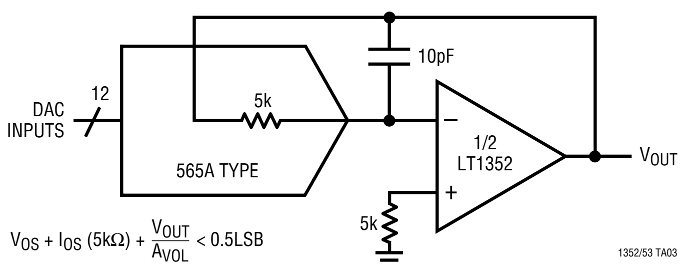
$$P_{D(MAX)} = (30V)(380\mu A) + (15V - 5V)(10mA) = 111mW$$
$$T_J = 85°C + (4)(111mW)(150°C/W) = 152°C$$

SIMPLIFIED SCHEMATIC

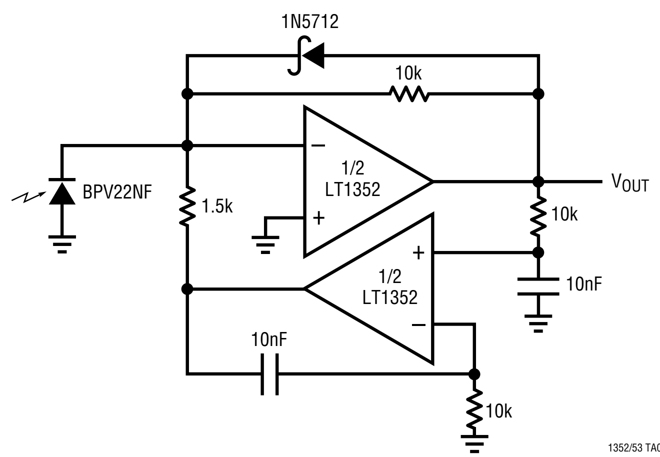


TYPICAL APPLICATIONS

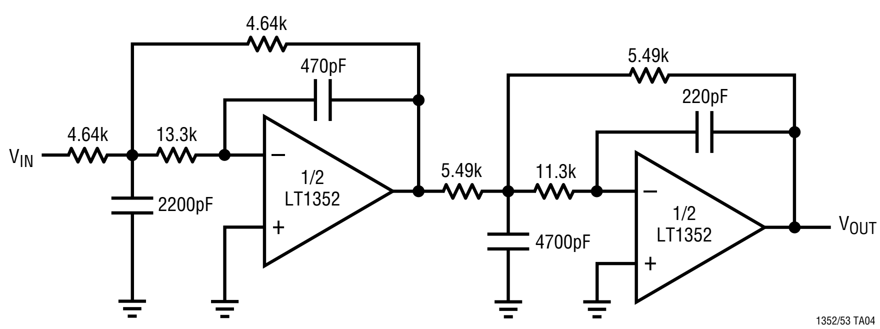
DAC I-to-V Converter



400kHz Photodiode Preamp with 10kHz Highpass Loop

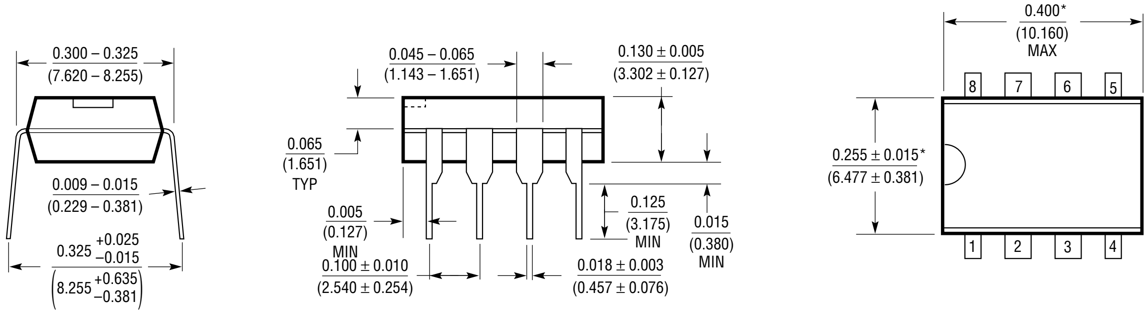


20kHz, 4th Order Butterworth Filter



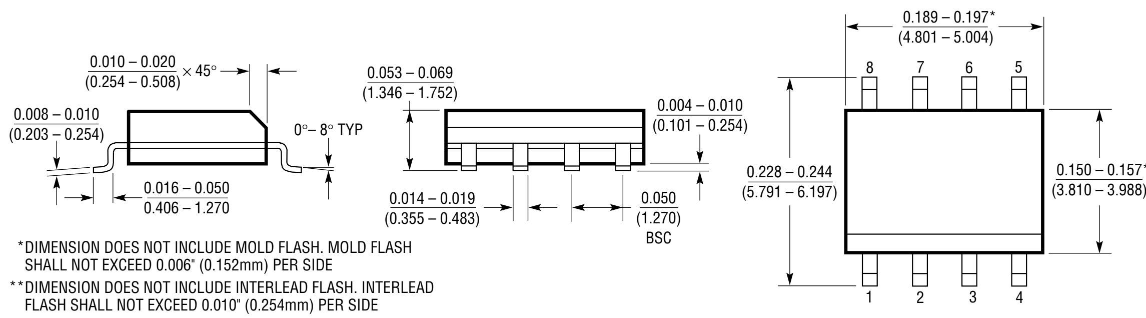
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



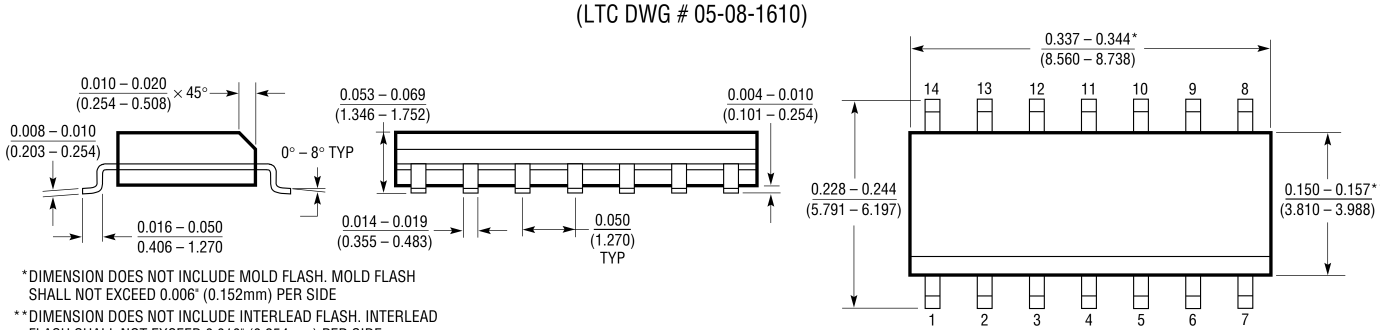
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1351	250µA, 3MHz, 200V/µs Op Amp	Good DC Precision, C-Load Stable, Power Saving Shutdown
LT1354/55/56	Single/Dual/Quad 1mA, 12MHz, 400V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads

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