

**LC8953**

General-Purpose 68000 MPU Peripheral Interface IC

PUPPET (Programmable Universal Peripheral/Port Expansion unit)

Overview

There are many application systems using the 68000 chip as their MPU (Main Processing Unit). It is common to them that designing the peripheral circuits such as address decoders, interrupt controllers, serial interface and DMA (Direct Memory Access) has become a time-consuming task. As a result, each of the application systems requires a larger board size, which makes it very expensive.

In addition, 68000 family peripherals are highly advanced functional ICs. The application system designer finds it difficult to use them in small- and medium-sized application products in terms of cost as well as functional complexity. The LC8953 (Programmable Universal Peripheral/Port Expansion unit) has optimized on-chip control circuits enabling the 68000 MPU to control the LC8951 (RCHIP) and LC8955. Use of the optimized control circuits allows the user to easily build up CD-ROM and CD-I systems which offer excellent performance in terms of space and cost.

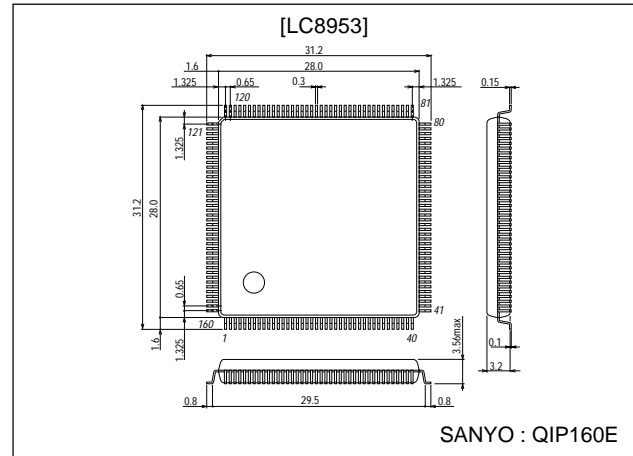
Features

- Programmable address decoder.
- Programmable \overline{DTACK} generator.
- Programmable interrupt handler.
- Clock divider.
- Bus error generator.
- TICK generator (programmable timer interrupt generator)
- Serial mouse interface (1 port)
- LC8951 (RCHIP-Real-time error Correction & Host-interface Integrated Processor) interface.
- LC8955 interface.
- Micro-programmable 1-channel DMA controller.

Package Dimensions

unit:mm

3153A-QIP160E



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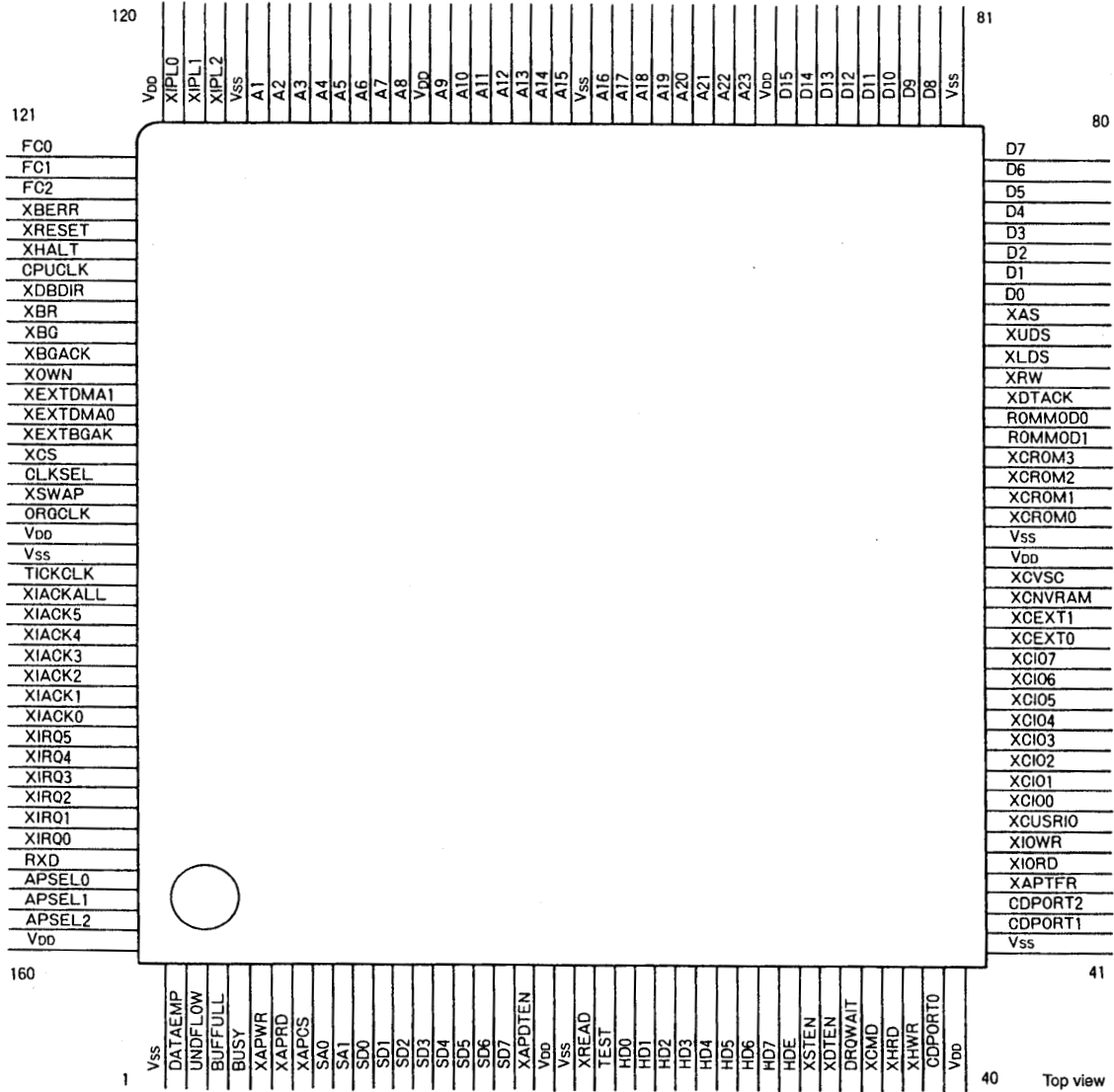
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Pin Assignment



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Pin Functions

| Number | Name ¹ | I/O | Function |
|--------|-------------------|-----|--|
| 1 | V _{SS} | – | Ground pin |
| 2 | DATAEMP | I | Data empty signal input pin for the LC8955 |
| 3 | UNDFLOW | I | Underflow signal input pin for the LC8955 |
| 4 | BUFFULL | I | Buffer full signal input pin for the LC8955 |
| 5 | BUSY | I | Busy signal input pin for the LC8955 |
| 6 | XAPWR | I | Data write signal input pin for the LC8955 |
| 7 | XAPRD | I | Data read signal input pin for the LC8955 |
| 8 | XAPCS | I | Chip select input pin for the LC8955 |
| 9 | SA0 | O | Resister select signal output pins for the LC8955 |
| 10 | SA1 | O | |
| 11 | SD0 | I/O | Data signal I/O pins for the LC8955 |
| 12 | SD1 | I/O | |
| 13 | SD2 | I/O | |
| 14 | SD3 | I/O | |
| 15 | SD4 | I/O | |
| 16 | SD5 | I/O | |
| 17 | SD6 | I/O | |
| 18 | SD7 | I/O | |
| 19 | XAPDTEN | O | Data enable signal output pin for the LC8955 for automatic request transfer |
| 20 | V _{DD} | – | +5V supply pin |
| 21 | V _{SS} | – | Ground pin |
| 22 | XREAD | I | Read signal input pin for the LC8955 for automatic request transfer |
| 23 | TEST | I | Test input pin (Tied low) |
| 24 | HD0 | I/O | Data signal I/O pins for the LC8951 (RCHIP) |
| 25 | HD1 | I/O | |
| 26 | HD2 | I/O | |
| 27 | HD3 | I/O | |
| 28 | HD4 | I/O | |
| 29 | HD5 | I/O | |
| 30 | HD6 | I/O | |
| 31 | HD7 | I/O | |
| 32 | HDE | I | Erasure flag signal input pin for the LC8951 (RCHIP) |
| 33 | XSTEN | I | Status enable signal input pin for the LC8951 (RCHIP) |
| 34 | XDTEN | I | Data enable signal input pin for the LC8951 (RCHIP) |
| 35 | DRQWAIT | I | Data request/Wait select signal input pin for the LC8951 (RCHIP) |
| 36 | XCMD | O | Command/Data select signal output pin for the LC8951 (RCHIP) |
| 37 | XHRD | O | Data read signal output pin for the LC8951 (RCHIP) |
| 38 | XHWR | O | Data write signal output pin for the LC8951 (RCHIP) |
| 39 | CDPORT0 | I/O | General-purpose input/output signal pin |
| 40 | V _{DD} | – | +5V supply pin |
| 41 | V _{SS} | – | Ground pin |
| 42 | CDPORT1 | I/O | General-purpose input/output signal pins |
| 43 | CDPORT2 | I/O | |
| 44 | XAPTFR | I | Mask operation select signal input pin for the LC8955 automatic request transfer |
| 45 | XIORD | O | IC read signal output pin for Intel peripheral ICs |
| 46 | XIOWR | O | Write signal output pin for Intel peripheral ICs |
| 47 | XCUSRIO | O | User I/O address select signal output pin |
| 48 | XCIO0 | O | Programmable I/O address select signal output pins |
| 49 | XCIO1 | O | |
| 50 | XCIO2 | O | |
| 51 | XCIO3 | O | |
| 52 | XCIO4 | O | |
| 53 | XCIO5 | O | |
| 54 | XCIO6 | O | |
| 55 | XCIO7 | O | |
| 56 | XCEXT0 | O | External address select signal output pins |
| 57 | XCEXT1 | O | |
| 58 | XCNVRAM | O | NVRAM address select signal output pin |
| 59 | XCVSC | O | VSC address select signal output pin |

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| Number | Name ¹ | I/O | Function |
|--------|-------------------|-----|--|
| 60 | V _{DD} | – | +5V supply pin |
| 61 | V _{SS} | – | Ground pin |
| 62 | XCROM0 | O | ROM address select signal output pins |
| 63 | XCROM1 | O | |
| 64 | XCROM2 | O | |
| 65 | XCROM3 | O | |
| 66 | ROMMOD1 | I | ROM mode select signal input pins |
| 67 | ROMMOD0 | I | |
| 68 | XDTACK | I/O | Data acknowledge signal input/output pin |
| 69 | XRW | I/O | Read/Write signal input/output pin |
| 70 | XLDS | I/O | Low-order data strobe signal input/output pin |
| 71 | XUDS | I/O | High-order data strobe signal input/output pin |
| 72 | XAS | I/O | Address strobe signal input/output pin |
| 73 | D0 | I/O | Data bus signal input/output pins |
| 74 | D1 | I/O | |
| 75 | D2 | I/O | |
| 76 | D3 | I/O | |
| 77 | D4 | I/O | |
| 78 | D5 | I/O | |
| 79 | D6 | I/O | |
| 80 | D7 | I/O | |
| 81 | V _{SS} | – | Ground pin |
| 82 | D8 | I/O | Data bus signal input/output pins |
| 83 | D9 | I/O | |
| 84 | D10 | I/O | |
| 85 | D11 | I/O | |
| 86 | D12 | I/O | |
| 87 | D13 | I/O | |
| 88 | D14 | I/O | |
| 89 | D15 | I/O | |
| 90 | V _{DD} | – | +5V supply pin |
| 91 | A23 | I/O | Address bus signal input/output pins |
| 92 | A22 | I/O | |
| 93 | A21 | I/O | |
| 94 | A20 | I/O | |
| 95 | A19 | I/O | |
| 96 | A18 | I/O | |
| 97 | A17 | I/O | |
| 98 | A16 | I/O | |
| 99 | V _{SS} | – | Ground pin |
| 100 | A15 | I/O | Address bus signal input/output pins |
| 101 | A14 | I/O | |
| 102 | A13 | I/O | |
| 103 | A12 | I/O | |
| 104 | A11 | I/O | |
| 105 | A10 | I/O | |
| 106 | A9 | I/O | |
| 107 | V _{DD} | – | +5V supply pin |
| 108 | A8 | I/O | Address bus signal input/output pins |
| 109 | A7 | I/O | |
| 110 | A6 | I/O | |
| 111 | A5 | I/O | |
| 112 | A4 | I/O | |
| 113 | A3 | I/O | |
| 114 | A2 | I/O | |
| 115 | A1 | I/O | |
| 116 | V _{SS} | – | Ground pin |
| 117 | XIPL2 | O | Interrupt level signal output pins for the MPU |
| 118 | XIPL1 | O | |
| 119 | XIPL0 | O | |

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| Number | Name ¹ | I/O | Function |
|--------|-------------------|-----|---|
| 120 | V _{DD} | – | +5V supply pin |
| 121 | FC0 | I/O | MPU function code signal input/output pins |
| 122 | FC1 | I/O | |
| 123 | FC2 | I/O | |
| 124 | XBERR | O | Bus error signal output pin |
| 125 | XRESET | I | Reset signal input pin |
| 126 | XHALT | I | Halt signal input pin |
| 127 | CPUCLK | O | MPU clock signal output pin |
| 128 | XDBDIR | O | Data bus direction signal output pin |
| 129 | XBR | O | DMA bus request signal output pin |
| 130 | XBG | I | DMA bus request-granted signal input pin |
| 131 | XBGACK | O | DMA bus request-granted acknowledge signal output pin |
| 132 | XOWN | O | DMA cycle active signal output pin |
| 133 | XEXTDMA1 | I/O | DMA signal input/output pins |
| 134 | XEXTDMA0 | I/O | |
| 135 | XEXTBGAK | I | External DMA bus request-granted acknowledge signal input pin |
| 136 | XCS | I | Address decoder mode select signal input pin |
| 137 | CLKSEL | I | Master clock (CPUCLK) divider select signal input pin |
| 138 | XSWAP | I | Memory swap function select signal input pin |
| 139 | ORGCLK | I | Clock input pin |
| 140 | V _{DD} | – | +5V supply pin |
| 141 | V _{SS} | – | Ground pin |
| 142 | TICKCLK | I | External clock input pin for the tick generator |
| 143 | XIACKALL | O | Interrupt acknowledge common signal output pin |
| 144 | XIACK5 | O | Interrupt acknowledge signal output pins |
| 145 | XIACK4 | O | |
| 146 | XIACK3 | O | |
| 147 | XIACK2 | O | |
| 148 | XIACK1 | O | |
| 149 | XIACK0 | O | |
| 150 | XIRQ5 | I | Interrupt request signal input pins |
| 151 | XIRQ4 | I | |
| 152 | XIRQ3 | I | |
| 153 | XIRQ2 | I | |
| 154 | XIRQ1 | I | |
| 155 | XIRQ0 | I | |
| 156 | RXD | I | Mouse data signal input pin |
| 157 | APSEL0 | O | General-purpose output port pins |
| 158 | APSEL1 | O | |
| 159 | APSEL2 | O | |
| 160 | V _{DD} | – | +5V supply pin |

1. An “X” at the beginning of a pin name indicates negative logic.

Specifications

Absolute Maximum Ratings at $V_{SS} = 0V$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------|-----------------------|------------------------|------------|
| Maximum supply voltage | $V_{DD\ max}$ | $T_a=25^\circ C$ | -0.3 to +7.0 | V |
| Input and output voltage | V_I, V_O | $T_a=25^\circ C$ | -0.3 to $V_{DD} + 0.3$ | V |
| Allowable power dissipation | $P_d\ max$ | $T_a \leq 70^\circ C$ | 400 | mW |
| Operating temperature range | T_{opr} | | -30 to +70 | $^\circ C$ |
| Storage temperature range | T_{stg} | | -55 to +125 | $^\circ C$ |
| Soldering temperature | T_{sol} | Manual soldering, 3s | 350 | $^\circ C$ |
| | | Reflow soldering, 10s | 235 | $^\circ C$ |

Allowable Operating Ranges at $T_a = -30$ to $+70^\circ C$, $V_{SS} = 0V$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------|----------|------------|---------|-----|----------|------|
| | | | min | typ | max | |
| Supply voltage | V_{DD} | | 4.5 | 5.0 | 5.5 | V |
| Input voltage range | V_{IN} | | 0 | | V_{DD} | V |

DC Electrical Characteristics at $T_a = -30$ to $+70^\circ C$, $V_{SS} = 0V$, $V_{DD} = 4.5$ to $5.5V$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|-----------|---|--------------|-----|-----|---------|
| | | | min | typ | max | |
| Input high-level voltage | V_{IH1} | TTL compatible: All input pins (including bidirectional pins) except those listed in notes 1 and 2. | 2.2 | | | V |
| Input low-level voltage | V_{IL1} | | | | 0.8 | V |
| Input high-level voltage | V_{IH2} | TTL-compatible Schmitt: See note 1. | 2.5 | | | V |
| Input low-level voltage | V_{IL2} | | | | 0.6 | V |
| Output high-level voltage | V_{OH1} | $I_{OH} = -3mA$ | 2.4 | | | V |
| Output low-level voltage | V_{OL1} | $I_{OL} = 3mA$ | | | | |
| Input leakage current | I_L | $V_I = V_{SS}, V_{DD}$ | -25 | | +25 | μA |
| Output leakage current | I_{OZ} | High-impedance output | | | | |
| Input high-level voltage | V_{IH3} | CMOS compatible: ORGCLK (pin 139) | 0.7 V_{DD} | | | V |
| Input low-level voltage | V_{IL3} | | | | | |
| Output high-level voltage | V_{OH2} | $I_{OH} = -6mA$ | 2.4 | | | V |
| Output low-level voltage | V_{OL2} | $I_{OL} = 6mA$ | | | | |
| | | XDTACK (pin 68), D0 to D15 (pins 73 to 89) | | | 0.4 | V |

Notes

1. DATAEMP (pin 2), UNDFLOW (pin 3), BUFFULL (pin 4), BUSY (pin 5), XSTEN (pin 33), XD TEN (pin 34), DRQWAIT (pin 35), XAP TFR (pin 44), XRESET (pin 125), XHALT (pin 126), XEXTBGAK (pin 135), XIRQ0 to 5 (pins 150 to 155), RXD (pin 156)
2. ORGCLK (pin 139)
3. XDTACK (pin 68), D0 to D15 (pins 73 to 89)

Internal Functional Blocks

The PUPPET consists of about 10 functional blocks. See the “Block Diagram”.

PADEC (Programmable Address Decoder)

The PADEC functional block is used to generate the chip select (CS) signals for ROM, RAM, I/O devices and so on. The CS signal addresses are programmable, which enables address allocation specific to your system configuration.

DTAKGEN (Programmable DTACK Generator)

The DTAKGEN functional block is used to generate the data acknowledge signals for the chip select address space selected by the PADEC. The access speed of peripheral IC devices is generally slower than that of the main processing unit (MPU). To adjust this speed gap between them, the user is allowed to insert from 0 to 4 wait cycles into each address cycle. The number of wait cycles to be inserted is programmable. In addition, the user is permitted to disable the DTACK (active low) generator so that it can be generated by an external device.

PINTH (Programmable Interrupt Handler)

The PINTH functional block is used as an interrupt handler to output the vectored numbers corresponding to the 68000 MPU vectored interrupts. Each of the IPL levels and vectored numbers for internal block/external interrupt requests is programmable.

RCHIPIF (LC8951 RCHIP Interface)

The RCHIPIF functional block is used to provide the interface between the 68000 MPU and the LC8951 RCHIP. This interface enables direct communication between them. As a result, status data, data signal and error bit information can be directly communicated between them.

ADPCMIF (LC8955 Interface)

The ADPCMIF functional block is used to provide the interface between the 68000 MPU and the LC8955. This interface enables direct communication between them. As a result, data can be directly read from or written to internal registers of the LC8955 from the MPU.

TICKGEN (Tick Generator)

The TICKGEN functional block is used to generate timer interrupt clocks for a real-time operating system. The timer interrupt clocks can be generated by dividing the system clock or selecting an external input clock. As a result, the tick can be set independent of the system clock frequency.

MOUSEIF (Serial Mouse Interface)

The MOUSEIF functional block is used as the data receive port for a standard serial mouse. The communication parameters such as parity bit, stop bit, data bits and baud rate can be changed by software. In addition, the interrupt signal generation timing can be set to either 3-byte or 1-byte intervals. Therefore, this functional block can be used as a general-purpose receive serial port as well as the mouse serial port. Note that the mouse transmits an XY coordinate value to the serial port in 3-byte packets.

MPDMAC (Micro-Programmable DMA Controller)

The MPDMAC functional block is used as the DMA controller. With this controller, the operation can be programmed by a 16-instruction micro code. These instructions can be programmed to support data read operations from the LC8951 (RCHIP), data write operations to the LC8955 as well as the basic transfer operations with memory. In addition, they include rather complicated instructions to enable data comparison, logical operation and conditional jump operations. Therefore, this controller block can be used as a sub-CPU to enable intelligent processing, and to reduce the load on the MPU.

BERRGEN (Bus Error Generator)

The BERRGEN functional block is used to generate the bus error signal for the 68000 MPU when no AS (active low) signal is detected. There are four AS signal inactive periods. The user is allowed to select one from the four to best suit the application system in mind.

CLKDIV (Clock Divider Circuit)

The CLKDIV function block is used to generate the MPU clock with 1:1 duty cycle by dividing the master clock by 2.

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