Ordering number : EN5964

CMOS IC

LC75750E, 75750W

1/3 Duty VFD Driver

Overview

The LC75750E and LC75750W are 1/3 duty VFD drivers that can be used for electronic tuning frequency display and other applications under the control of a micro-controller. These products can directly drive VFDs with up to 264 segments.

Features

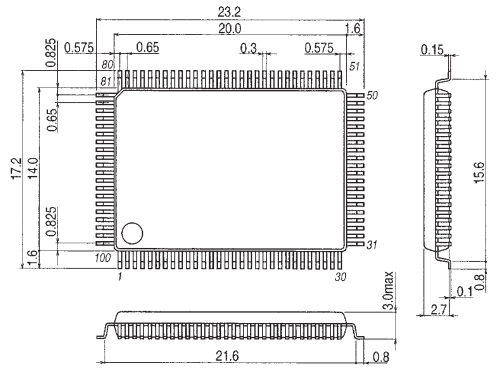
- 264 segment outputs.
- Noise reduction circuits are built into the output drivers.
- Serial data input supports CCB format communication with the system controller.
- Dimmer can be controlled by serial data input.
- High generality since display data is displayed without the intervention of a decoder.
- All segments can be turned off with the $\overline{\text{BLK}}$ pin.

Package Dimensions

unit: mm

3151-QFP100E

[LC75750E]

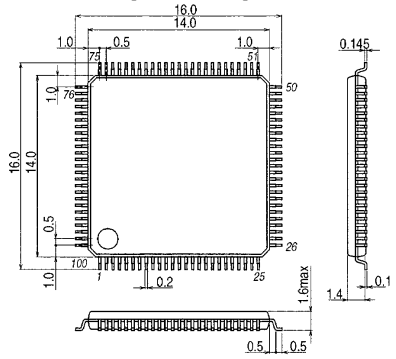


SANYO: QFP100E (QIP100E)

unit: mm

3181B-SQFP100

[LC75750W]



SANYO: SQFP100

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +6.5	V
	V_{FL} max	V_{FL}	–0.3 to +21.0	V
Input voltage	$V_{IN}1$	DI, CL, CE, $\overline{BLK}$	–0.3 to +6.5	V
	$V_{IN}2$	OSCI	–0.3 to V_{DD} +0.3	V
Output voltage	$V_{OUT}1$	S1 to S88, G1 to G3	–0.3 to V_{FL} +0.3	V
	$V_{OUT}2$	OSCO	–0.3 to V_{DD} +0.3	V
Output current	$I_{OUT}1$	S1 to S88	6	mA
	$I_{OUT}2$	G1 to G3	60	mA
Allowable power dissipation	Pd max	Ta = 85°C (LC75750E)	500	nW
		Ta = 85°C (LC75750W)	450	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +150	°C

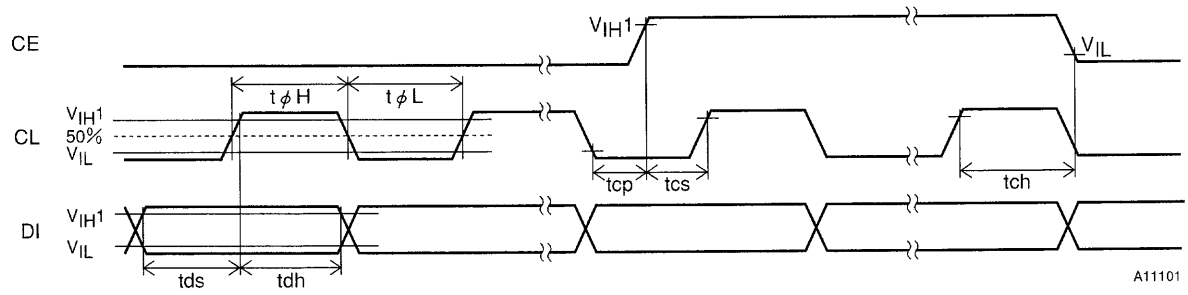
Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5	5.0	5.5	V
	V_{FL}	V_{FL}	8	12	18	V
Input high-level voltage	$V_{IH}1$	DI, Cl, CE, $\overline{BLK}$	0.8 V_{DD}		5.5	V
	$V_{IH}2$	OSCI	0.8 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL}	DI, CL, CE, $\overline{BLK}$, OSCI	0		0.2 V_{DD}	V
Guaranteed oscillator range	f_{OSC}	OSCI, OSCO	0.9	2.4	3.7	MHz
Recommended external resistance	R_{OSC}	OSCI, OSCO	2.2	12	47	KΩ
Recommended external capacitance	C_{OSC}	OSCI, OSCO	15	33	100	pF
Low level clock pulse width	$t_{øL}$	CL : Figure 1	160			ns
High level clock pulse width	$t_{øH}$	CL : Figure 1	160			ns
Data setup time	t_{ds}	DI, CL : Figure 1	160			ns
Data hold time	t_{dh}	DI, CL : Figure 1	160			ns
CE wait time	t_{cp}	CE, CL : Figure 1	160			ns
CE setup time	t_{cs}	CE, CL : Figure 1	160			ns
CE hold time	t_{ch}	CE, CL : Figure 1	160			ns
$\overline{BLK}$ switching time	t_c	$\overline{BLK}$, CE : Figure 3	10			µs

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH}1$	DI, CL, CE, $\overline{BLK}$: V_{IN} = 5.5V			5	µA
	$I_{IH}2$	OSCI : V_{IN} = V_{DD}			5	µA
Input low-level current	I_{IL}	DI, CL, CE, $\overline{BLK}$, OSCI : V_{IN} = 0V	–5			µA
Output high-level voltage	$V_{OH}1$	S1 to S88 : I_O = –2 mA	V_{FL} – 0.6			V
	$V_{OH}2$	G1 to G3 : I_O = –50 mA	V_{FL} – 1.3			V
	$V_{OH}3$	OSCO : I_O = –0.5 mA	V_{DD} – 2.0			V
Output low-level voltage	$V_{OL}1$	S1 to S88, G1 to G3 : I_O = 50 µA			0.5	V
	$V_{OL}2$	OSCO :I_O = 0.5mA			2.0	V
Oscillator frequency	f_{OSC}	R_{OSC} = 12 kΩ, C_{OSC} = 33 pF		2.4		MHz
Hysteresis voltage	V_H	DI, CL, CE, $\overline{BLK}$		0.1 V_{DD}		V
Current drain	I_{DD}	Outputs open : f_{OSC} = 2.4 MHz			10	mA

• When CL is stopped at the low level



• When CL is stopped at the high level

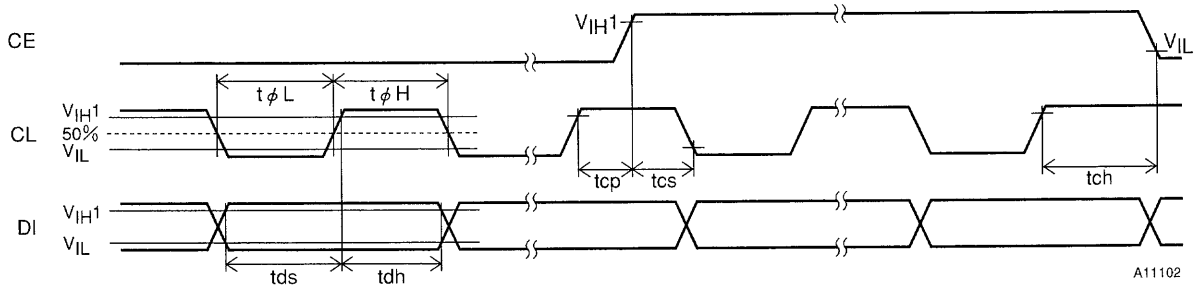
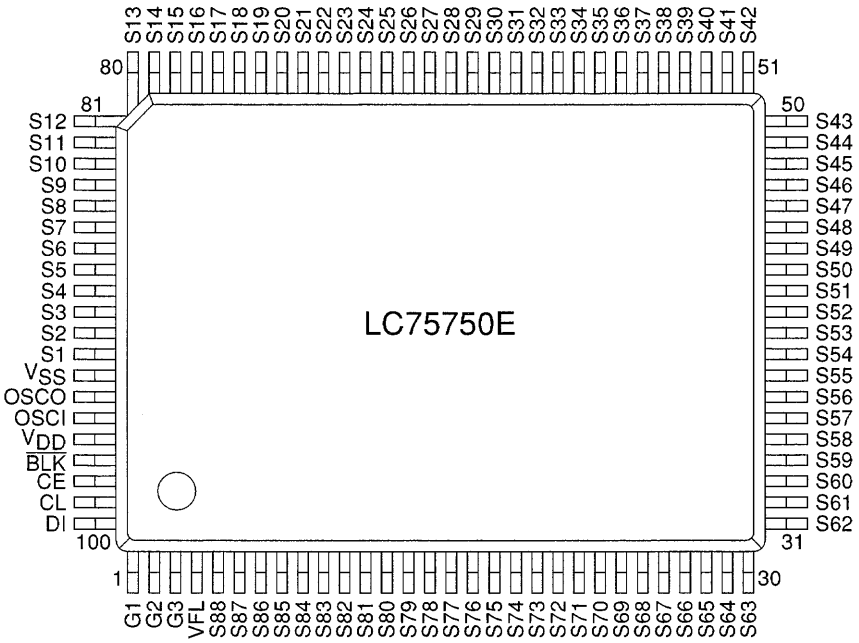


Figure 1

Pin Assignment

(Top view)



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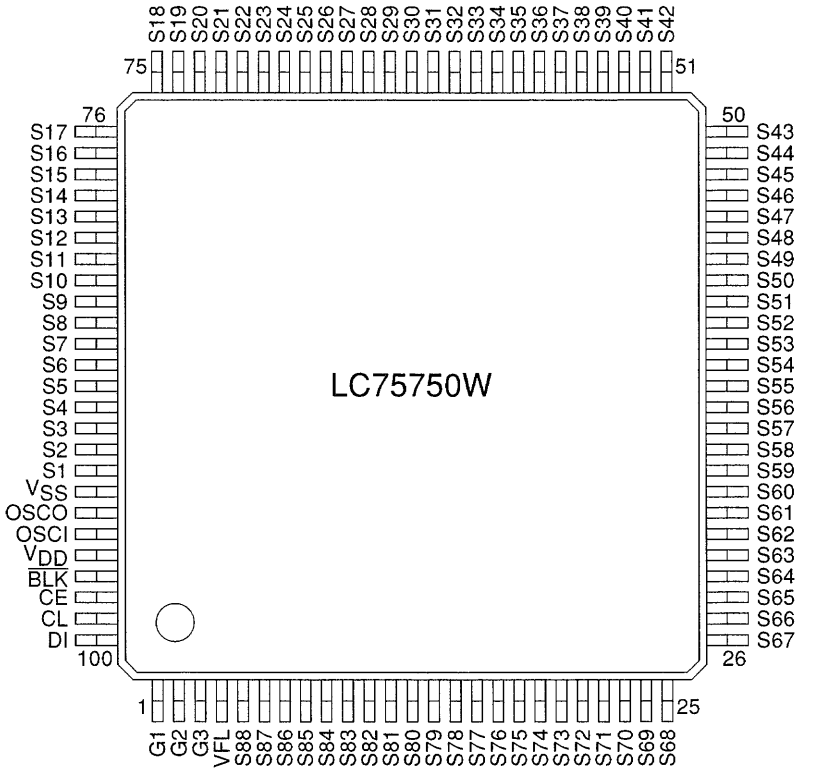

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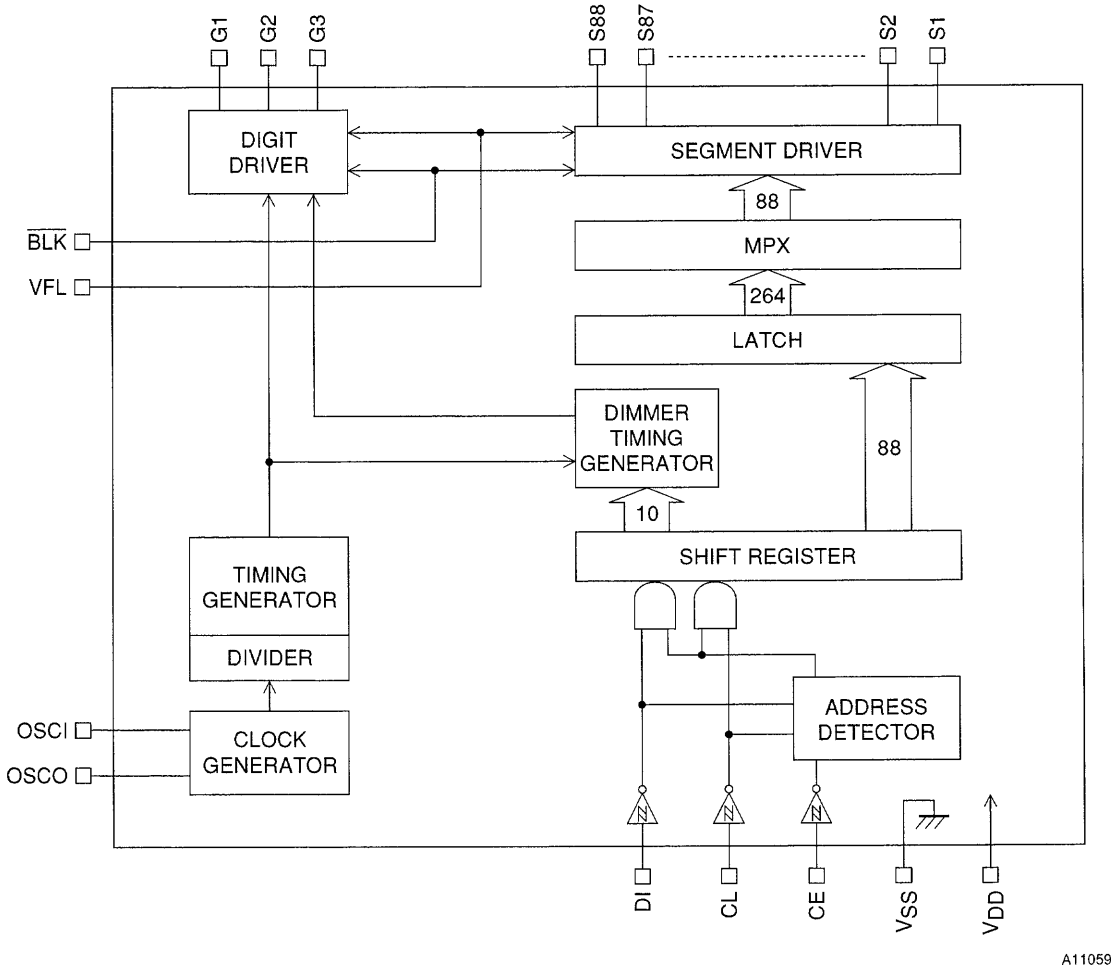
Block Diagram

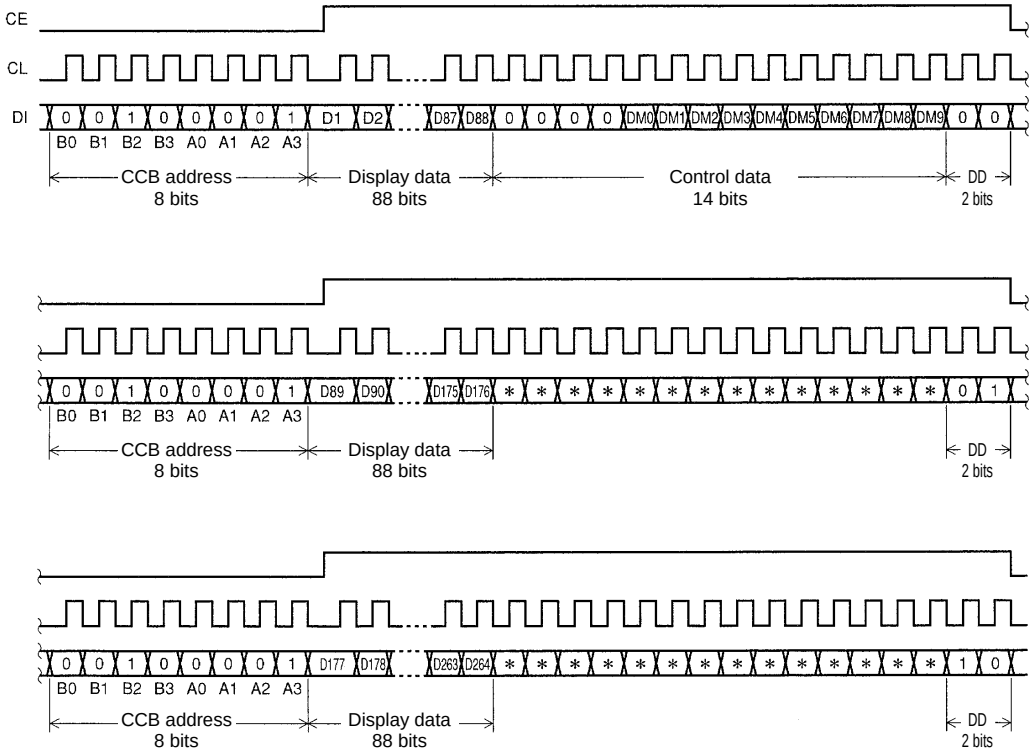


Pin Functions

Pin No.	Pin	Function	I/O	Handling when unused
4	V_{FL}	Driver block power supply. A voltage of between 8.0 and 18.0 V must be supplied.	—	—
96	V_{DD}	Logic block power supply. A voltage of between 4.5 and 5.5 V must be supplied.	—	—
93	V_{SS}	Power supply. Must be connected to the system ground.	—	—
95	OSCI	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to these pins.	I	GND
94	OSCO		O	OPEN
97	$\overline{BLK}$	Display off control input. $\overline{BLK}$ = L (V_{SS}) .....Display off (S1 to S24, G1 to G3 = L) $\overline{BLK}$ = H (V_{DD}) .....Display on Note that serial data can be transferred while the display is turned off.	I	GND
99	CL	Serial data transfer inputs. These pins must be connected to the system microcontroller. CL : Synchronization clock DI : Transfer data CE : Chip enable	I	GND
100	DI			
98	CE			
1 to 3	G1 to G3	Digit outputs. The frame frequency fo is (f_{OSC}/6144)Hz.	O	OPEN
92 to 5	S1 to S88	Segment outputs for displaying the display data transferred by serial data input	O	OPEN

Serial Data Transfer Format

• When CL is stopped at the low level



• When CL is stopped at the high level

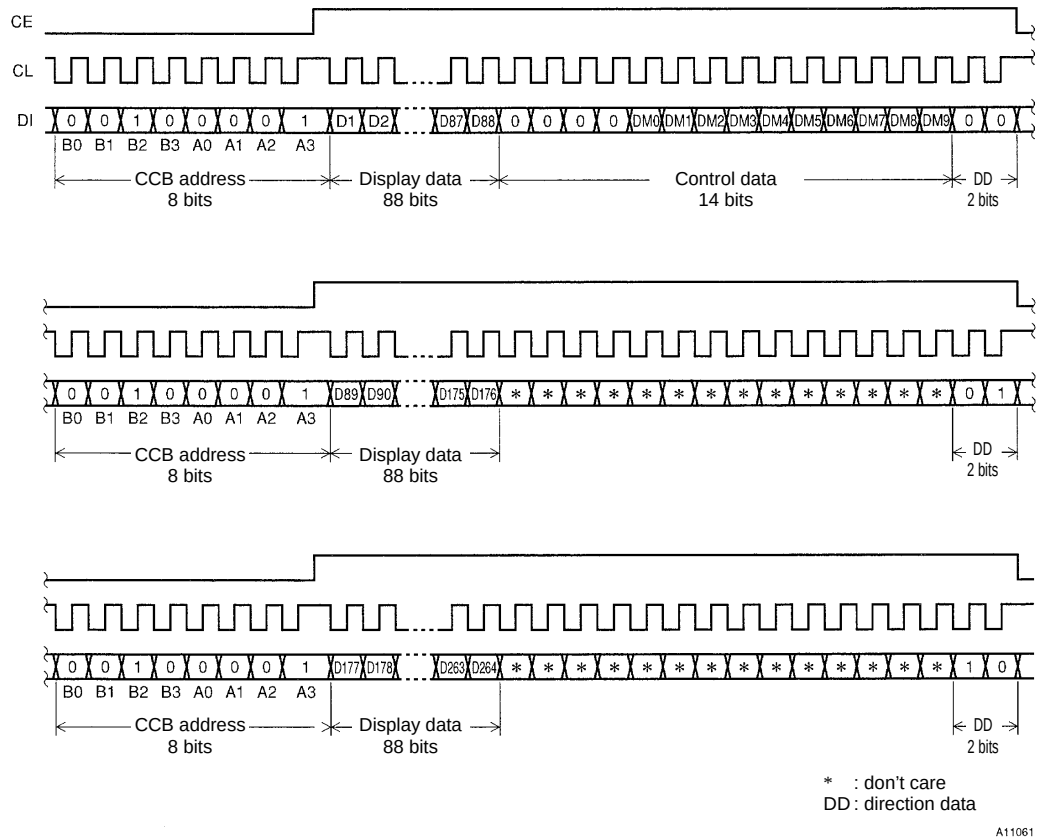


Figure 2

CCB address : Transfer 00100001B (84_H) as shown in Figure 2

DM0 to DM9 : Dimmer data

This data controls the duty of the G1 to G3 digit output pins, and consists of 10 bits with DM0 being the LSB. Note that the intensity of the display can be adjusted by controlling the duty of the G1 to G3 digit output pins.

The relationship between the dimmer data and the dimmer value is as follows.

DM9	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	Dimmer value (t4/t3)
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
0	0	0	0	0	0	0	0	1	0	2/1024
⋮										⋮
1	1	1	1	1	1	1	1	0	0	1020/1024
1	1	1	1	1	1	1	1	0	1	1021/1024
1	1	1	1	1	1	1	1	1	0	1022/1024
1	1	1	1	1	1	1	1	1	1	Not used

t3, t4 : See Figure 4.

D1 to D88 : Display data for the G1 digit output pin.

Dn (n = 1 to 88) = 1 : On

Dn (n = 1 to 88) = 0 : Off

D89 to D176 : Display data for the G2 digit output pin.

Dn (n = 89 to 176) = 1 : On

Dn (n = 89 to 176) = 0 : Off

D177 to D264 : Display data for the G3 digit output pin.

Dn (n = 177 to 264) = 1 : On

Dn (n = 177 to 264) = 0 : Off

Correspondence between Display Data (D1 to D264) and Segment Output Pins

Segment output pins	G1	G2	G3
S1	D1	D89	D177
S2	D2	D90	D178
S3	D3	D91	D179
S4	D4	D92	D180
S5	D5	D93	D181
S6	D6	D94	D182
S7	D7	D95	D183
S8	D8	D96	D184
S9	D9	D97	D185
S10	D10	D98	D186
S11	D11	D99	D187
S12	D12	D100	D188
S13	D13	D101	D189
S14	D14	D102	D190
S15	D15	D103	D191
S16	D16	D104	D192
S17	D17	D105	D193
S18	D18	D106	D194
S19	D19	D107	D195
S20	D20	D108	D196
S21	D21	D109	D197
S22	D22	D110	D198
S23	D23	D111	D199
S24	D24	D112	D200
S25	D25	D113	D201
S26	D26	D114	D202
S27	D27	D115	D203
S28	D28	D116	D204
S29	D29	D117	D205
S30	D30	D118	D206

Segment output pins	G1	G2	G3
S31	D31	D119	D207
S32	D32	D120	D208
S33	D33	D121	D209
S34	D34	D122	D210
S35	D35	D123	D211
S36	D36	D124	D212
S37	D37	D125	D213
S38	D38	D126	D214
S39	D39	D127	D215
S40	D40	D128	D216
S41	D41	D129	D217
S42	D42	D130	D218
S43	D43	D131	D219
S44	D44	D132	D220
S45	D45	D133	D221
S46	D46	D134	D222
S47	D47	D135	D223
S48	D48	D136	D224
S49	D49	D137	D225
S50	D50	D138	D226
S51	D51	D139	D227
S52	D52	D140	D228
S53	D53	D141	D229
S54	D54	D142	D230
S55	D55	D143	D231
S56	D56	D144	D232
S57	D57	D145	D233
S58	D58	D146	D234
S59	D59	D147	D235
S60	D60	D148	D236

Segment output pins	G1	G2	G3
S61	D61	D149	D237
S62	D62	D150	D238
S63	D63	D151	D239
S64	D64	D152	D240
S65	D65	D153	D241
S66	D66	D154	D242
S67	D67	D155	D243
S68	D68	D156	D244
S69	D69	D157	D245
S70	D70	D158	D246
S71	D71	D159	D247
S72	D72	D160	D248
S73	D73	D161	D249
S74	D74	D162	D250
S75	D75	D163	D251
S76	D76	D164	D252
S77	D77	D165	D253
S78	D78	D166	D254
S79	D79	D167	D255
S80	D80	D168	D256
S81	D81	D169	D257
S82	D82	D170	D258
S83	D83	D171	D259
S84	D84	D172	D260
S85	D85	D173	D261
S86	D86	D174	D262
S87	D87	D175	D263
S88	D88	D176	D264

Example : Segment output pin S11 is controlled as follows :

Display data			Segment output pin S11 state
D11	D99	D187	
0	0	0	The segments corresponding to the G1, G2, and G3 digit output pins are off
0	0	1	The segments corresponding to the G3 digit output pin are on
0	1	0	The segments corresponding to the G2 digit output pin are on
0	1	1	The segments corresponding to the G2 and G3 digit output pins are on
1	0	0	The segments corresponding to the G1 digit output pin are on
1	0	1	The segments corresponding to the G1 and G3 digit output pins are on
1	1	0	The segments corresponding to the G1 and G2 digit output pins are on
1	1	1	The segments corresponding to the G1, G2, and G3 digit output pins are on

$\overline{\text{BLK}}$ and the Display Control

Since the IC internal data (D1 to D264 and the control data) is undefined when power is first applied, the display is off (S1 to S88, G1 to G3 = low) by setting the $\overline{\text{BLK}}$ pin low at the same time as power is applied. Then, meaningless display at power on can be prevented by transferring all 336 bits of serial data from the controller and setting $\overline{\text{BLK}}$ pin high after the transfer completes while the display is off. (See Figure 3.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 3.)

- Power on : Logic block power supply (V_{DD}) on $\rightarrow$ Driver block power supply (V_{FL}) on
- Power off : Driver block power supply (V_{FL}) off $\rightarrow$ Logic block power supply (V_{DD}) off

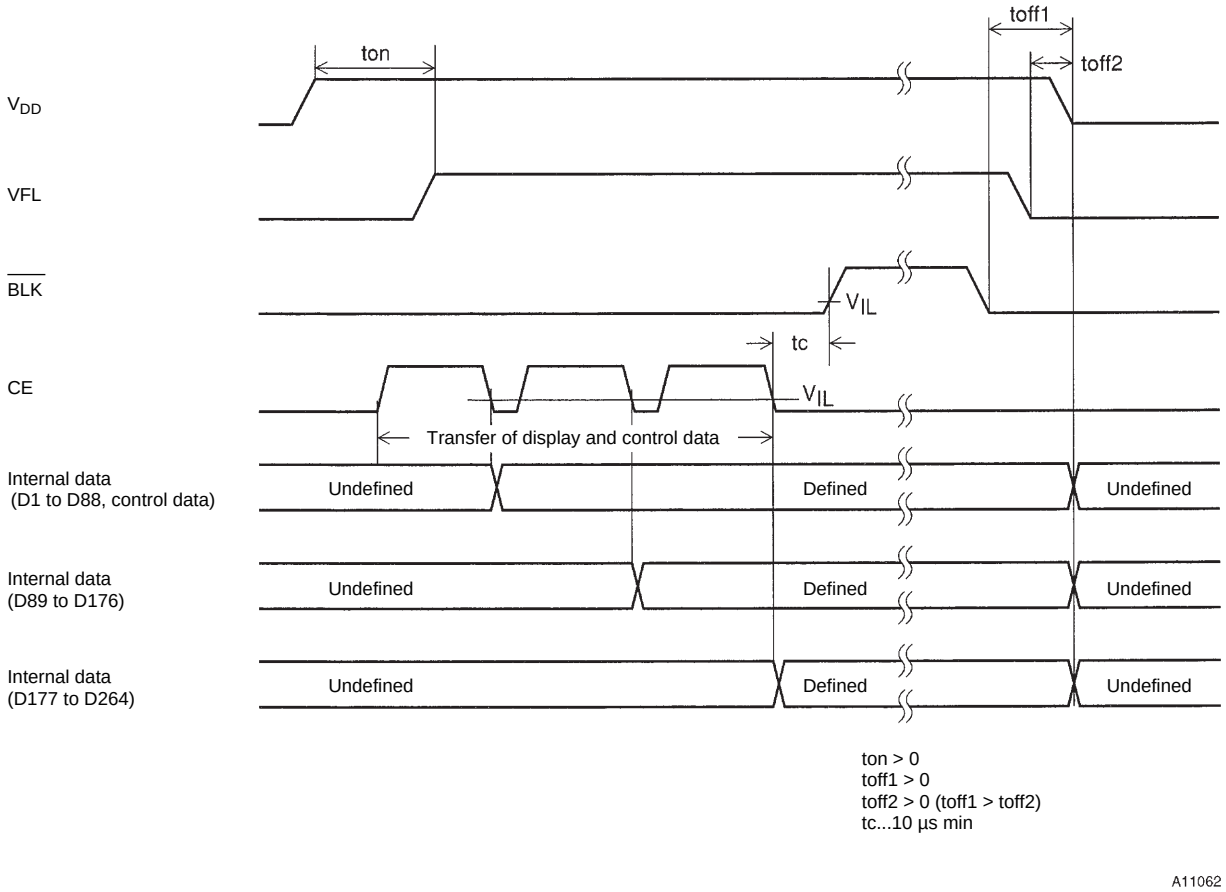
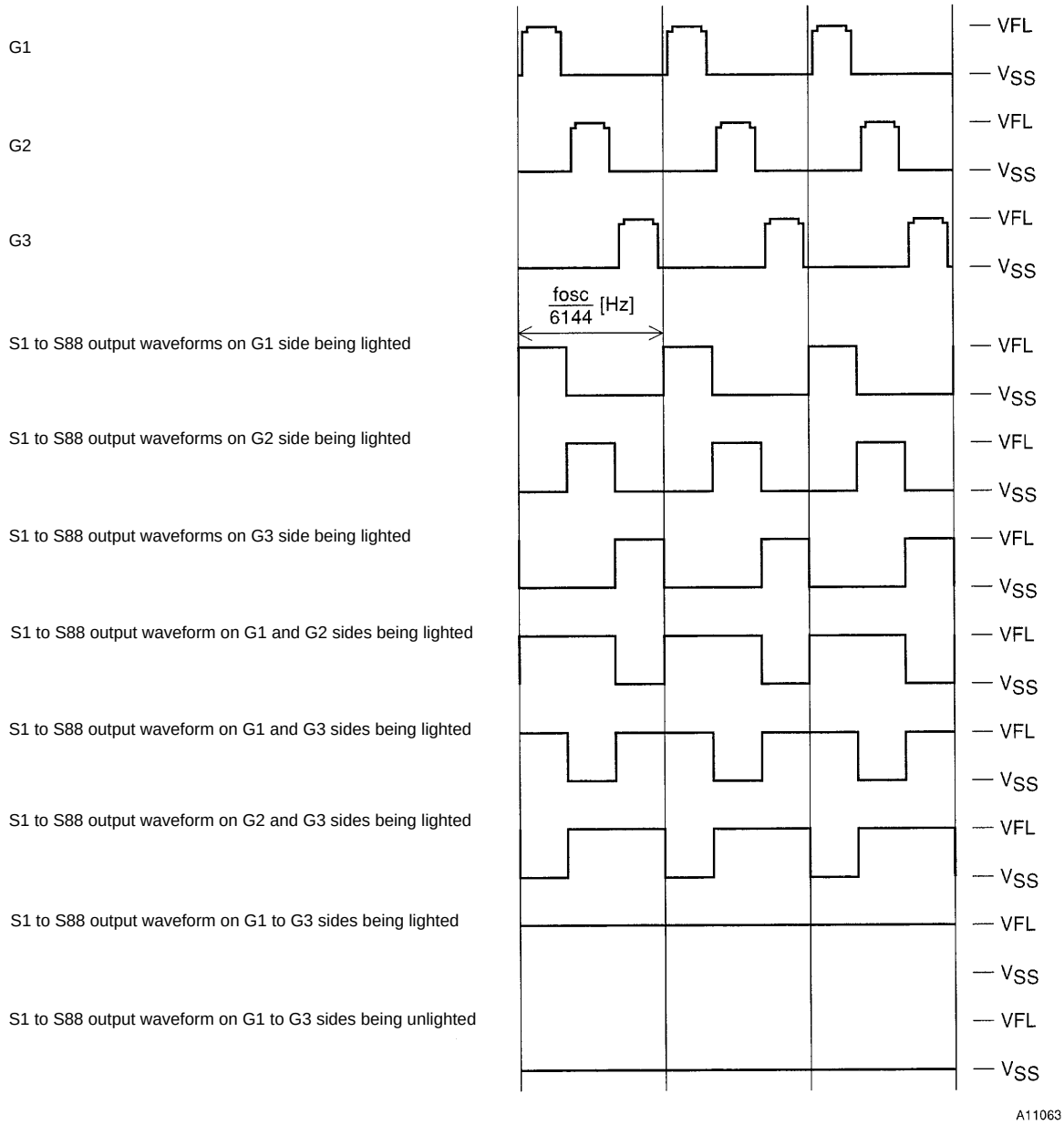


Figure 3

Output Waveforms (S1 to S88)



Relationship between Segment and Digit outputs

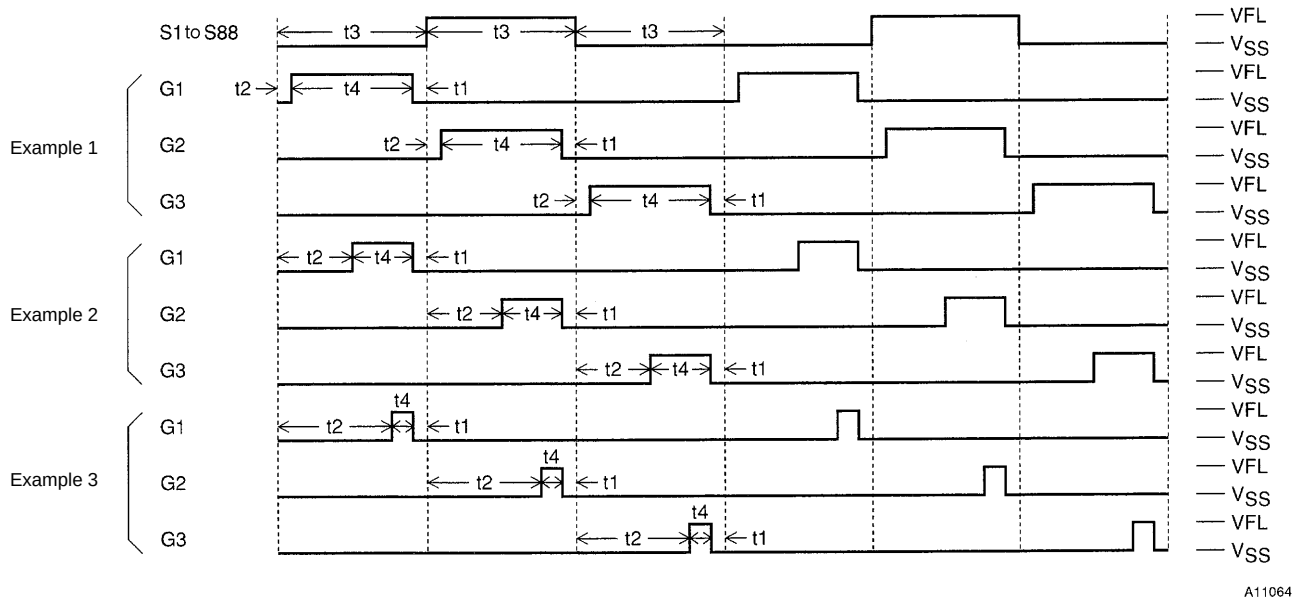


Figure 4

- Consider the examples shown in Figure 4, where display data is set up so that the segment outputs S1 to S88 output V_{SS} level on the G1 and G3 digit output timing and V_{FL} level on the G2 digit output timing. (Here, the G2 side being lighted) The relationship between the time t3 and the oscillator frequency f_{OSC} is $t3 = 2048/f_{OSC}$.
- The digit output G1 to G3 waveforms in Example 1 are output when the dimmer data (DM0 to DM9) are set to 3FEH. The relationship between the time t1 and the oscillator frequency f_{OSC} is $t1=2/f_{OSC}$. Note that the time t1 and the time t2 are the same period in Example 1.
- The digit output G1 to G3 waveforms in Example 2 are those when the dimmer data (DM0 to DM9) are set to a smaller value. Although the time t1 does not change, the time t2 becomes longer.
  When the dimmer data (DM0 to DM9) are set to $1FF_H$ and the oscillator frequency fosc is 2.4 [MHz], then the time t2 is :

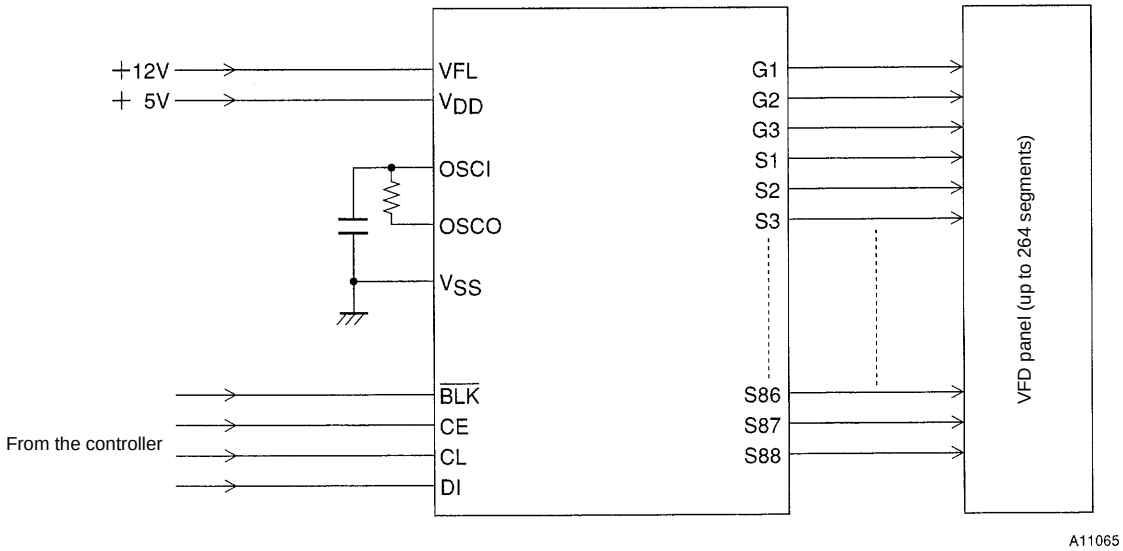
$$t2 = t3 - t1 \times (1FF_H + 1)$$

$$= \frac{1024}{f_{OSC}}$$

$$= 0.43[ms]$$

- When the dimmer data (DM0 to DM9) are set to an even smaller value, the time t2 becomes even longer, as in example 3. Note that the time t1 does not change here, either.

Sample Application Circuit



Notes on the segment and digit waveforms

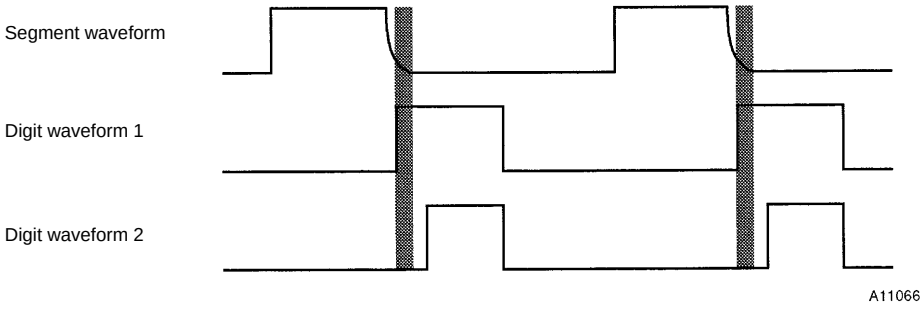


Figure 5

The segment waveform is distorted by the VFD panel used and the wiring, and furthermore, in the case of being used with essentially no dimming as in the digit waveform 1, as shown in Figure 5, the VFD panel glow dimly. By carefully considering the segment waveform, it can be seen that this problem can be resolved by applying an adequate amount of dimming, as shown in digit waveform 2.

Notes on transferring display data from the controller

Since display data is transferred in three operations as shown in Figure 2, we recommend that all display data be transferred within 30 [ms] to prevent degradation of the visual quality of the displayed image.