Ordering number: EN5421

Monolithic Linear IC

LA8518NM

Signal Processor for Cordless Telephone Base Sets

Functions

Speech network block
- 2-wire/4-wire conversion
- Line driver
- Transmitting amplifier
- Receiving amplifier (with ATT)
- Power supply switching circuit
- Impedance matching
- DTMF interface
- Key tone interface
- BN circuit network switching circuit
  (BN = Balancing Network)

Signal processor block
- Record preamplifier (with ALC)
- Record amplifier
- Power amplifier (V_{CC} = 5 V, R_L = 8 Ω, P_O = 200 mW)
- Playback equalizer amplifier
- Voice detector (VOX)
- Electronic volume control (4 dB, 7 steps)

Crosspoint switch block
- Crosspoint switches (mixing available)
- CPU interface

Features

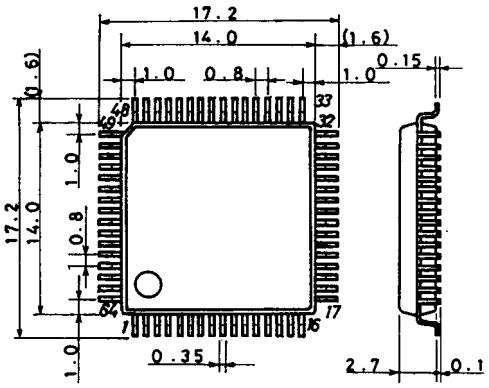
- Because it is possible to switch the Balancing Network between two systems, one for the near end and one for the far end, in accordance with the line current, this IC provides excellent sidetone characteristics over a wide range of line currents.
- Receiver amplifier supports ceramic receivers and dynamic receivers.
- Power amplifier on chip
  (V_{CC} = 5 V, R_L = 8 Ω, P_O = 200 mW).
- Crosspoint switches allow full mixing, permitting the implementation of a variety of functions, such as three- or four-way calls.
- Digital volume control on chip (power system output).

Package Dimensions

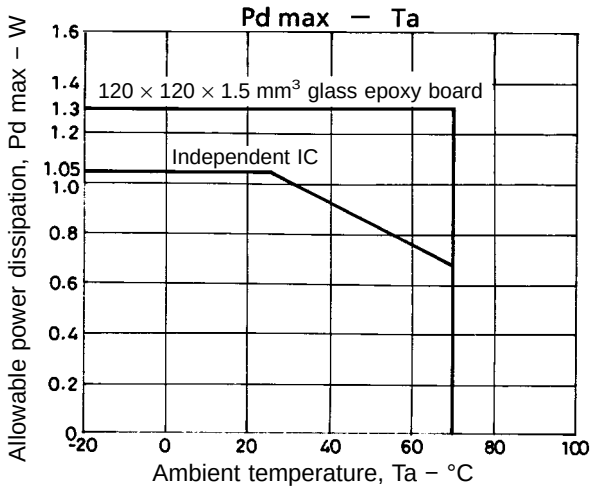
unit : mm

3159-QFP64E

[LA8515NM]



SANYO : QIP64E



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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_L max	Speech network block	15	V
	V_{CC} max	Other than speech network block	10	V
Line current	I_L max		130	mA
Allowable power dissipation	Pd max		1.05	W
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Other than speech network block	5	V
Operating supply voltage range	V_{CC} op		4.5 to 7.5	V

Operating Characteristics at Ta = 25°C, f = 1 kHz

Parameter	Symbol	Conditions	min	typ	max	Unit
[Speech Network Block (External power supply operating characteristics)]						
Line voltage	V_L	I_L = 20 mA	3.3	3.9	4.3	V
		I_L = 50 mA	4.9	5.7	6.5	V
		I_L = 120 mA	7.8	9.3	10.8	V
Internal supply voltage	V_{SP}	I_L = 20 mA	4.5	4.8	5.0	V
		I_L = 50 mA	4.5	4.8	5.0	V
		I_L = 120 mA	4.5	4.8	5.0	V
Transmitting gain	G_T	I_L = 20 mA, V_{IN} = –55 dBV	43	45	47	dB
		I_L = 120 mA, V_{IN} = –55 dBV	39	41	43	dB
Receiving gain	G_R	I_L = 20 mA, V_{IN} = –20 dBV	–3.0	–1.0	+1.0	dB
		I_L = 120 mA, V_{IN} = –20 dBV	–9.5	–7.5	–5.5	dB
DTMF gain	G_{MF}	I_L = 20 mA, V_{IN} = –30 dBV	28	30	32	dB
		I_L = 120 mA, V_{IN} = –30 dBV	24	26	28	dB
KT gain	G_{KT}	I_L = 20 mA, V_{IN} = –40 dBV	9	11	13	dB
		I_L = 120 mA, V_{IN} = –40 dBV	9	11	13	dB
Transmitting dynamic range	DR_T	I_L = 20 mA, THD = 4%	2.5			Vp-p
		I_L = 120 mA, THD = 4%	4.5			Vp-p
Receiving dynamic range (Single R_L = 150 Ω)	DR_{DR}	I_L = 20 mA, THD = 10%	0.5			Vp-p
		I_L = 120 mA, THD = 10%	0.5			Vp-p
Receiving dynamic range (BTL R_L = 3 kΩ)	DR_{SR}	I_L = 20 mA, THD = 10%	5			Vp-p
		I_L = 120 mA, THD = 10%	5			Vp-p
MUTE high-level input voltage	V_{IH}	I_L = 20 mA to 120 mA	0.6VSP			V
MUTE low-level input voltage	V_{IL}	I_L = 20 mA to 120 mA	0		0.4	V
Transmitting PADC attenuation	ΔG_T	I_L = 30 mA, ground at 24 kΩ		3.6		dB
Receiving PADC attenuation	ΔG_R	I_L = 30 mA, ground at 24 kΩ		6.5		dB
Internal reference voltage	V_{REF}	I_L = 20 mA		2.3		V
		I_L = 50 mA		2.3		V
		I_L = 120 mA		2.3		V
[Speech Network Block (Operating characteristics when power is off)]						
Line voltage	V_L	I_L = 20 mA	3.3	3.8	4.3	V
		I_L = 50 mA	4.8	5.4	6.2	V
		I_L = 120 mA	7.2	8.7	10.2	V
Internal supply voltage	V_{SP}	I_L = 20 mA	1.7	1.9	2.1	V
		I_L = 50 mA	2.5	2.8	3.1	V
		I_L = 120 mA	4.55	4.85	5.15	V

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Parameter	Symbol	Conditions	min	typ	max	Unit
Transmitting gain	G_T	I_L = 20 mA, V_{IN} = –55 dBV	42	44	46	dB
		I_L = 120 mA, V_{IN} = –55 dBV	39	41	43	dB
Receiving gain	G_R	I_L = 20 mA, V_{IN} = –20 dBV	–4.5	−2.5	–0.5	dB
		I_L = 120 mA, V_{IN} = –20 dBV	–9	–7	–5	dB
DTMF gain	G_{MF}	I_L = 20 mA, V_{IN} = –30 dBV	27	29	31	dB
		I_L = 120 mA, V_{IN} = –30 dBV	24	26	28	dB
KT gain	G_{KT}	I_L = 20 mA, V_{IN} = –40 dBV	6.7	8.7	10.7	dB
		I_L = 120 mA, V_{IN} = –40 dBV	9	11	13	dB
Transmitting dynamic range	DR_T	I_L = 20 mA, THD = 4 %	2.5			Vp-p
		I_L = 120 mA, THD = 4 %	4.5			Vp-p
Receiving dynamic range (Single R_L = 150 Ω)	DR_{DR}	I_L = 20 mA, THD = 10%	0.3			Vp-p
		I_L = 120 mA, THD = 10%	0.5			Vp-p
Receiving dynamic range (BTL R_L = 3 kΩ)	DR_{SR}	I_L = 20 mA, THD = 10%	2			Vp-p
		I_L = 120 mA, THD = 10%	6			Vp-p
MUTE high-level input voltage	V_{IH}	I_L = 20 mA to 120 mA	0.6VSP			V
MUTE low-level input voltage	V_{IL}	I_L = 20 mA to 120 mA	0		0.4	V
Transmitting PADC attenuation	ΔG_T	I_L = 30 mA, ground at 24 kΩ		3.7		dB
Receiving PADC attenuation	ΔG_R	I_L = 30 mA, ground at 24 kΩ		6.3		dB
Internal reference voltage	V_{REF}	I_L = 20 mA		0.65		V
		I_L = 50 mA		1.0		V
		I_L = 120 mA		1.7		V

Operating Characteristics at Ta = 25°C, f = 1 kHz

Parameter	Symbol	Conditions	min	typ	max	Unit
[Audio Signal Processing Block]						
PRE AMP Input from crosspoint switch						
Voltage gain	VG_C	–45 dBV input	6	8	10	dB
Total harmonic distortion	THD	–20 dBV input		0.4	1.0	%
ALC saturation output level	V_{OS}	–20 dBV input	90	110	130	mVrms
ALC range	ALCW	From when ALC is on until THD is 1%	15			dB
Equivalent input noise voltage	V_{NI}	Input AC-shorted, 20 to 20 kHz		5.0	10	µVrms
PB AMP						
Voltage gain	VG_E	–60 dBV input	46.5	48.5	50.5	dB
Total harmonic distortion	THD	–60 dBV input		0.5	1.5	%
Equivalent input noise voltage	V_{NI}	Pin AC-shorted, 20 to 20 kHz		5.0	10	µVrms
OGM AMP						
Voltage gain	VG_G	–20 dBV input	7	9	11	dB
Total harmonic distortion	THD	–20 dBV input		0.1	1.0	%
REC AMP						
Voltage gain	VG_R	Pin 20 Z_{AC} = 8.1 kΩ, between pins 25 and 21	4	6	8	dB
Output bias voltage (Voltage at pin 21)	V_B	Pin 20 Z_{DC} = 15 kΩ, pin 21 load = 8.2 kΩ	0.8	1.0	1.2	V
Total harmonic distortion	THD			0.8	1.5	%
MIC AMP						
Voltage gain	VG_M	–40 dBV input	27	29	31	dB
Total harmonic distortion	THD	–40 dBV input		0.1	1.0	%
Equivalent input noise voltage	V_{NI}	Pin 33 AC-shorted, 20 to 20 kHz		2.0	5	µVrms
POWER AMP R_L = 8 Ω						
Voltage gain	VG_P	–30 dBV input	28	30	32	dB
Output voltage	P_O	THD = 10%	200	250		mW
Total harmonic distortion	THD	–30 dBV input		0.6	1.5	%
Input resistance	R_{IN}			15		kΩ
Ripple rejection ratio	SVRR	Rg = 0, fr = 100 Hz, Vr = –20 dBV	40			dB
Output noise voltage	V_{NO}	Pin 42 AC-shorted, 20 to 20 kHz		0.04	0.1	µVrms

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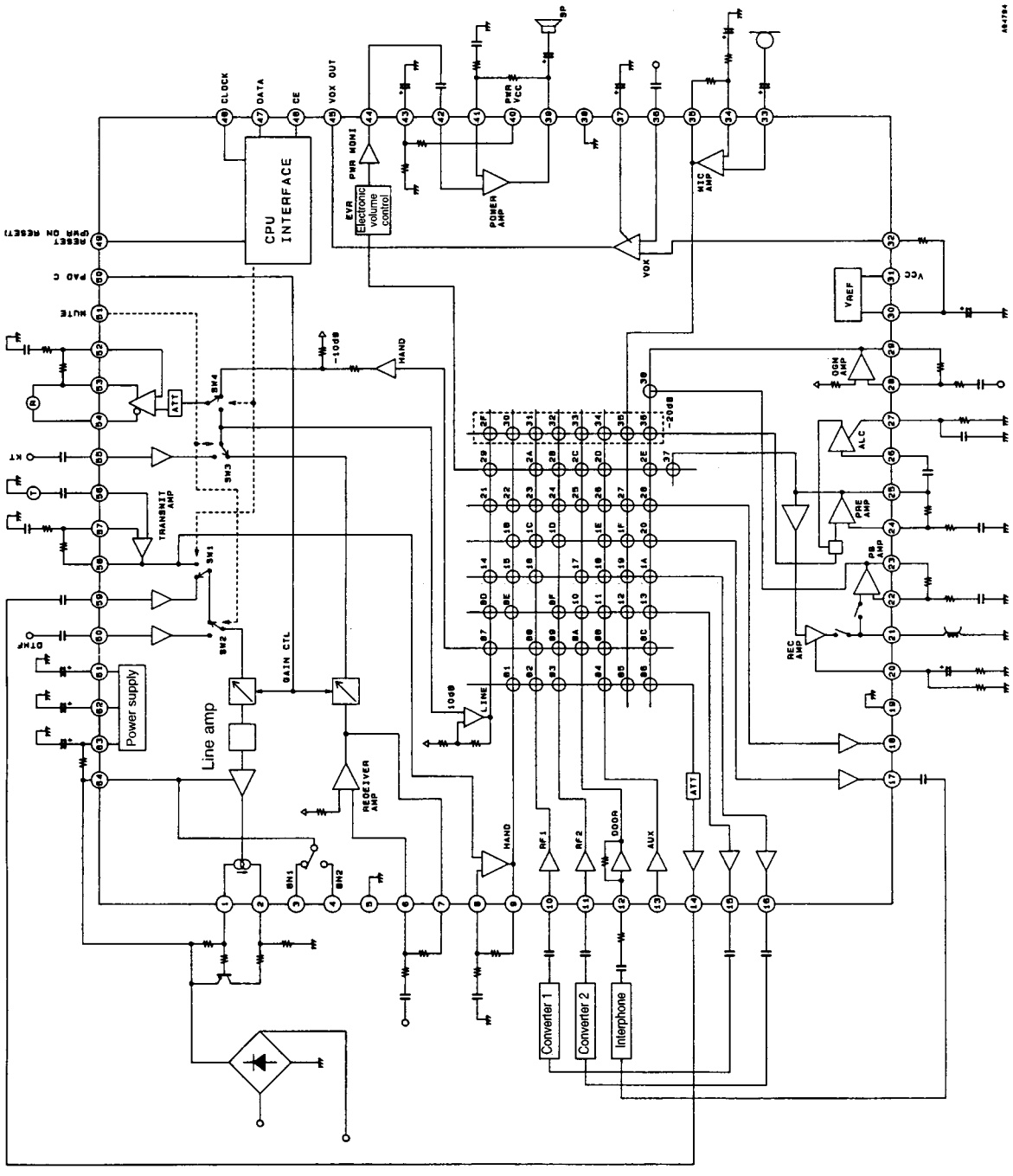
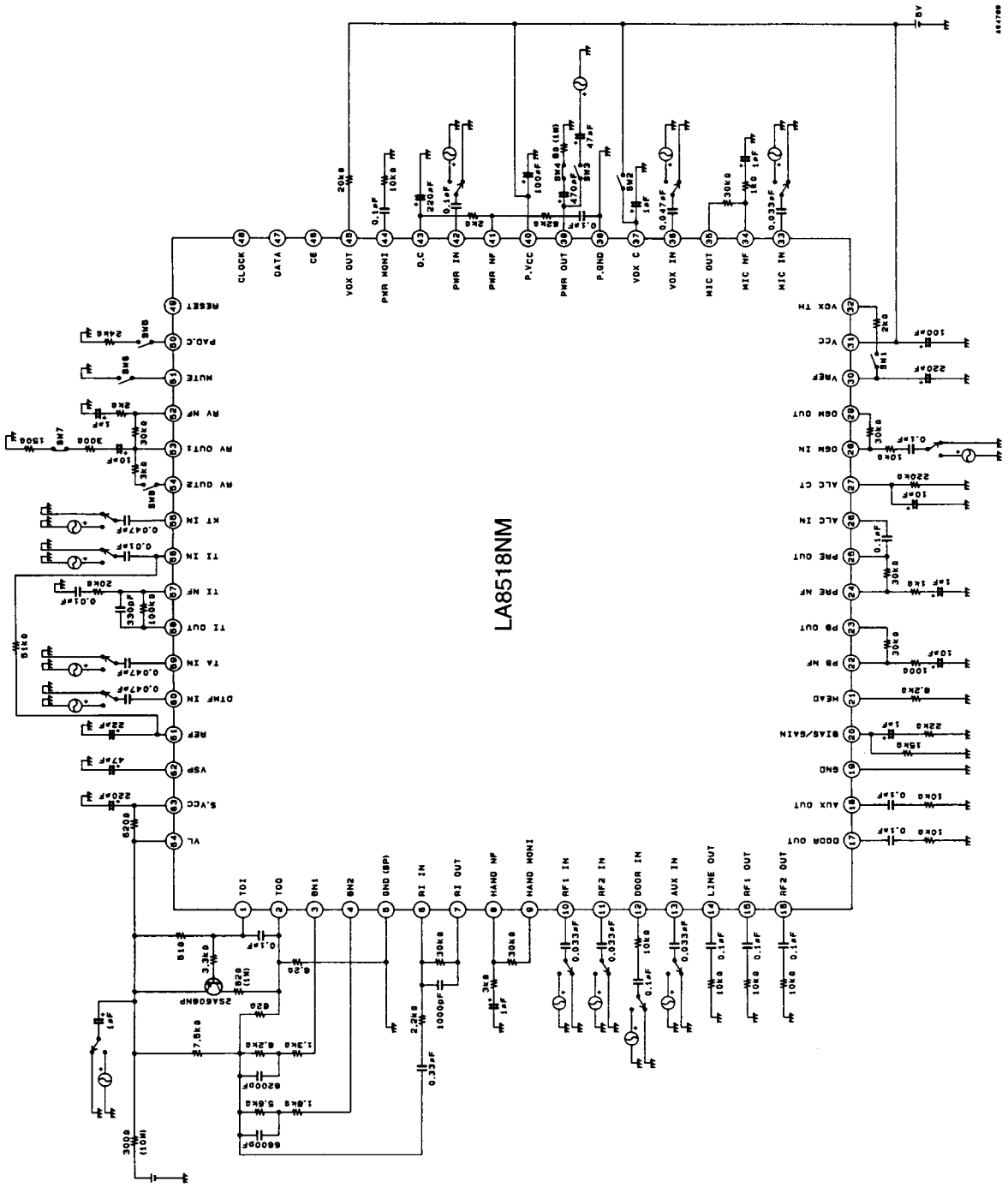
Parameter	Symbol	Conditions	min	typ	max	Unit
VOX						
Sensitivity 1	V_{OXL}	–24 dBV input			0.3	V
Sensitivity 2	V_{OXH}	–27 dBV input	4.8			V
Electronic volume control						
Step width	E_{VRW}			3.8		dB
VREF						
Output voltage	V_{REF}		2.1	2.3	2.5	V
Control						
Clock frequency	F_{CK}				500	kHz
High-level input signal	V_H		3			V
Low-level input signal	V_L				1.5	V
Power supply switch						
Pin 31 voltage 1	V_{CH1}	The voltage applied to pin 31 is effective	3.5			V
Pin 31 voltage 2	V_{CH2}	The voltage supplied from pin 64 is effective			1.2	V
Quiescent current	I_{CCO}	Power amplifier on	19	26	35	mA

Block Diagram

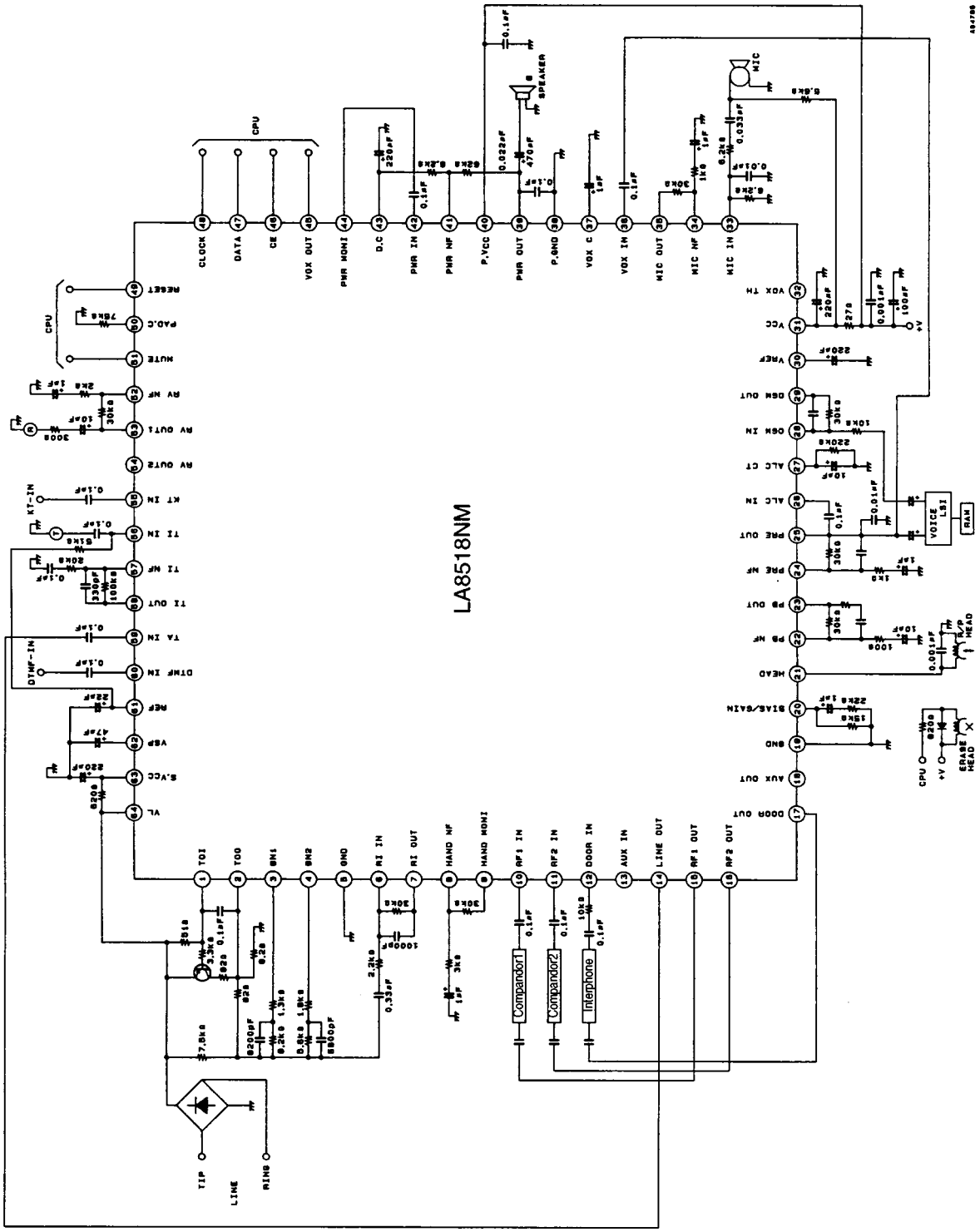
1. TOI
2. TOO
3. BN1
4. BN2
5. GND (SP)
6. RI IN
7. RI OUT
8. HAND NF
9. HAND MONI
10. RF1 IN
11. RF2 IN
12. DOOR IN
13. AUX IN
14. LINE OUT
15. RF1 OUT
16. RF2 OUT
17. DOOR OUT
18. AUX OUT
19. GND
20. BIAS/GAIN
21. HEAD
22. PB NF
23. PB OUT
24. PRE NF
25. PRE OUT
26. ALC IN
27. ALC CT
28. OGM IN
29. OGM OUT
30. V_{REF}
31. V_{CC}
32. VOX TH
33. MIC IN
34. MIC NF
35. MIC OUT
36. VOX IN
37. VOX C
38. P.GND
39. PWR OUT
40. P.V_{CC}
41. PWR NF
42. PWR IN
43. D.C
44. PWR MONI
45. VOX OUT
46. CE
47. DATA
48. CLOCK
49. RESET
50. PAD.C
51. MUTE
52. RV NF
53. RV OUT1
54. RV OUT2
55. KT IN
56. TI IN
57. TI NF
58. TI OUT
59. TA IN
60. DTMF IN
61. REF
62. VSP
63. S.V_{CC}
64. V_L



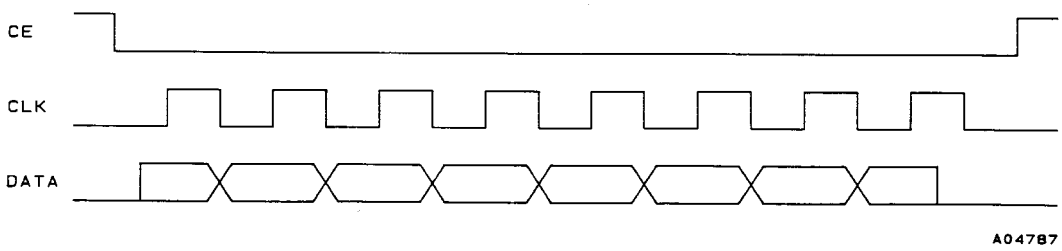
Test Circuit Diagram



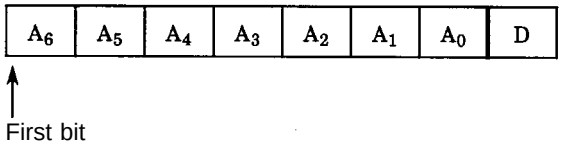
Sample Application Circuit



— Serial control data format —

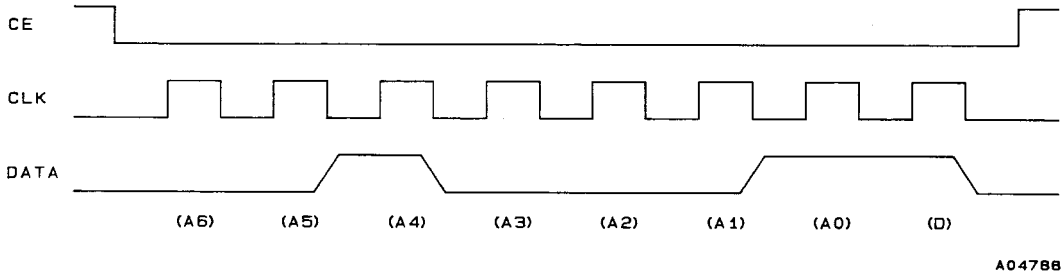


• Serial data content



A0 to A6 → Specify the address of a crosspoint switch and a control switch.
D → Turns the crosspoint switch on and off and controls the control switch.
(When D = 1, the switch is on; when D = 0, the switch is off.)

• Example: Turning address 11 (AUX input, RF1 output) on



The address table is shown on the following page:

Note 1: Because there is a power-on reset function, all crosspoint switches and control switches are reset when the external power supply (V_{CC} at pin 31) is turned on.
Note 2: SW2 and SW3 in the block diagram are controlled by the MUTE pin (pin 51); the signals that are enabled are shown below.

MUTE pin	SW2	SW3
H	Transmitting (Pin 58) TAIN (Pin 59)	Receiving (Pin 7)
L	DTMF (Pin 60)	KT (Pin 55)

— Address chart —

		Input								
		LINE	HAND	RF1	RF2	DOOR	AUX	MIC	OGM	PRE
Output	LINE	—	01	02	03	—	04	05	06	—
	HAND	07	—	08	09	0A	0B	—	0C	—
	RF1	0D	0E	—	0F	10	11	12	13	—
	RF2	14	15	16	—	17	18	19	1A	—
	DOOR	—	1B	1C	1D	—	1E	1F	20	—
	AUX	21	22	23	24	25	26	27	28	—
	PWR	29	—	2A	2B	2C	2D	—	2E	37
	PRE	2F	30	31	32	33	34	35	36	—

Other Control Switches

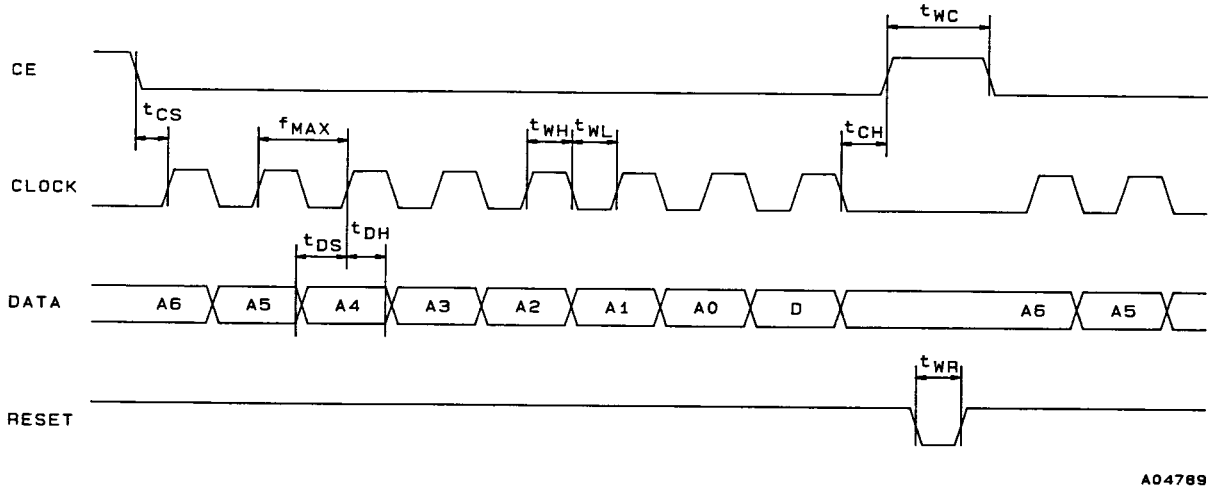
00 All crosspoint switches and control switches off *2
38 Mixing switch for PB amplifier-OGM amplifier on
39 Transmitting/receiving CTL (SW1 and SW2 in the block diagram) *1
3A Receiver amplifier ATT Set to 0 dB
3B Line amplifier ATT Set to –6 dB
3C ALC on
3D PB amplifier on
3E REC amplifier on
3F Power amplifier on
40 Electronic volume control 0 dB
41 Electronic volume control –4dB
42 Electronic volume control –8dB
43 Electronic volume control –12dB
44 Electronic volume control –16dB
45 Electronic volume control –20dB
46 Electronic volume control –24dB
47 Electronic volume control –28dB

*2

*1: When address 39 is on, SW1 enables the transmitting amplifier output (pin 58) signal, and SW4 enables the receiving amplifier output (pin 7) or KT (pin 55) signal. If voltage is not supplied to pin 31 (V_{CC}) (power is off), the status of SW1 and SW4 is the same as address 39 is in on state.
*2: When setting address 00 and 40 to 47, ‘‘D’’ data may be either ‘‘0’’ or ‘‘1’’.

Note 1: The receiver amplifier ATT is set to −6 dB when power is first applied, when a reset is performed, and when all of the switches are off.
Note 2: The line amplifier ATT is set to 0 dB when power is first applied, when a reset is performed, and when all of the switches are off.
Note 3: The electronic volume control is set to 0 dB when power is first applied, when a reset is performed, and when all of the switches are off.
Note 4: The addresses are given in hexadecimal notation.

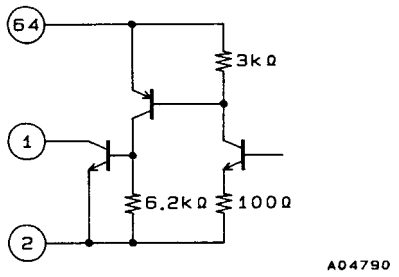
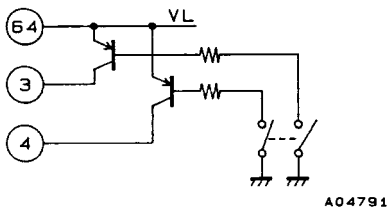
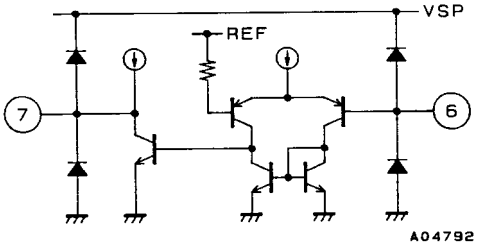
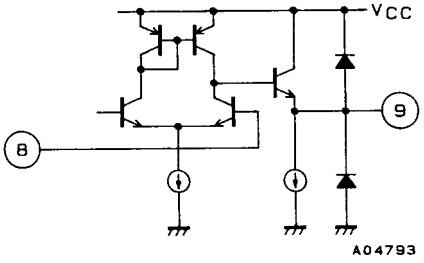
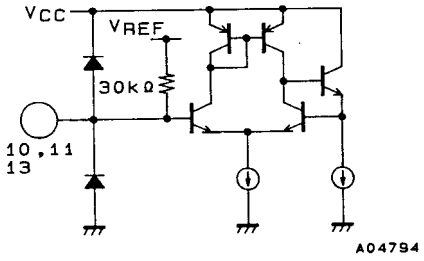
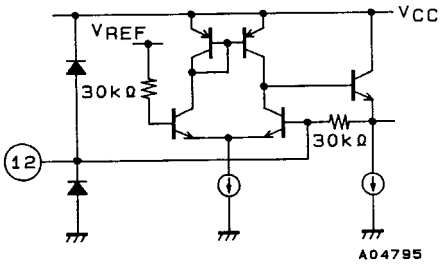
Input Port Timing



• f_{MAX}	(Maximum clock frequency)	500 kHz
• f_{WL}	(Clock pulse width "L")	1µs or longer
• f_{WH}	(Clock pulse width "H")	1µs or longer
• t_{CS}	(Chip enable setup time)	1µs or longer
• t_{CH}	(Chip enable hold time)	1µs or longer
• t_{DS}	(Data setup time)	1µs or longer
• t_{DH}	(Data hold time)	1µs or longer
• t_{WC}	(Chip enable pulse width)	1µs or longer
• t_{WR}	(Reset pulse width)	1µs or longer

Note: The control data must input 400 ms or longer after the supply voltage is applied to V_{CC} (pin 31).

Pin Functions

Pin No.	Pin Name	Internal Equivalent Circuit	Pin Function
64 1 2	V_L T_{OI} T_{OO}		• Line current input pin, line voltage pin. • Transmitting output current input pin. • Transmitting output current output pin.
3 4	BN1 BN2		• BN switch pin 1. • BN switch pin 2. Connect when there are two balancing network circuits. Open when not used.
5	GND (SP)		• Speech network system GND pin.
6 7	RI IN RI OUT		• Receiving input amplifier – input pin. • Receiving input amplifier output pin.
8 9	HAND NF HAND MONI		• Handset amplifier – input pin. • Handset amplifier output pin.
10 11 13	RF1 IN RF2 IN AUX IN		• Compander 1 input pin. • Compander 2 input pin. • Unused input pin.
12	DOOR IN		• Amplifier input pin for interphone. Because there is a feedback resistor (30 kΩ) on chip, the input is passed through an external resistor.

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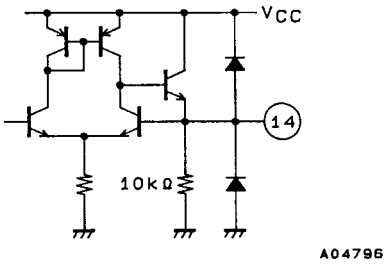
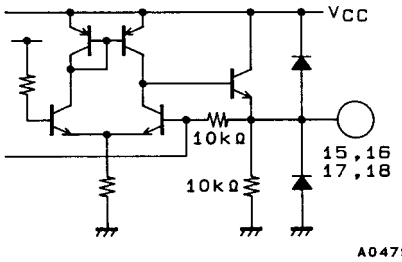
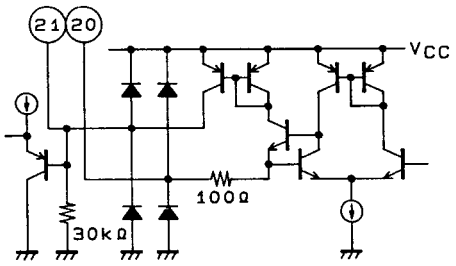
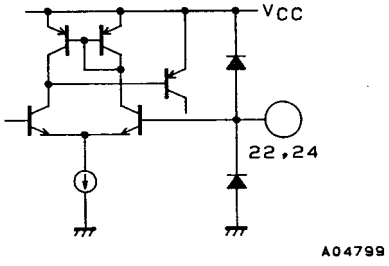
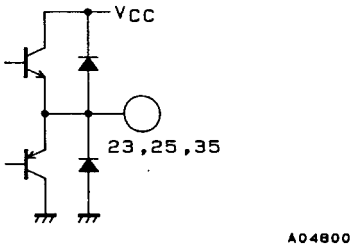
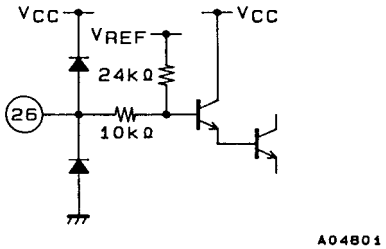
Pin No.	Pin Name	Internal Equivalent Circuit	Pin Function
14	LINE OUT		• Line output pin.
15 16 17 18	RF1 OUT RE2 OUT DOOR OUT AUX OUT		• Compander 1 input pin. • Compander 2 input pin. • Interphone output pin. • Auxiliary output pin.
19	GND		• Signal processing system GND.
20 21	BIAS/GAIN HEAD		• Bias pin. The REC amplifier gain and the REC bias gain can be controlled by an external resistor. • REC amplifier output pin and PB amplifier + input pin.
22 24	PB NF PRE NF		• PB amplifier − input pin. • PRE amplifier − input pin.
23 25 35	PB OUT PRE OUT MIC OUT		• PB amplifier output pin. • PRE amplifier output pin. • MIC amplifier output pin
26	ALC IN		• ALC input pin. Input from the PRE output (pin 25) via a coupling capacitor. In addition, the ALC level can be adjusted by connecting resistors in series.

Continued on next page.

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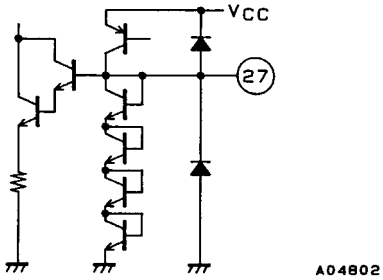
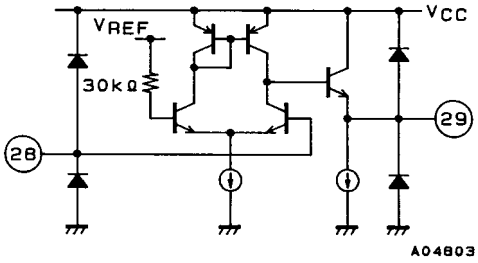
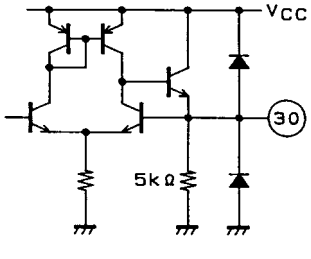
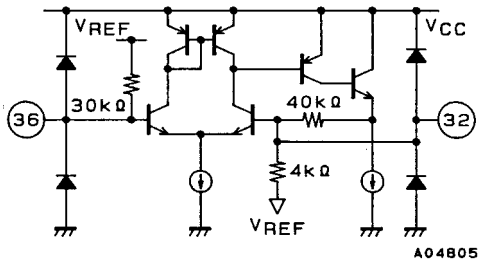
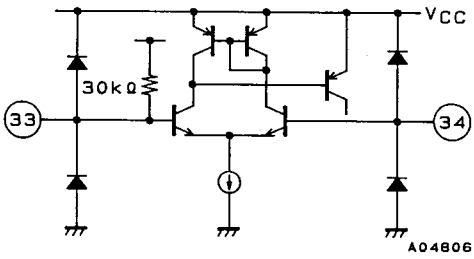
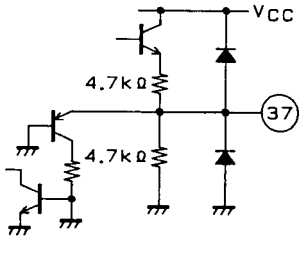
Pin No.	Pin Name	Internal Equivalent Circuit	Pin Function
27	ALC CT		• ALC time constant adjustment pin. Adjusts the ALC attack time and recovery time.
28 29	OGM IN OGM OUT		• OGM amplifier − input pin. • OGM amplifier output pin.
30	VREF		• Internal reference voltage output pin (approx. 2.3 V).
31	V_{CC}		• External power supply input pin. Supplies power to the signal processing system and to V_{SP} (pin 62).
32 36	VOX TH VOX IN		• VOX sensitivity adjustment pin. The VOX sensitivity can be adjusted by connecting this pin to pin 30 (V_{REF}) through a resistor. • VOX + input pin.
33 34	MIC IN MIC NF		• MIC amplifier + input pin. • MIC amplifier − input pin.
37	VOX.C		• VOX detection pin. Can also be used as a waveform shaper by forcing this pin high.

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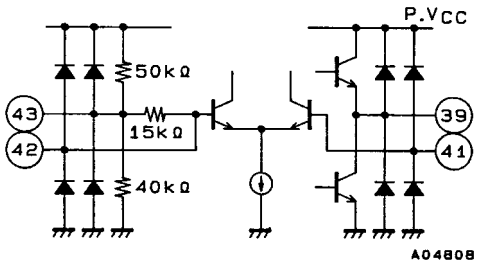
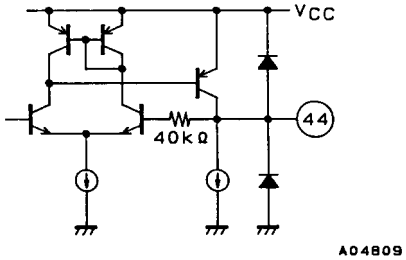
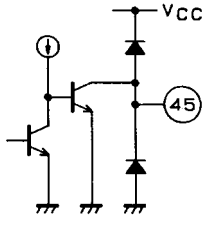
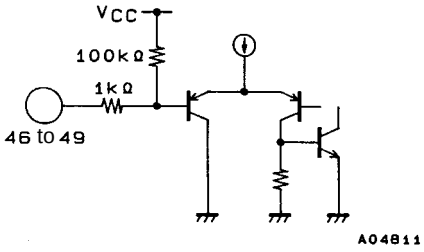
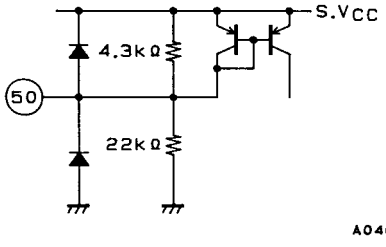
Pin No.	Pin Name	Internal Equivalent Circuit	Pin Function
38	P. GND		• Power system GND pin.
40	P. V_{CC}		• Power system power supply pin.
39 41 42 43	PWR OUT PWR NF PWR IN D.C		• Power amplifier output pin. Goes to high impedance when MUTE is on. • Power amplifier − input pin. • Power amplifier + input pin. • Power amplifier reference voltage pin (approximately 4/9 × P. V_{CC}).
44	PWR MONI		• Output pin for power amplifier.
45	VOX OUT		• VOX output pin. Open collector output.
46 47 48 49	CE DATA CLOCK RESET		• Chip enable input pin. • Data input pin. • Clock input pin. • Reset pin. Power-on reset.
50	PADC		• Pad control pin. By connecting this pin to GND or to S. V_{CC} (pin 63) through a resistor, it is possible to use the line current for gain control and to control the operating current for BN switching.

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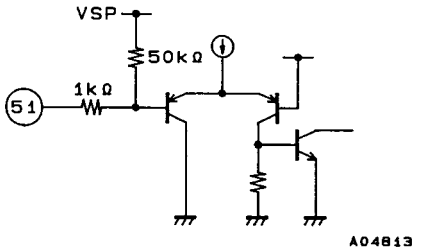
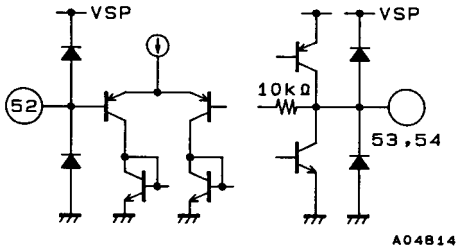
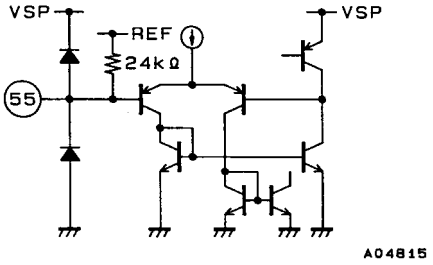
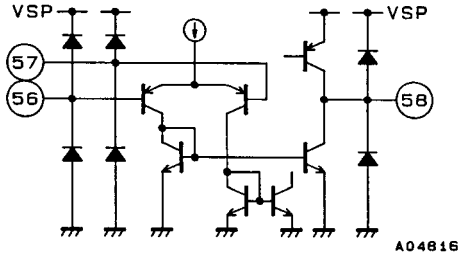
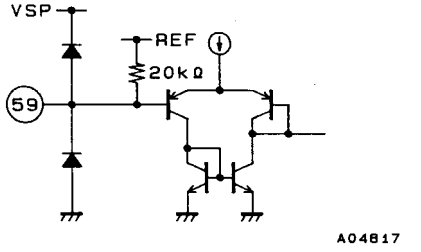
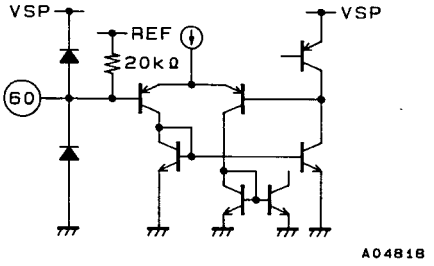
Pin No.	Pin Name	Internal Equivalent Circuit	Pin Function
51	MUTE		• Mute pin. Switches the transmitting signal and the DTMF signal in the transmitting system, and the receiving signal and the KT signal in the receiving system (SW2 and SW3 in the block diagram). When low, the DTMF and KT signals are valid.
52 53 54	RV NF RV OUT1 RV OUT2		• Receiver amplifier − input pin. • Receiver amplifier 1 output pin. • Receiver amplifier 2 output pin.
55	KT IN		• Key tone input pin.
56 57 58	TI IN TI NF TI OUT		• Transmission input amplifier + input. Because bias voltage is not applied internally, connect signal from REF (pin 61) via a resistor. • Transmission input amplifier − input pin. • Transmission input amplifier output pin.
59	TA IN		• Input pin for LINE output pin.
60	DTMF IN		• Input for DTMF input pin.

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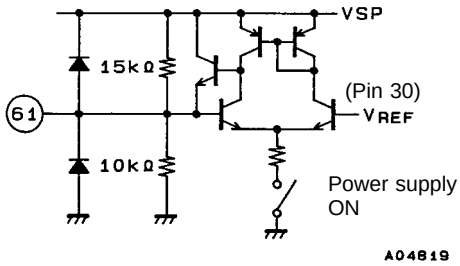
Pin No.	Pin Name	Internal Equivalent Circuit	Pin Function
61	REF		• Speech network system internal reference voltage output. When the V_{CC} (pin 31) voltage is 3.5 V or more, V_{REF} (pin 30) is output. When the V_{CC} voltage is 1.2 V or less, voltage of approximately (2/5) × V_{SP} is output.
62	V_{SP}		• Speech network system internal power supply. When the V_{CC} (pin 31) voltage is 3.5 V or more, (V_{CC} applied voltage or thereabout − 0.3 V) is output. When the V_{CC} voltage is 1.2 V or less, (S. V_{CC} (pin 63) or thereabout − 0.3 V) is output.
63	S. V_{CC}		• Speech network system power supply. When the V_{CC} (pin 31) voltage is 1.2 V or less, voltage is supplied to V_{SP} (pin 62) from the line voltage.

Usage Explanations

- Speech network

  • External Transistors

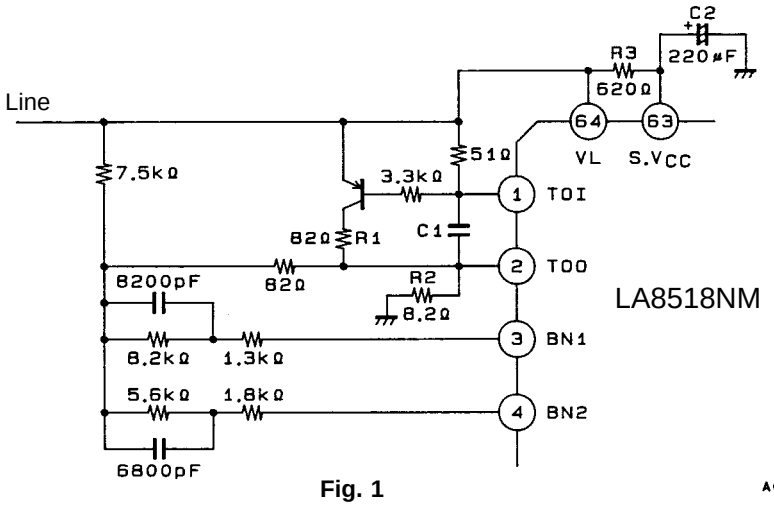


Fig. 1

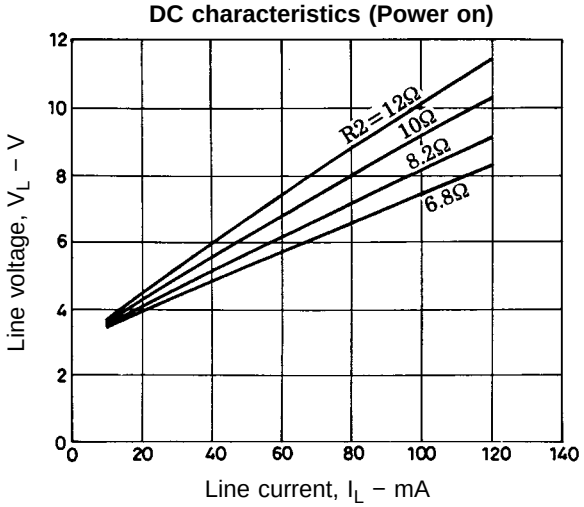
Because the IC has a built-in power amplifier, for reasons concerning allowable power dissipation, connect a transistor for heat dissipation purposes as shown in Fig. 1 so that the line current is consumed externally from the IC. In addition, when establishing the allowable power for R1 and R2, take into consideration the maximum line current that can be expected.
* When oscillation is generated due to the load state between V_L-GND, insert C1 (about 0.1μF).

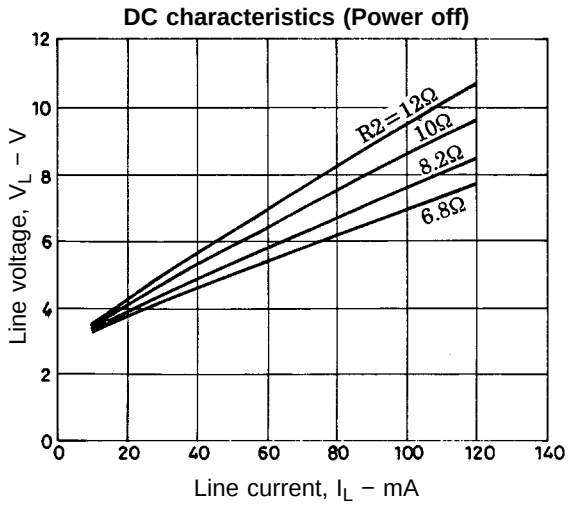
- DC resistance conversion method

  By varying R2 in Fig. 1, it is possible to change the DC resistance. (Refer to the graphs below.)
  * Note that varying R2 will also change the transmitting system gain and the balancing network conditions.

- AC impedance setting method

  The AC impedance is basically determined by R3 (620 Ω) and C2 (220 μF) in Fig. 1. Because AC loads other than the speech network will be placed on the line, adjust the AC impedance in conjunction with the speech network impedance.
  * Note that varying R3 changes the DC resistance.





• Balancing Network

It is possible to switch the Balancing Network between two systems, one for the near end and one for the far end, in accordance with the line current. (Refer to Fig. 1 for the connection method.) In addition, the switching point can be varied by connecting the PADC pin (pin 50) to GND or to S. V_{CC} (pin 63) via a resistor.
(When using only one Balancing Network, refer to Fig. 2.)

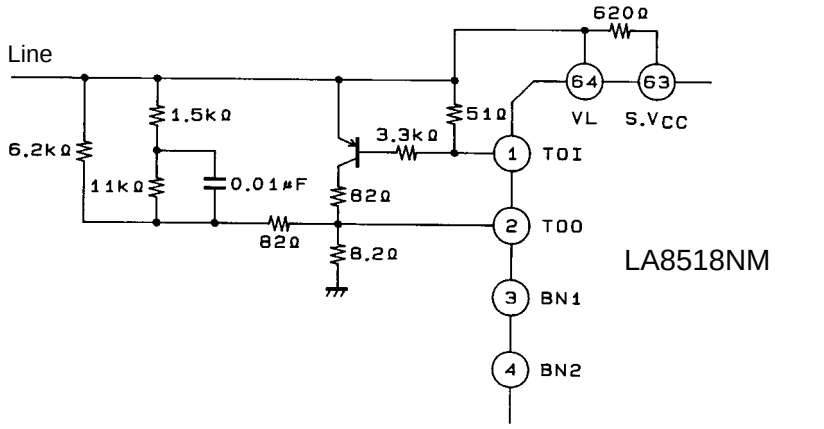
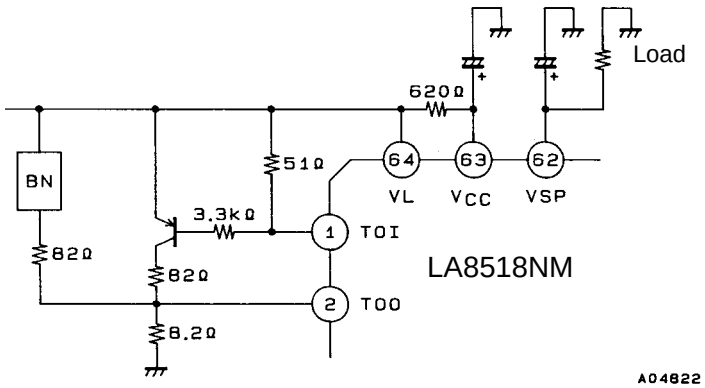


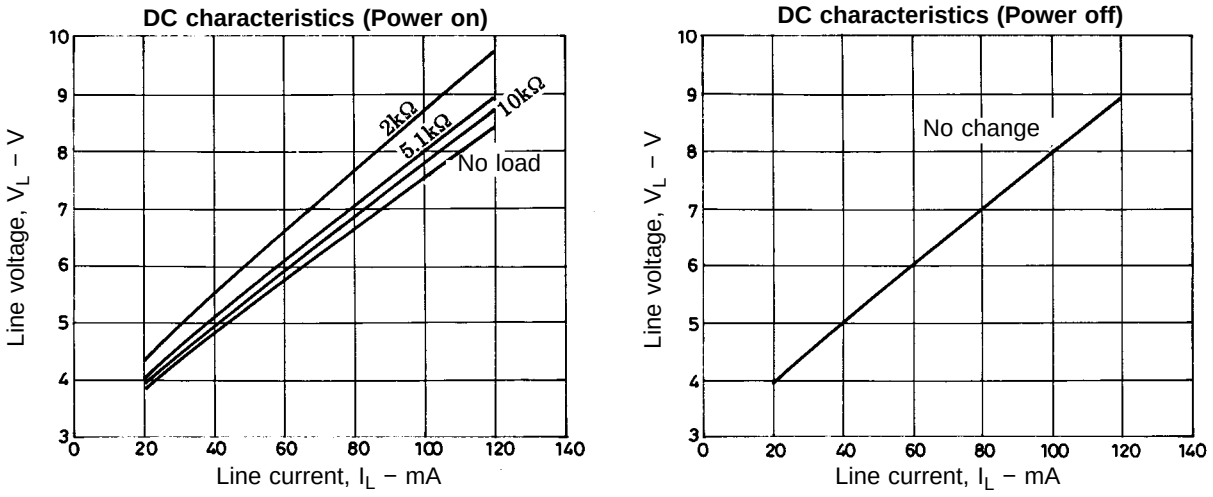
Fig. 2

Note) The constant of Balancing Network is a reference value.

• The DC characteristics when the power is off

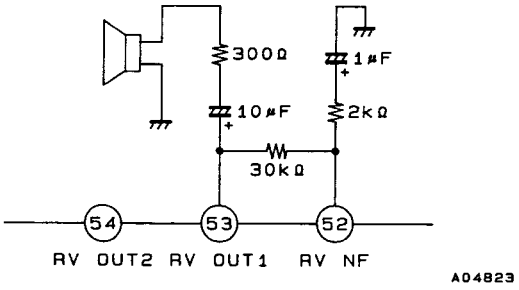


By connecting a load to V_{SP} (pin 62), it is possible to change the DC characteristics without changing the DC characteristics only when the power is off. (Refer to the diagram below.)

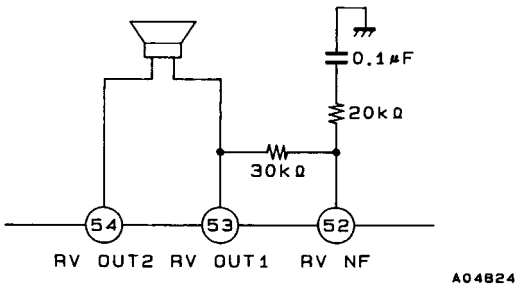


• Receiver Amplifier Application Circuit

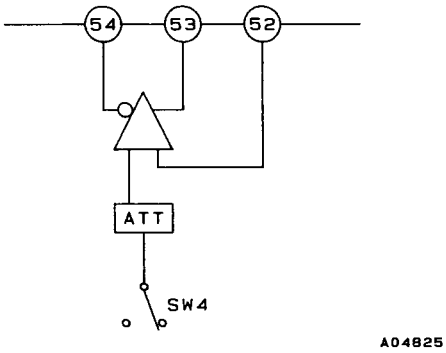
① When using the dynamic receiver



② When using the ceramic receiver

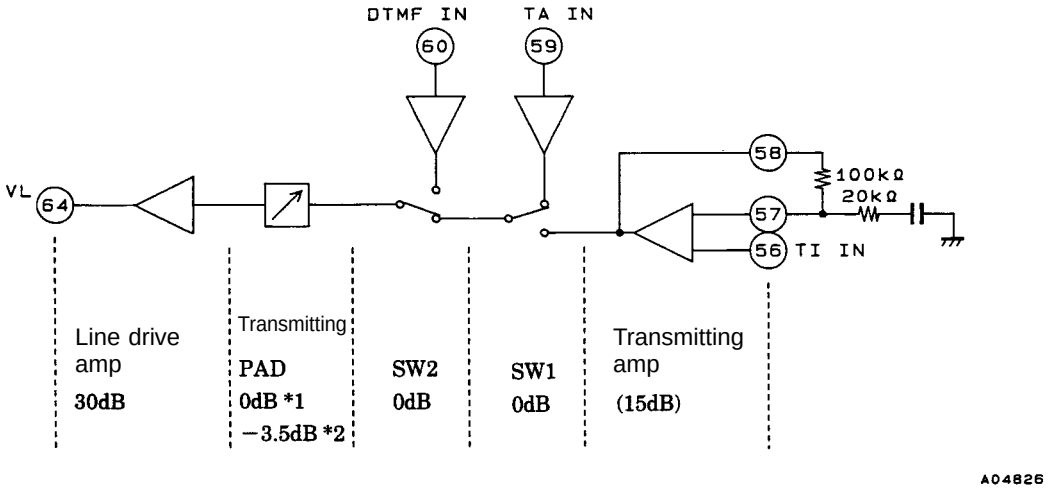


• The Receiver Amplifier Attenuator



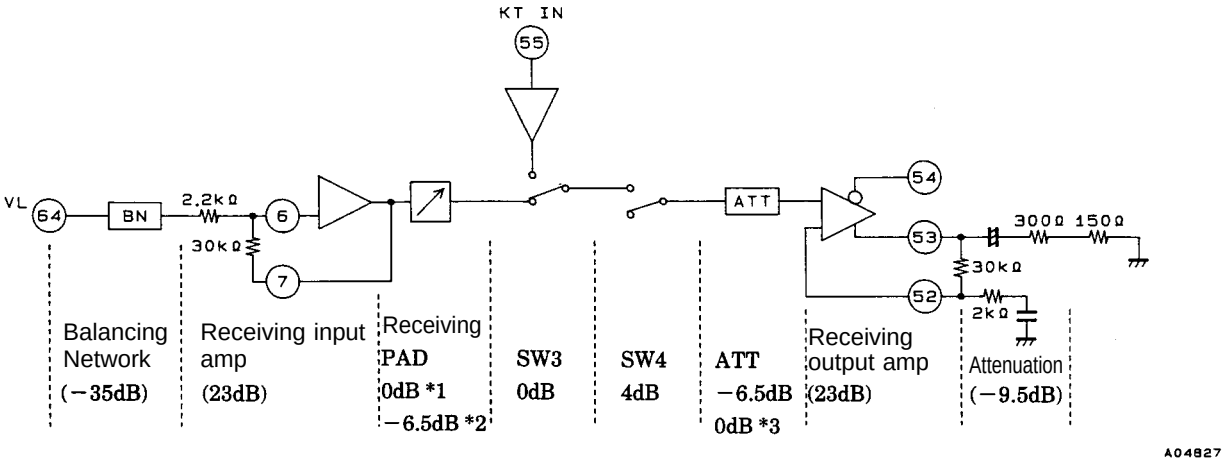
Normally, the attenuator is set to −6 dB. It is set to 0 dB when serial data 3A is on.

• Gain Distribution



*1 I_L = 20 mA
*2 I_L = 120 mA

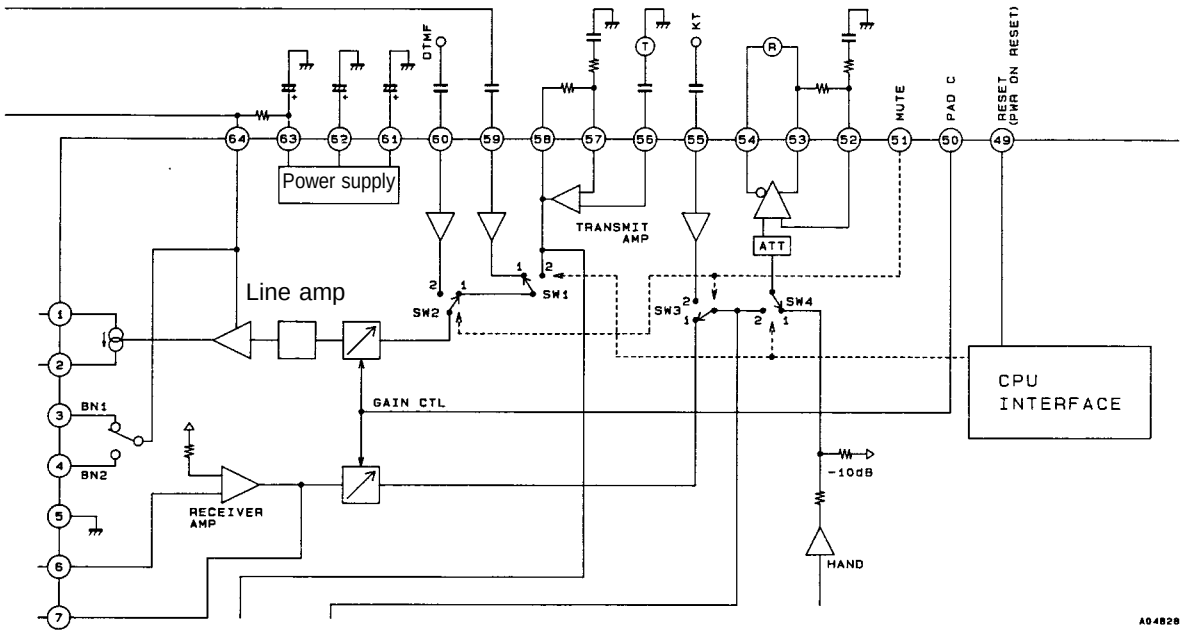
Note 1) Terminal of line 600 Ω



*1 I_L = 20 mA
*2 I_L = 120 mA
*3 When serial data 3A is turned on.

Note 2) The gain values are approximate values.
Note 3) The values shown in parentheses can be varied externally.

Speech Network Block Switch Operation



SW2 and SW3 are controlled by pin 51 (MUTE), while SW1 and SW4 are controlled by the serial data (address 39). (SW2 and SW3, and SW1 and SW4 are coupled to each other.)

SW1, SW4 operation

Condition	SW1	SW4
Power on (Initial state)	1	1
Address 39 on	2	2
Power off	2	2

* When the power is off, SW1 and SW2 are fixed at ‘‘2’’ and cannot be switched.

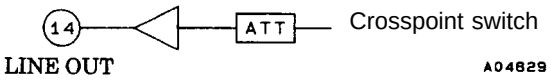
SW2, SW3 operation

Pin 51 (MUTE)	SW2	SW3
High	1	1
Low	2	2

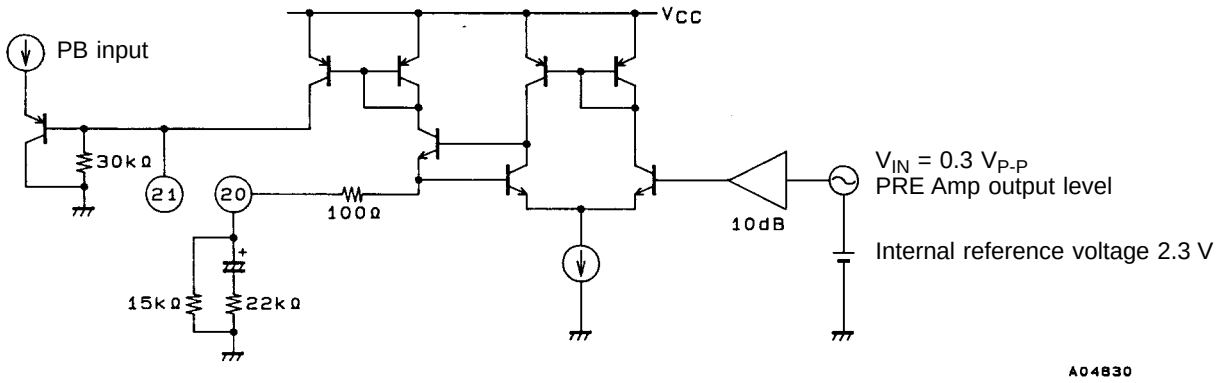
* SW2 and SW3 operate as shown in the table at left, regardless of whether the power is on or off.

• LINE amplifier attenuator

Normally, the attenuator is set to 0 dB. It is set to −6 dB when serial data 3 dB is on.



• REC amplifier V/I conversion

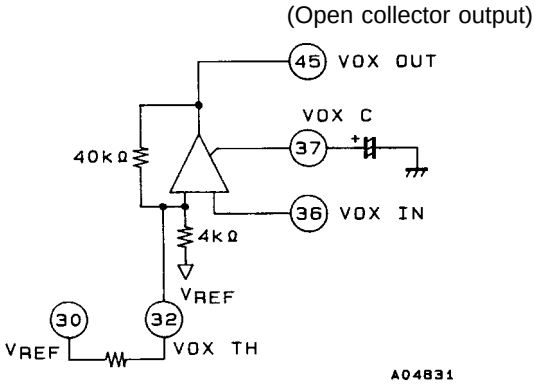


In order to derive the recording current for the DC bias, this circuit performs V/I conversion. The conversion gain and the bias current can be controlled by the external resistor connected to pin 20. Current equal to the current output from pin 20 is output from pin 22.

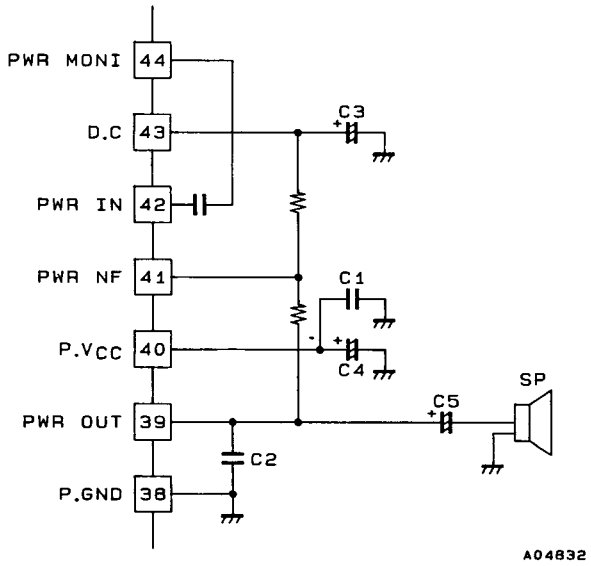
DC bias current = 2.3 V/(100 Ω + 15 kΩ) ≒ 150 µA

Signal current = 1.0 Vp-p/(100 Ω + 15 kΩ//22 kΩ) ≒ 110 µAp-p

• VOX
  ① The VOX circuit determines whether or not conversation is taking place. If the VOX input (pin 36) signal is −24dB or higher, the VOX output (pin 45) goes low. The output level is adjusted by inserting a resistor between VOX TH (pin 32) and V_{REF} (pin 30).
  ② Because the circuit can be used as a waveform shaper by connecting VOX C (pin 37) to V_{CC} (setting pin 37 high), a 400 Hz beep tone can be detected.



• Power amplifier application



C1 : 0.1 µF
C2 : 0.1 µF
C3 : 220 µF
C4 : 220 µF
C5 : 100 to 470 µF
SP : 8 to 16 Ω

- Voltage gain: 20 to 30 dB
- No capacitor for frequency characteristics adjustment connected to the feedback resistor.

* The phase compensation capacitor C2 should be located near the IC.

* When muting (address 3F ‘‘off’’), the impedance of the power amplifier output (pin 39) is high.

• Serial control mode example
Below are the basic modes.

Mode	Serial Data								Address	Remarks
	A6	A5	A4	A3	A2	A1	A0	D0		
ICM REC	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	1	1	1	1	37	Input PRE, output PWR
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	0	1	3E	REC ON
	0	1	1	1	1	1	1	1	3F	PWR ON
2 WAY REC (Base set)	0	0	0	0	0	0	1	1	01	Input HAND, output LINE
	0	0	0	0	1	1	1	1	07	Input LINE, output HAND
	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	0	0	0	1	30	Input HAND, output PRE
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	0	1	3E	REC ON
(Handset)	0	0	0	0	0	1	0	1	02	Input RF1, output LINE
	0	0	0	1	1	0	1	1	0D	Input LINE, output RF1
	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	0	0	1	1	31	Input RF1, output PRE
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	0	1	3E	REC ON
DECT REC	0	1	1	0	1	0	1	1	35	Input MIC, output PRE
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	0	1	3E	REC ON
2 WAY BEEP (Base set)	0	0	0	0	0	0	1	1	01	Input HAND, output LINE
	0	0	0	0	1	1	1	1	07	Input LINE, output HAND
	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	0	0	0	1	30	Input HAND, output PRE
	0	0	0	0	1	1	0	1	06	Input OGM, output LINE
	0	1	0	1	1	1	0	1	2E	Input OGM, output PWR
	0	1	1	1	0	1	1	1	3B	LINE −6dB
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	0	1	3E	REC ON
	0	1	1	1	1	1	1	1	3F	PWR ON
(Handset)	0	0	0	0	0	1	0	1	02	Input RF1, output LINE
	0	0	0	1	1	0	1	1	0D	Input LINE, output RF1
	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	0	0	1	1	31	Input RF1, output PRE
	0	0	0	0	1	1	0	1	06	Input OGM, output LINE
	0	1	0	1	1	1	0	1	2E	Input OGM, output PWR
	0	1	1	1	0	1	1	1	3B	LINE −6dB
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	0	1	3E	REC ON
ICM OUT	0	0	0	0	1	1	0	1	06	Input OGM, output LINE
	0	1	0	1	1	1	0	1	2E	Input OGM, output PWR
	0	1	1	1	0	0	0	1	38	Mix OGM and PB
	0	1	1	1	1	0	1	1	3D	PB ON
	0	1	1	1	1	1	1	1	3F	PWR ON

Mode	Serial Data								Address	Remarks
	A6	A5	A4	A3	A2	A1	A0	D0		
ICM PLAY (Base set)	0	1	0	1	1	1	0	1	2E	Input OGM, output PWR
	0	1	1	1	0	0	0	1	38	Mix OGM and PB
	0	1	1	1	1	0	1	1	3D	PB ON
	0	1	1	1	1	1	1	1	3F	PWR ON
(Handset)	0	0	1	0	0	1	1	1	13	Input OGM, output RF1
	0	1	1	1	0	0	0	1	38	Mix OGM and PB
	0	1	1	1	1	0	1	1	3D	PB ON
OGM REC (Base set)	0	1	1	0	1	0	1	1	35	Input MIC, output PRE
	0	1	1	1	1	0	0	1	3C	ALC ON
(Handset)	0	1	1	0	0	0	1	1	31	Input RF1, output PRE
	0	1	1	1	1	0	0	1	3C	ALC ON
OGM CHANGE	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	1	1	1	1	37	Input PRE, output PWR
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	1	1	3F	PWR ON
OGM OUT	0	0	0	0	1	1	0	1	06	Input OGM, output LINE
	0	1	0	1	1	1	0	1	2E	Input OGM, output PWR
	0	1	1	1	1	1	1	1	3F	PWR ON
OGM PLAY (Base set)	0	1	0	1	1	1	0	1	2E	Input OGM, output PWR
	0	1	1	1	1	1	1	1	3F	PWR ON
(Handset)	0	0	1	0	0	1	1	1	13	Input OGM, output RF1
ROOM MONI	0	0	0	0	1	0	1	1	05	Input MIC, output LINE
ROOM OUT	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	1	1	1	1	37	Input PRE, output PWR
	0	1	1	1	1	1	1	1	3F	PWR ON
VOICE SELE	0	0	0	0	1	1	0	1	06	Input OGM, output LINE
	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	0	1	1	1	1	37	Input PRE, output PWR
	0	1	1	1	1	1	1	1	3F	PWR ON
Interactive REC	0	0	0	0	1	1	0	1	06	Input OGM, output LINE
	0	1	0	1	1	1	1	1	2F	Input LINE, output PRE
	0	1	1	1	1	0	0	1	3C	ALC ON
	0	1	1	1	1	1	0	1	3E	REC ON
Extension call	0	0	0	1	0	0	0	1	08	Input RF1, output HAND
	0	0	0	1	1	1	0	1	0E	Input HAND, output RF1
Three-way call	0	0	0	0	0	0	1	1	01	Input HAND, output LINE
	0	0	0	0	0	1	0	1	02	Input RF1, output LINE
	0	0	0	0	1	1	1	1	07	Input LINE, output HAND
	0	0	0	1	0	0	0	1	08	Input RF1, output HAND
	0	0	0	1	1	0	1	1	0D	Input LINE, output RF1
	0	0	0	1	1	1	0	1	0E	Input HAND, output RF1

“1”= HIGH “0”= LOW

Usage Examples for Each Mode

1) ICM REC (In Coming Message Rec.)
- Recording incoming messages.
- Recording memos from an outside location (remote control from an outside location).

2) 2WAY REC
- Recording of both sides of conversations.
- Recording incoming messages.

3) DECT REC
- Recording memos using the microphone (recording messages to family or making simple recordings).

4) 2WAY BEEP
- An alarm sound is output from the speaker and recorded as an ICM, and is simultaneously output on the line and relayed to the other party.
- Can be indicated to the other party that recording is in progress.
- Line output is reduced by 6 dB in comparison with other modes.

5) ICM OUT
- Playing back incoming messages.
- Listening to incoming messages from an outside phone.
- Transferring incoming messages.
- Playing back the memo recording.

6) ICM PLAY
- Playing back incoming messages.
- Playing back the memo recording.

7) OGM REC (Outgoing Message rec.)
- Recording the answering message in the IC.

8) OGM CHANGE
- Changing the answering message by remote control from an outside phone.

9) OGM OUT
- Playing back the answering message.
- Transmitting the answering message (by remote control, etc.).

10) OGM PLAY
- Playing back and checking the answering message.

11) ROOM MONI
- Listening to the microphone input by remote control from an outside telephone.

12) ROOM OUT
- Outputting messages, etc., over the speaker by remote control from an outside telephone.

13) VOICE SELE
- Outputting the other party’s voice over the speaker when transmitting the response message.

14) Interactive recording
- Recording an incoming message while transmitting the answering message.

IC Usage Notes

1) Printed circuit board
When creating a printed circuit board, make the GND lines for pins 19 and 38 thick and short. Common impedance could result in a worsening of distortion.

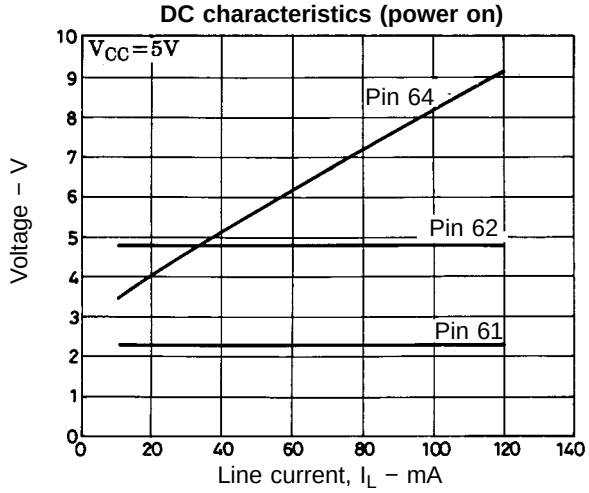
2) When used nearly at the maximum ratings, even a slight fluctuation in conditions could result in the maximum ratings being exceeded, which may result in damage to the IC. Therefore, allow for an adequate safety margin in regards to the power supply voltage, etc., and use the IC only within ranges that will not exceed the maximum ratings under any circumstances.

3) Short circuits between pins
Turning on the power while there is a short circuit between pins is a cause of IC damage and deterioration. Therefore, when mounting the IC on a board, make sure that the pins are not short-circuited by solder, etc., before applying power.

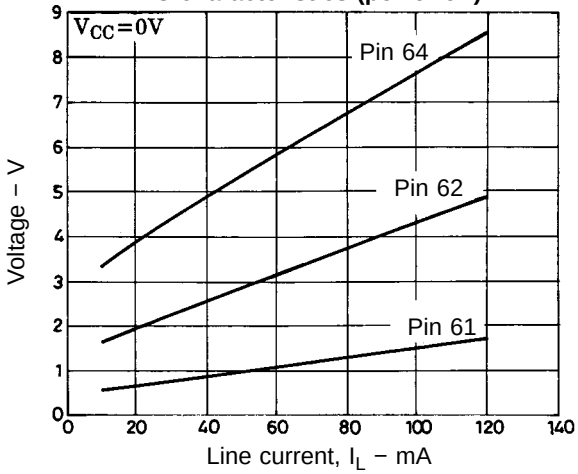
4) Load short circuit
Leaving a load in a short-circuited state for an extended period of time is a cause of IC damage and deterioration. Therefore, do not short-circuit the load at any time.

5) Power amplifier
A phase compensation capacitor must be connected between pin 39 (PWR OUT) and pin 38 (P. GND) and positioned near the IC.

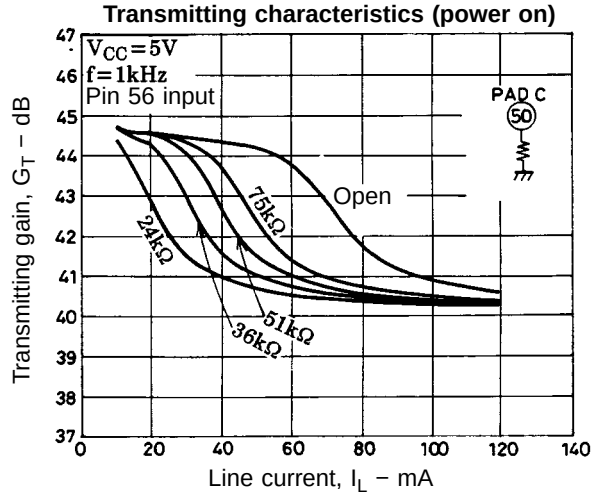
DC characteristics (power on)



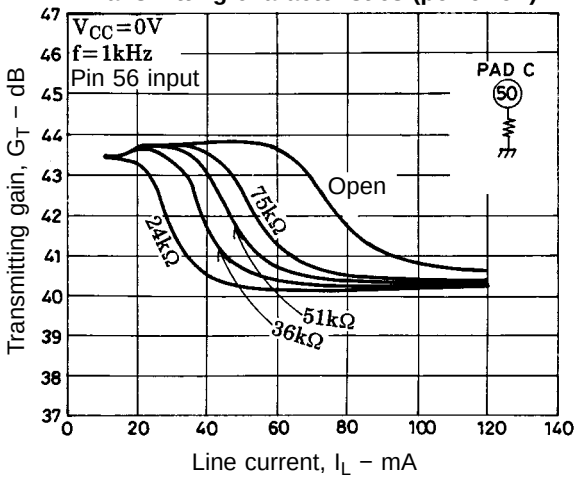
DC characteristics (power off)



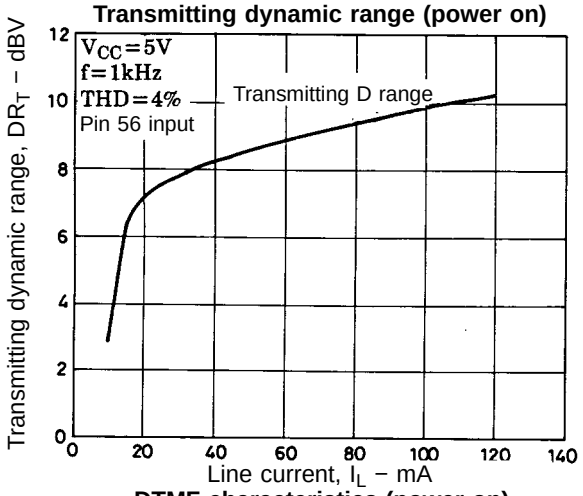
Transmitting characteristics (power on)



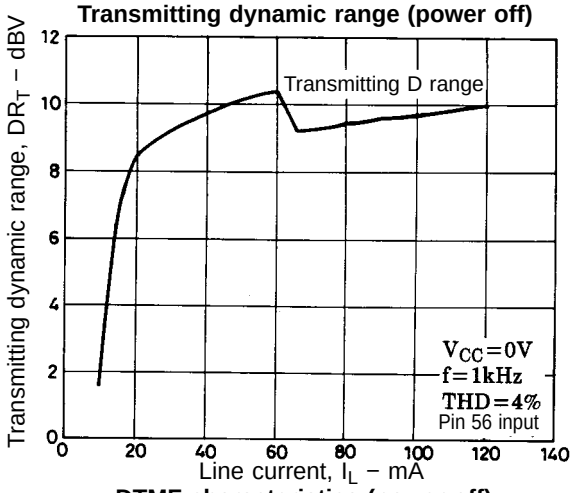
Transmitting characteristics (power off)



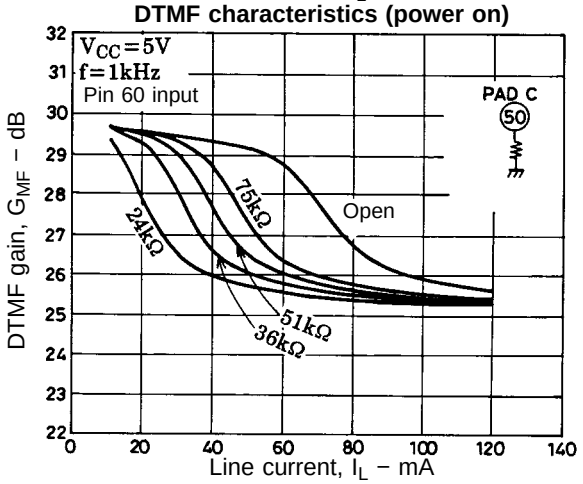
Transmitting dynamic range (power on)



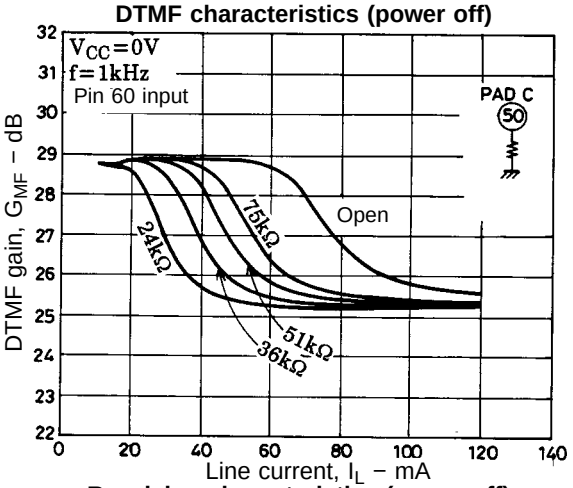
Transmitting dynamic range (power off)



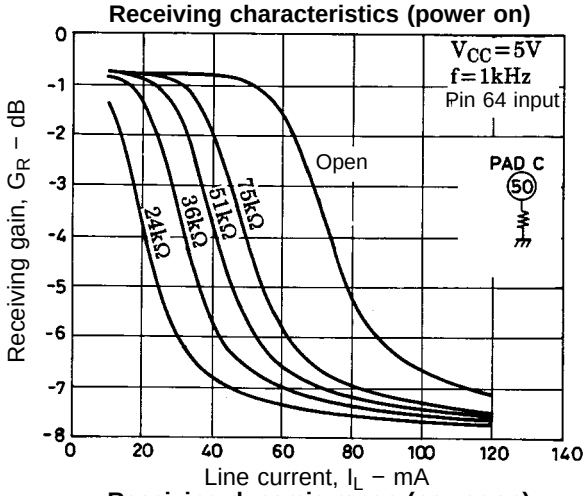
DTMF characteristics (power on)



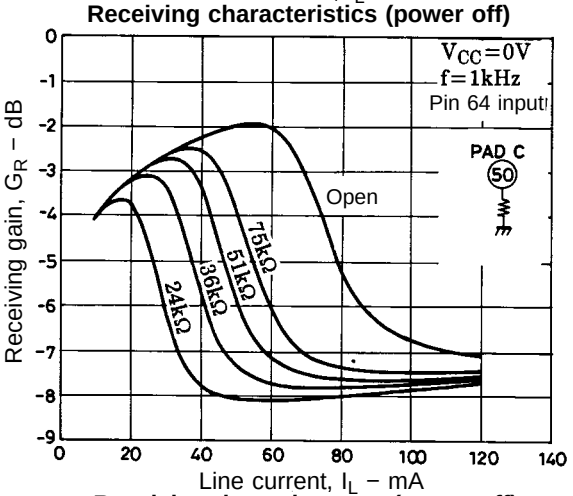
DTMF characteristics (power off)



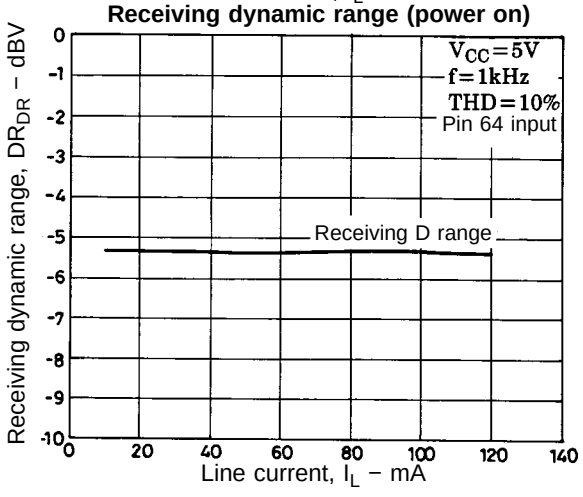
Receiving characteristics (power on)



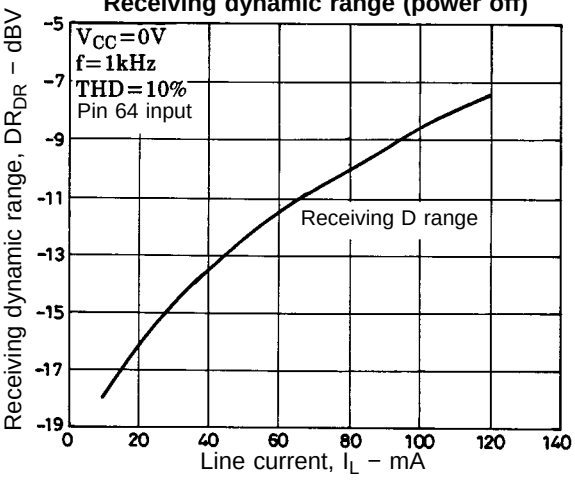
Receiving characteristics (power off)



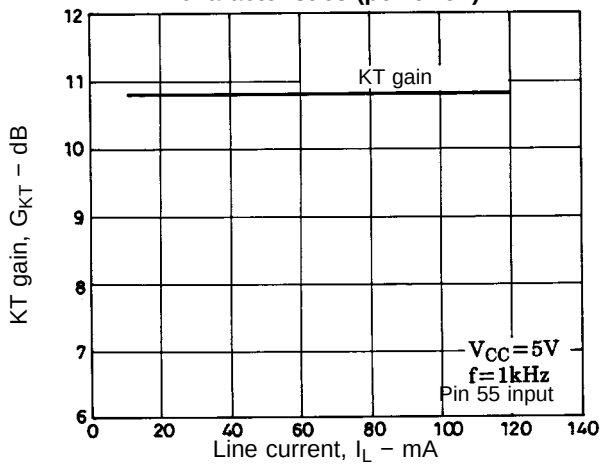
Receiving dynamic range (power on)



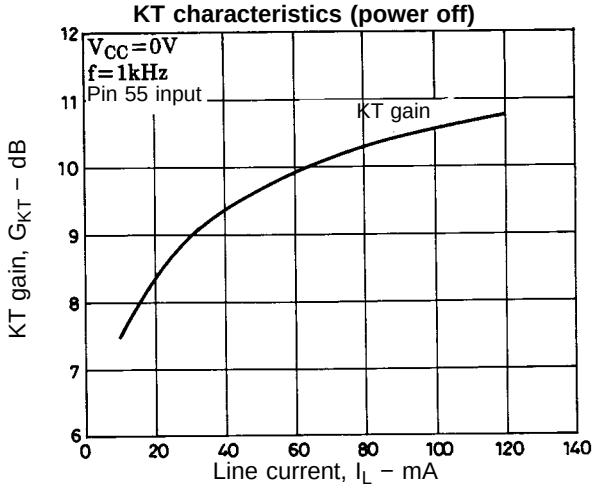
Receiving dynamic range (power off)



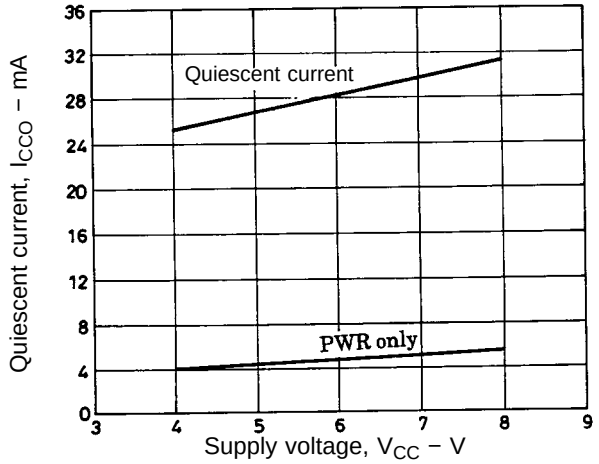
KT characteristics (power on)



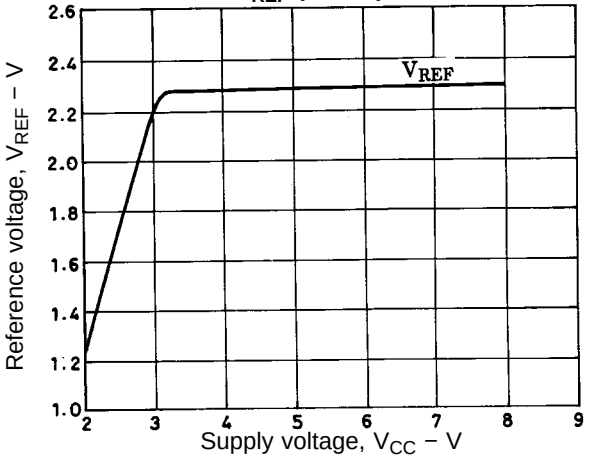
KT characteristics (power off)



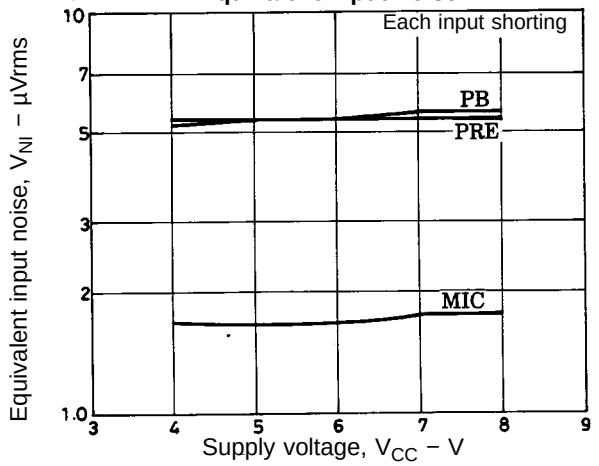
Quiescent current



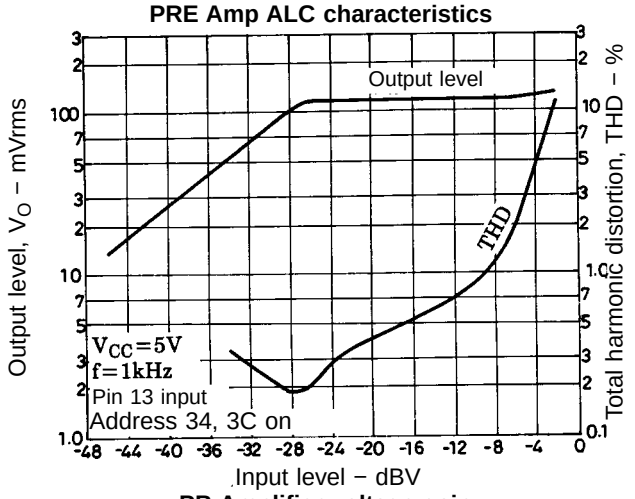
V_{REF} (Pin 30)



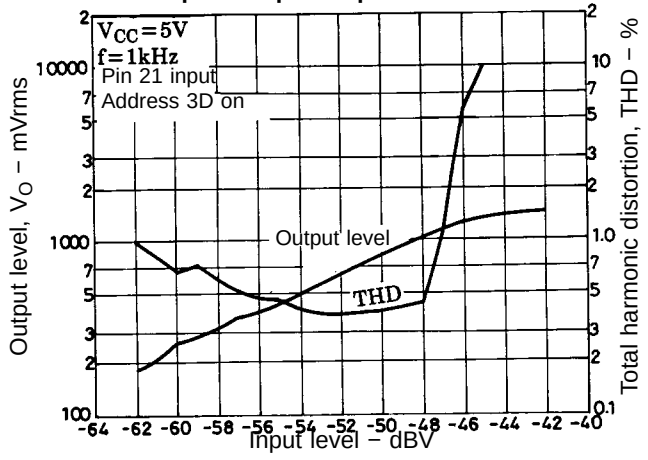
Equivalent input noise



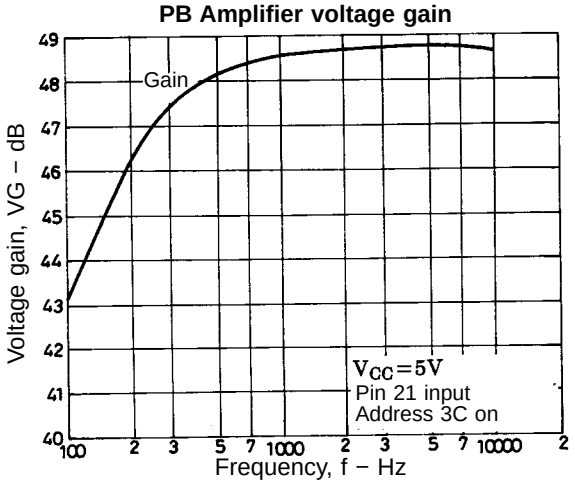
PRE Amp ALC characteristics



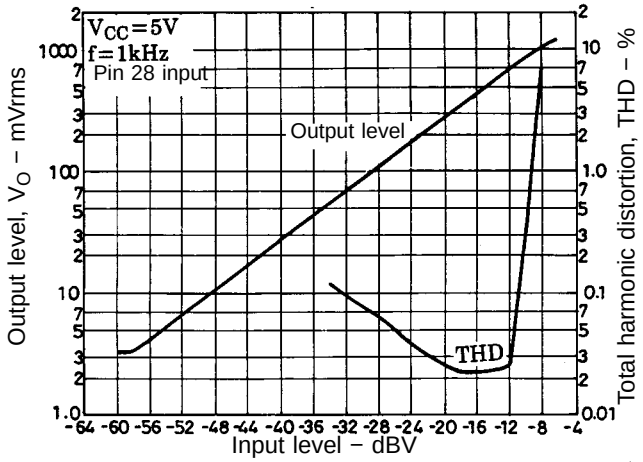
PB Amplifier input/output characteristics



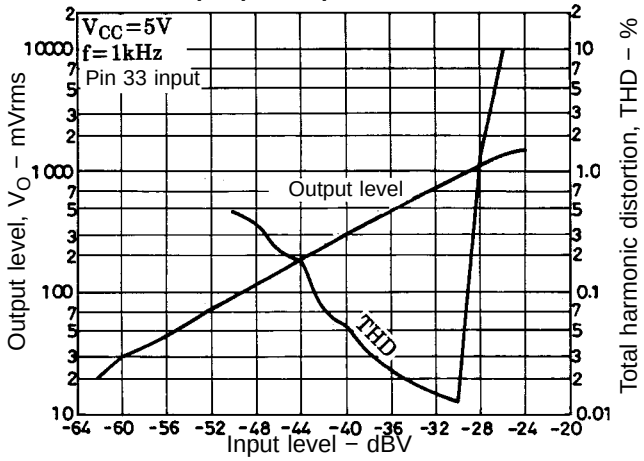
PB Amplifier voltage gain



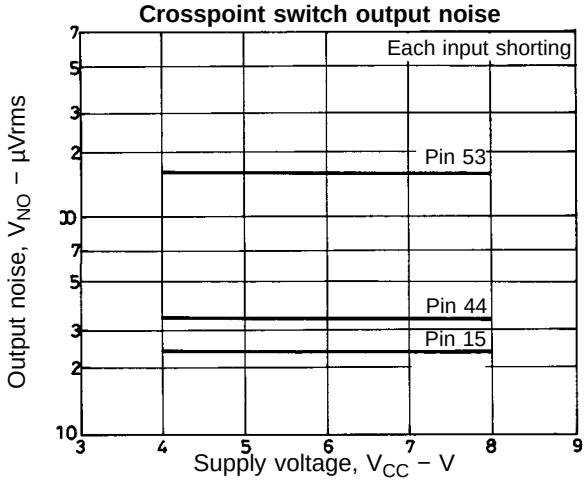
OGM Amplifier input/output characteristics



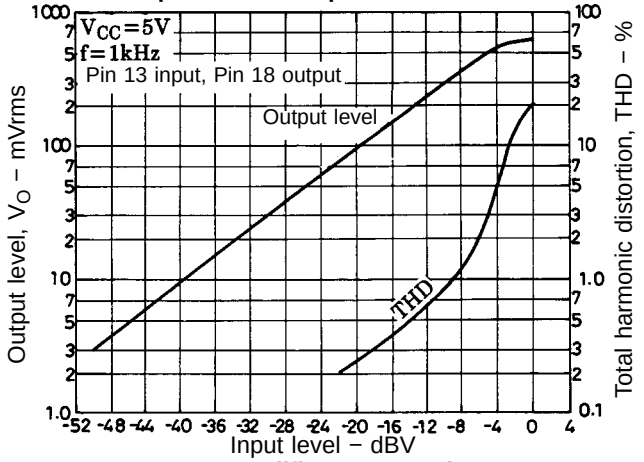
MIC Amp input/output characteristics



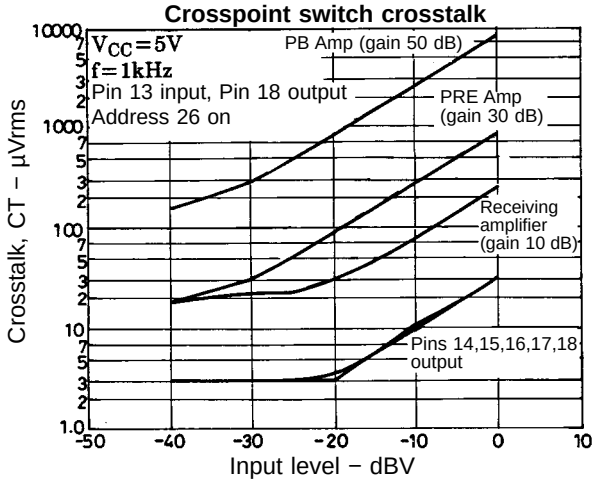
Crosspoint switch output noise



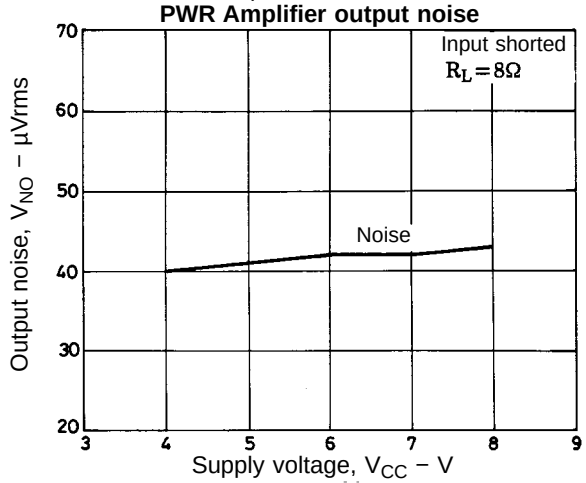
Crosspoint switch input characteristics



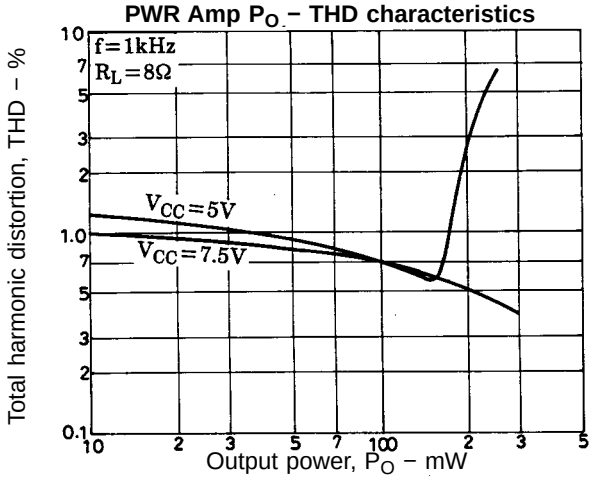
Crosspoint switch crosstalk



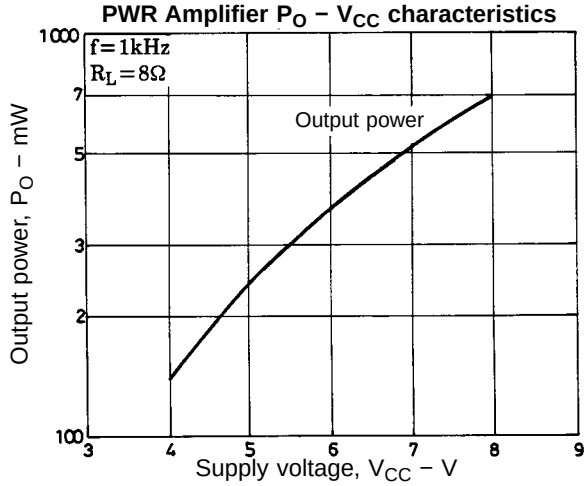
PWR Amplifier output noise



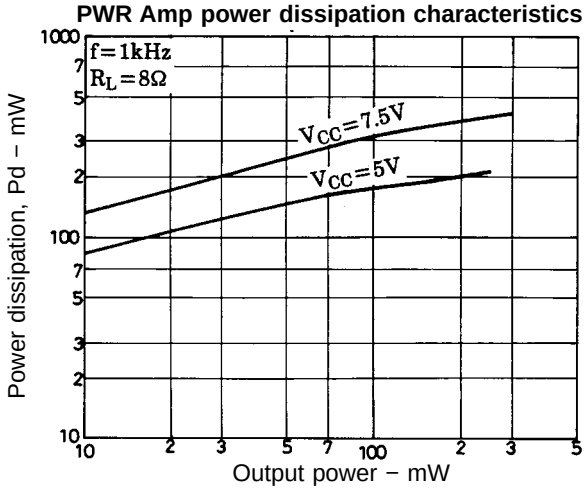
PWR Amp P_O – THD characteristics



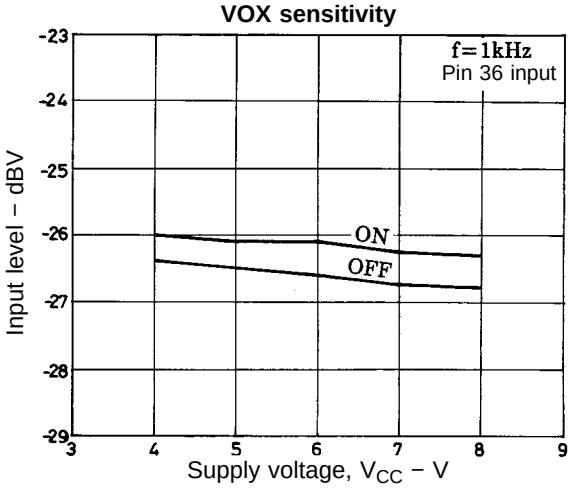
PWR Amplifier P_O – V_{CC} characteristics



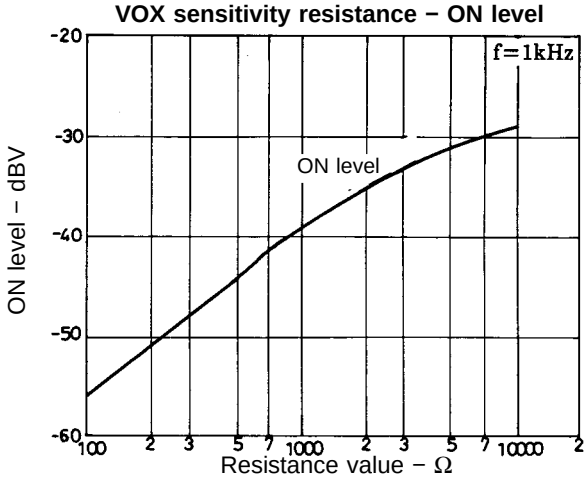
PWR Amp power dissipation characteristics



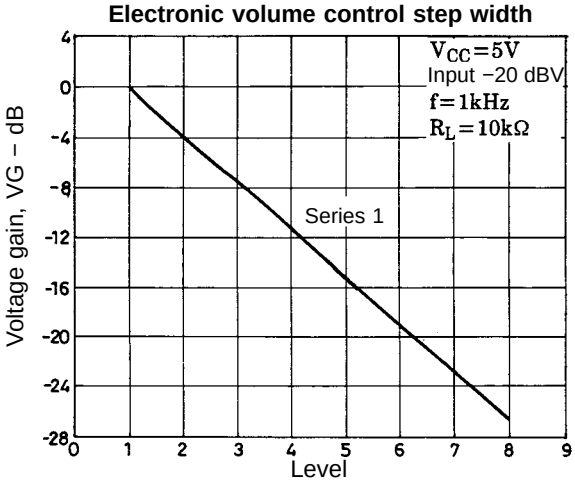
VOX sensitivity



VOX sensitivity resistance – ON level



Electronic volume control step width



VOX waveform shaping duty