

The μ A733M is obsolete
and no longer supplied.

μ A733C, μ A733M DIFFERENTIAL VIDEO AMPLIFIERS

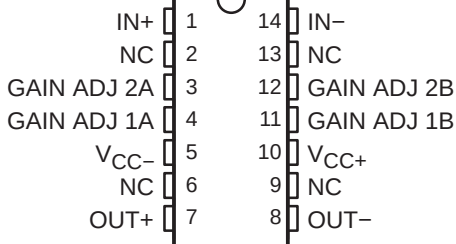
SLFS027B – NOVEMBER 1970 – REVISED MAY 2004

- 200-MHz Bandwidth
- 250-k Ω Input Resistance
- Selectable Nominal Amplification of 10, 100, or 400
- No Frequency Compensation Required

μ A733C . . . D, N, OR NS PACKAGE

μ A733M . . . J PACKAGE

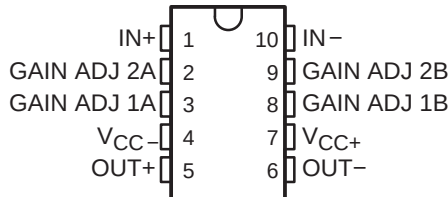
(TOP VIEW)



NC — No internal connection

μ A733M . . . U PACKAGE

(TOP VIEW)



description/ordering information

The μ A733 is a monolithic two-stage video amplifier with differential inputs and differential outputs. Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads, and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 10 V/V, 100 V/V, or 400 V/V may be selected without external components, or amplification may be adjusted from 10 V/V to 400 V/V by the use of a single external resistor connected between 1A and 1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The μ A733C is characterized for operation from 0°C to 70°C; the μ A733M is characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	P-DIP (N)	Tube of 25	UA733CN	UA733CN
	SOIC (D)	Tube of 50	UA733CD	UA733C
		Reel of 2500	UA733CDR	
	SOP (NS)	Reel of 2000	UA733CNSR	UA733

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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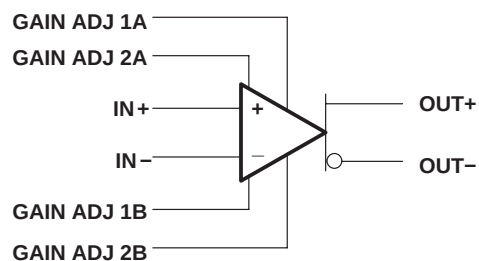
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μA733C, μA733M **DIFFERENTIAL VIDEO AMPLIFIERS**

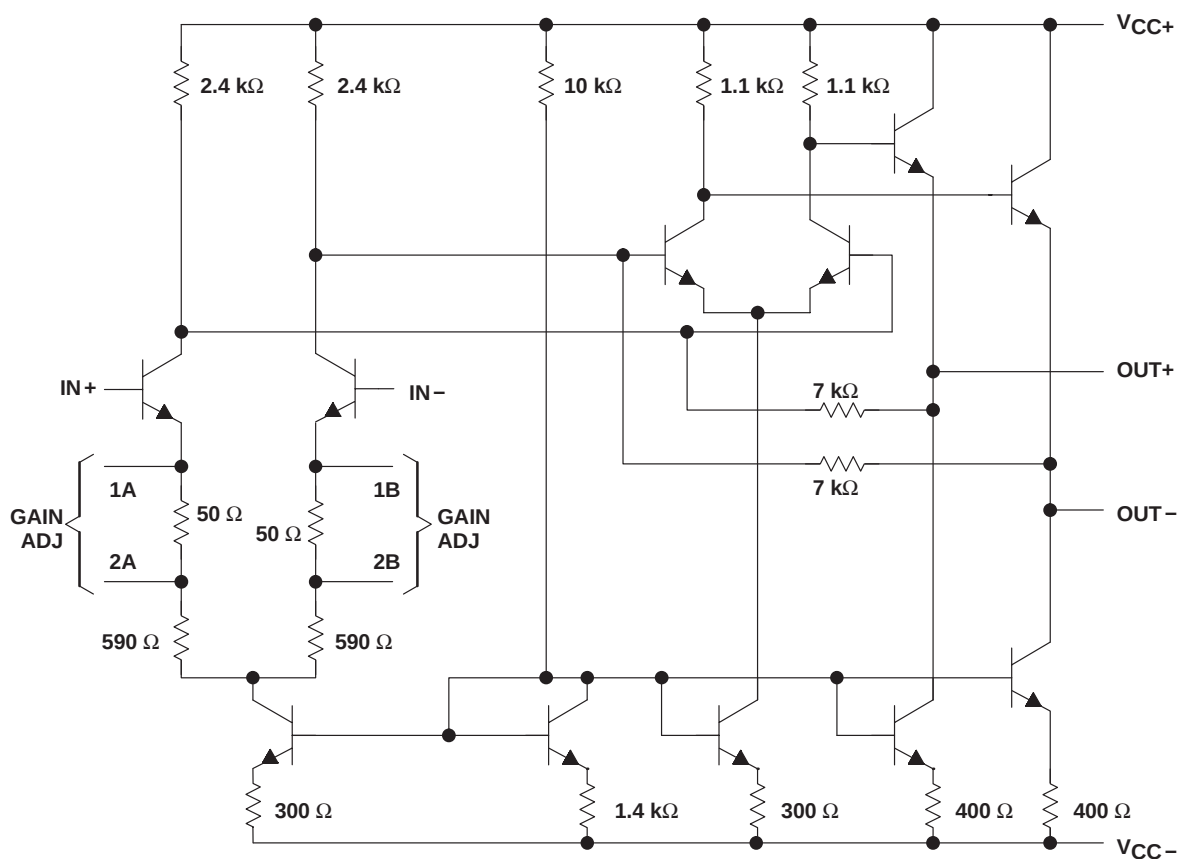
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symbol



schematic



Component values shown are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

		μ A733C	μ A733M	UNIT
Supply voltage V_{CC+} (see Note 1)		8	8	V
Supply voltage V_{CC-} (see Note 1)		– 8	– 8	V
Differential input voltage		± 5	± 5	V
Common-mode input voltage		± 6	± 6	V
Output current		10	10	mA
Continuous total power dissipation		See Dissipation Rating Table		
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	D package	86		$^{\circ}\text{C}/\text{W}$
	N package	80		
	NS package	76		
Maximum junction temperature, T_J		150		$^{\circ}\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package		300	$^{\circ}\text{C}$
Storage temperature range, T_{Stg}		– 65 to 150	– 65 to 150	$^{\circ}\text{C}$

[†] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential input voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^{\circ}\text{C}$ POWER RATING	$T_A = 125^{\circ}\text{C}$ POWER RATING
J (μ A733M)	500 mW	11.0 mW/ $^{\circ}\text{C}$	104°C	500 mW	269 mW

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electrical characteristics, $V_{CC\pm} = \pm 6\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		FIGURE	TEST CONDITIONS	GAIN OPTION†	μA733C			μA733M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A _{VD}	Large-signal differential voltage amplification	1	V _{OD} = 1 V	1	250	400	600	300	400	500	V/V
				2	80	100	120	90	100	110	
				3	8	10	12	9	10	11	
BW	Bandwidth	2	R _S = 50 Ω	1	50			50			MHz
				2	90			90			
				3	200			200			
I _{IO}	Input offset current			Any	0.4 5			0.4 3			μA
I _{IB}	Input bias current			Any	9 30			9 20			μA
V _{ICR}	Common-mode input voltage range	1		Any	±1			±1			V
V _{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V _{OO}	Output offset voltage	1		1	0.6 1.5			0.6 1.5			V
				2 & 3	0.35 1.5			0.35 1			
V _{OPP}	Maximum peak- to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r _i	Input resistance	3	V _{OD} ≤ 1 V	1	4			4			kΩ
				2	10	24		20	24		
				3	250			250			
r _o	Output resistance				20			20			Ω
C _i	Input capacitance	3	V _{OD} ≤ 1 V	2	2			2			pF
CMRR	Common-mode rejection ration	4	V _{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V _{IC} = ±1 V, f = 5 MHz	2	70			70			
k _{SVR}	Supply voltage rejection ratio (ΔV _{CC} /(ΔV _{IO}))	1	ΔV _{CC} ± = ±0.5 V	2	50	70		50	70		dB
V _n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any	12			12			μV
t _{pd}	Propagation delay time	2	R _S = 50 Ω, Output voltage step = 1 V	1	7.5			7.5			ns
				2	6.0	10		6.0	10		
				3	3.6			3.6			
t _r	Rise time	2	R _S = 50 Ω, Output voltage step = 1 V	1	10.5			10.5			ns
				2	4.5	12		4.5	10		
				3	2.5			2.5			
I _{sink(max)}	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I _{CC}	Supply current		No load, No signal	Any	16	24		16	24		mA

† The gain option is selected as follows:

Gain Option 1: Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.

Gain Option 2: Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.

Gain Option 3: All four gain-adjust pins are open.



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electrical characteristics, $V_{CC\pm} = \pm 6\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C for μA733C , -55°C to 125°C for μA733M

PARAMETER		FIGURE	TEST CONDITIONS	GAIN OPTION†	μA733C		μA733M		UNIT
					MIN	MAX	MIN	MAX	
A_{VD}	Large-signal differential voltage amplification	1	$V_{OD} = 1\text{ V}$	1	250	600	200	600	V/V
				2	80	120	80	120	
				3	8	12	8	12	
I_{IO}	Input offset current			Any		6		5	μA
I_{IB}	Input bias current			Any		40		40	μA
V_{ICR}	Common-mode input voltage range	1		Any	± 1		± 1		V
V_{OO}	Output offset voltage	1		1		1.5		1.5	V
				2 & 3		1.5		1.2	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	2.8		2.5		V
r_i	Input resistance	3	$V_{OD} \leq 1\text{ V}$	2	8		8		$\text{k}\Omega$
CMRR	Common-mode rejection ratio	4	$V_{IC} = +1\text{ V}$, $f \leq 100\text{ kHz}$	2	50		50		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/(\Delta V_{IO})$)	1	$\Delta V_{CC\pm} = \pm 0.5\text{ V}$	2	50		50		dB
$I_{\text{sink(max)}}$	Maximum output sink current			Any	2.5		2.2		mA
I_{CC}	Supply current		No load, No signal	Any		27		27	mA

† The gain option is selected as follows:

Gain Option 1: Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.

Gain Option 2: Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.

Gain Option 3: All four gain-adjust pins are open.



PARAMETER MEASUREMENT INFORMATION

test circuits

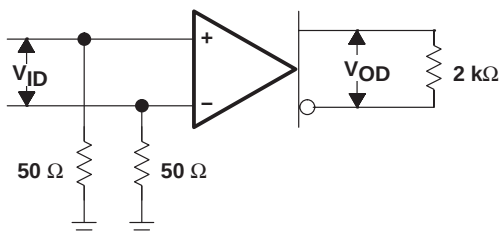


Figure 1

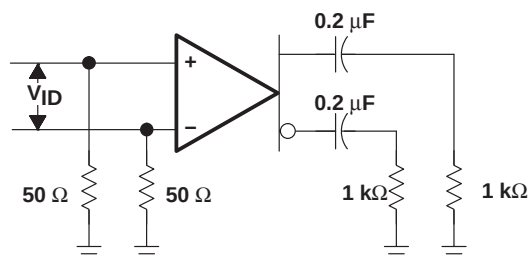


Figure 2

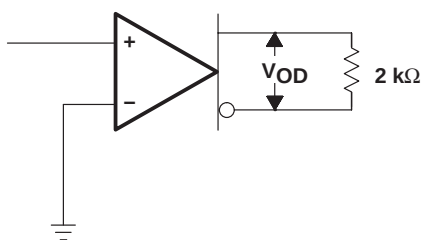


Figure 3

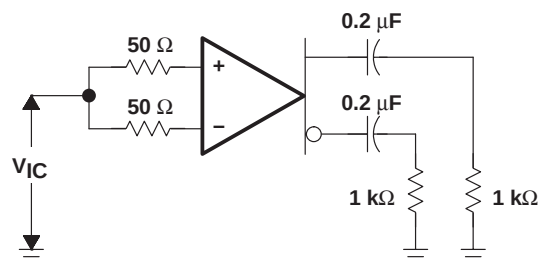


Figure 4

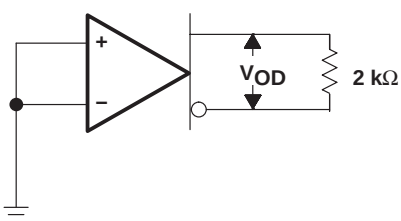
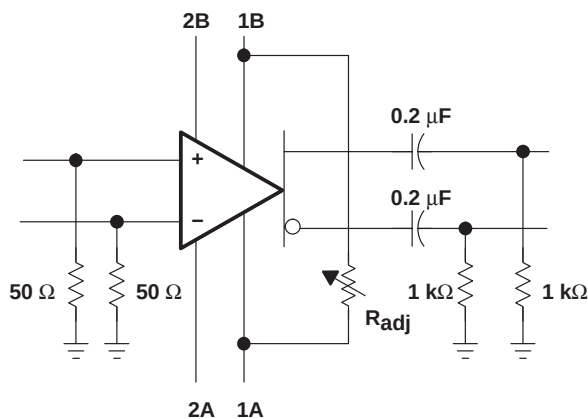


Figure 5



VOLTAGE AMPLIFICATION ADJUSTMENT

Figure 6

TYPICAL CHARACTERISTICS

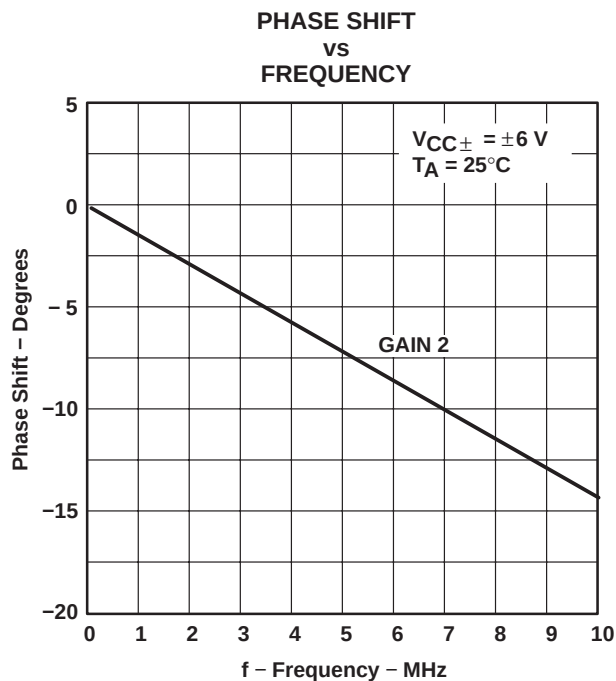


Figure 7

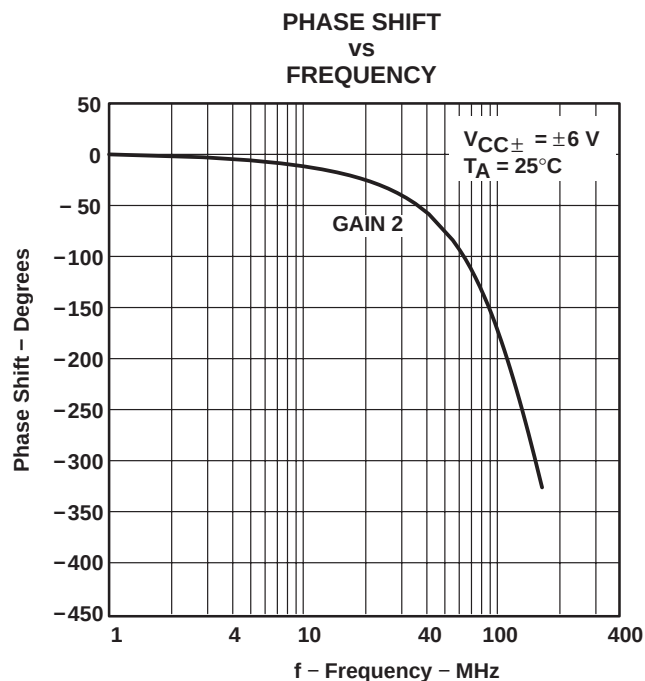


Figure 8

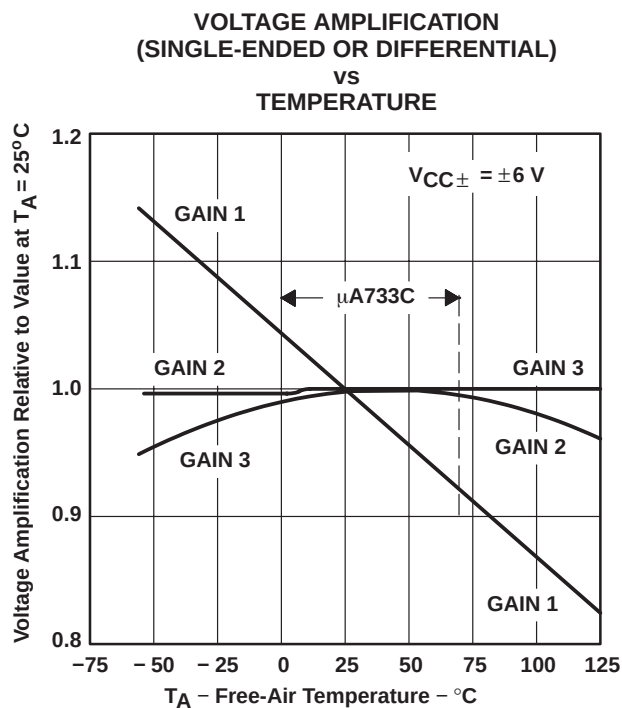


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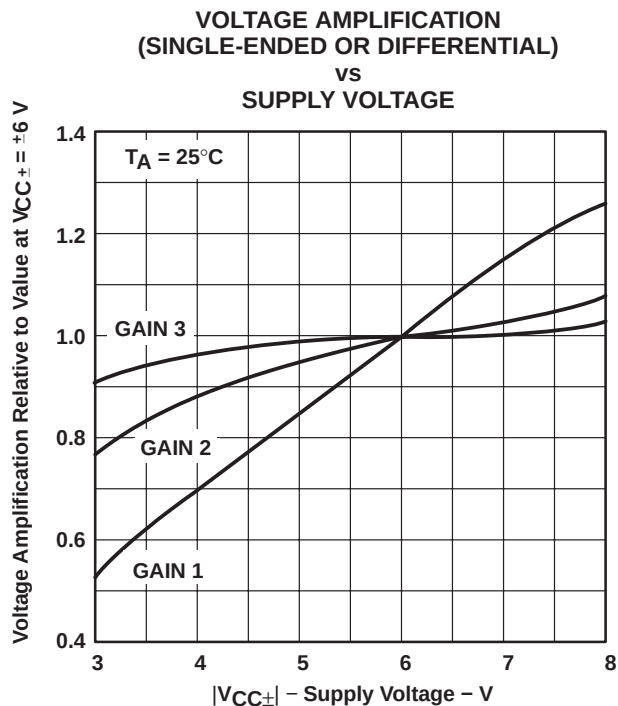


Figure 10

TYPICAL CHARACTERISTICS

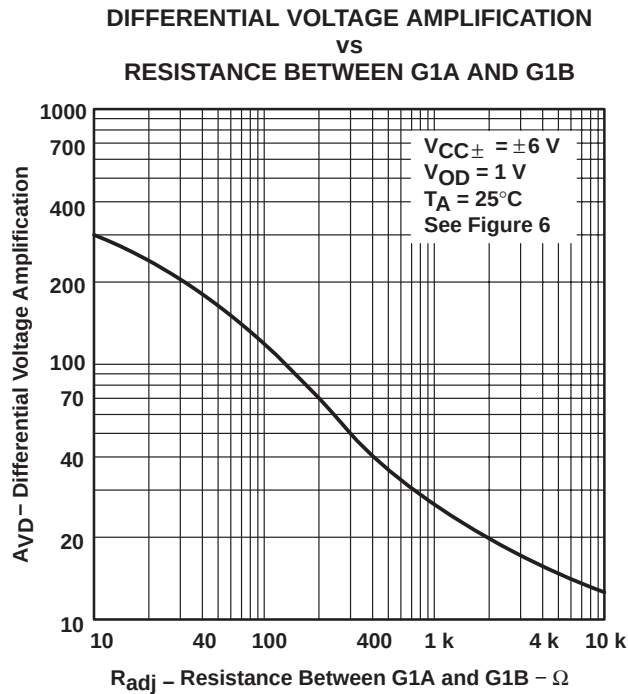


Figure 11

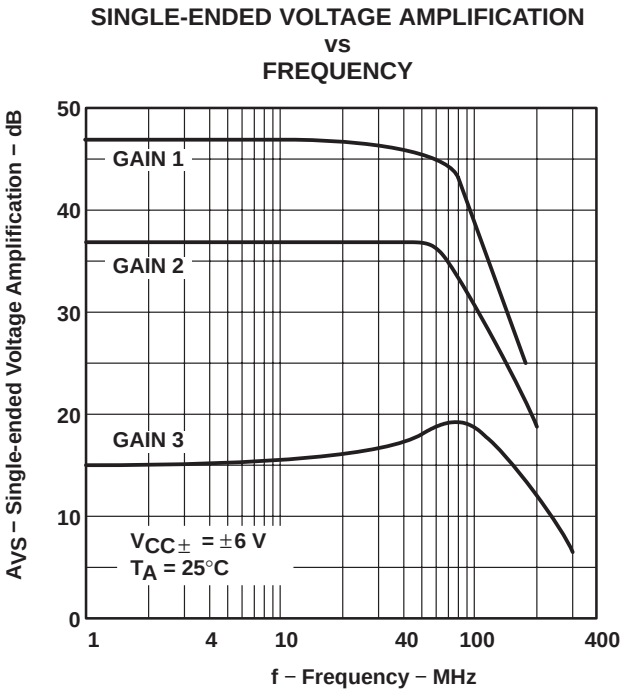


Figure 12

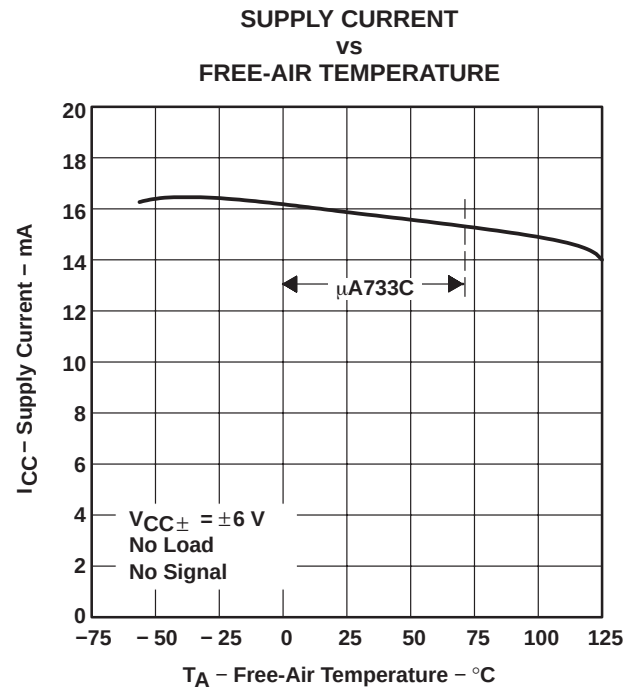


Figure 13

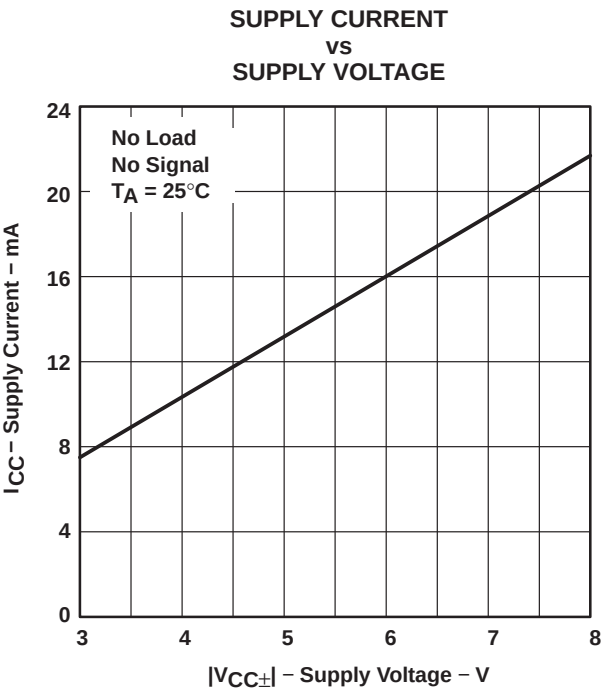


Figure 14

TYPICAL CHARACTERISTICS

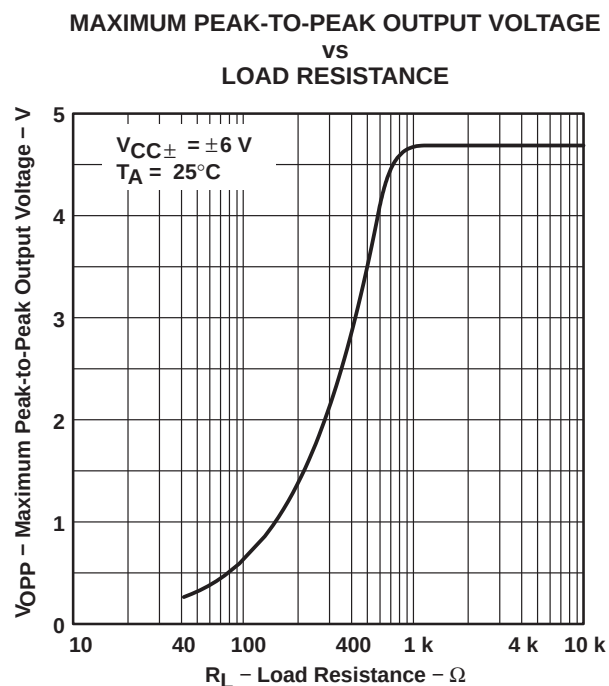


Figure 15

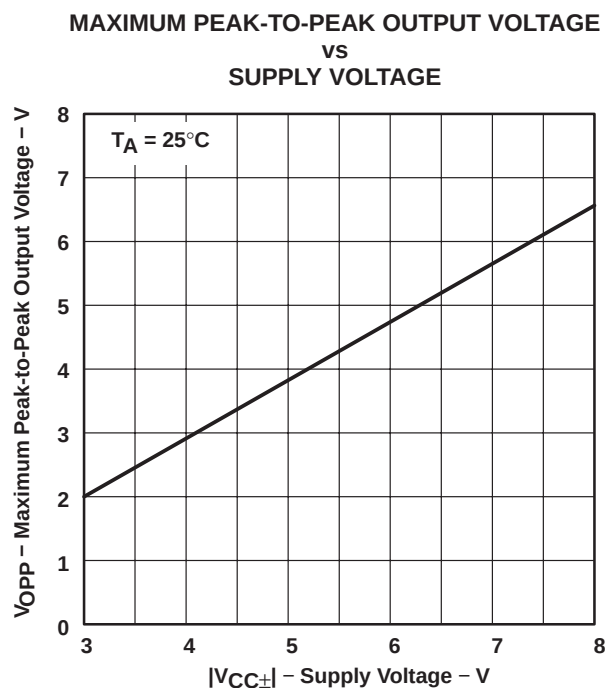


Figure 16

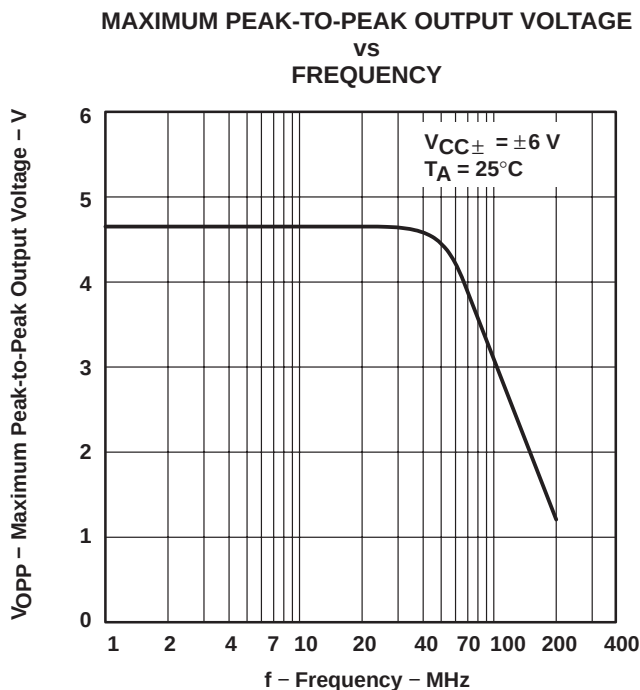


Figure 17

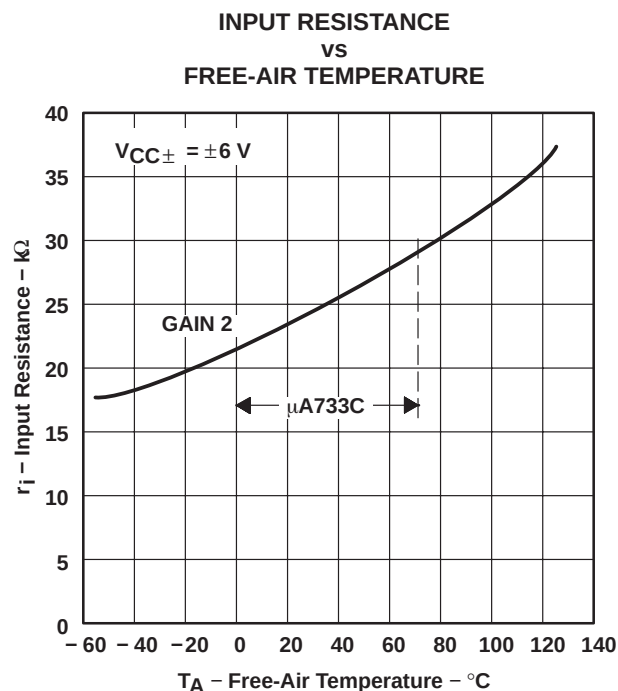
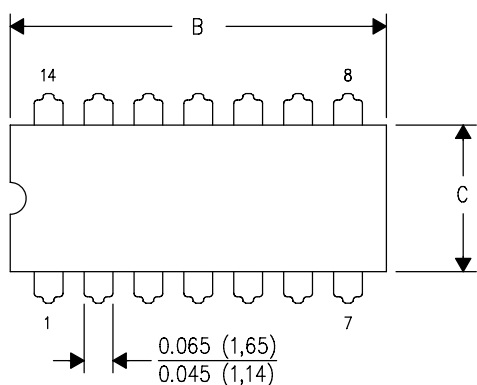


Figure 18

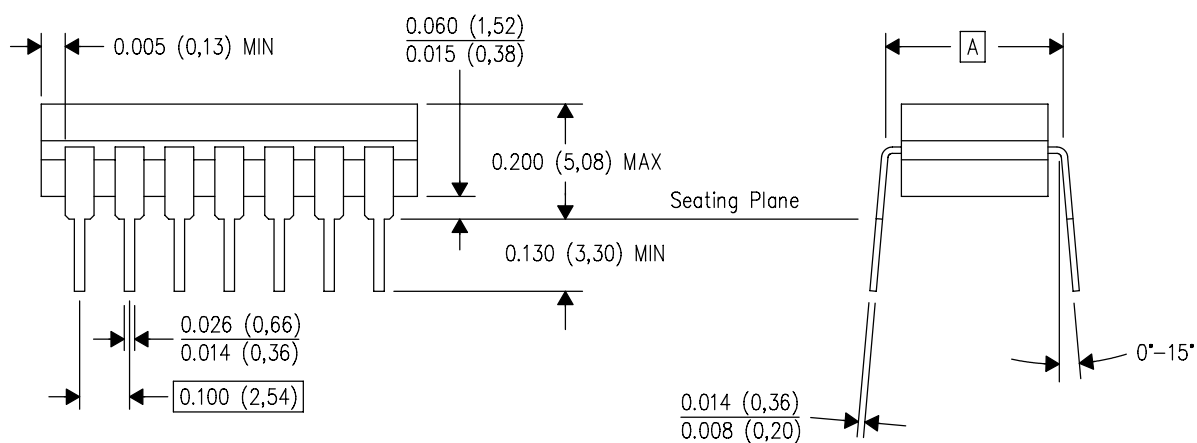
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

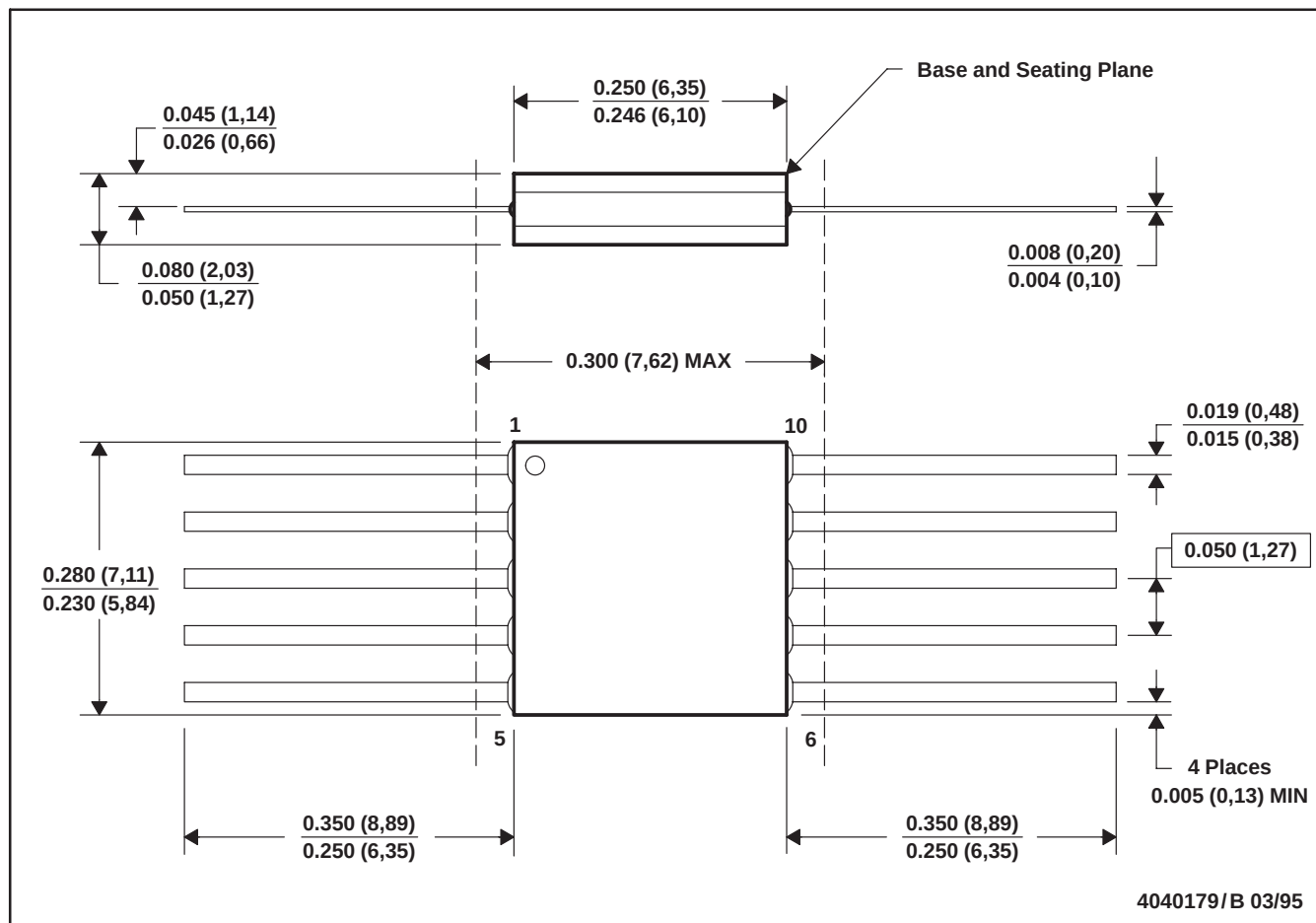


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK

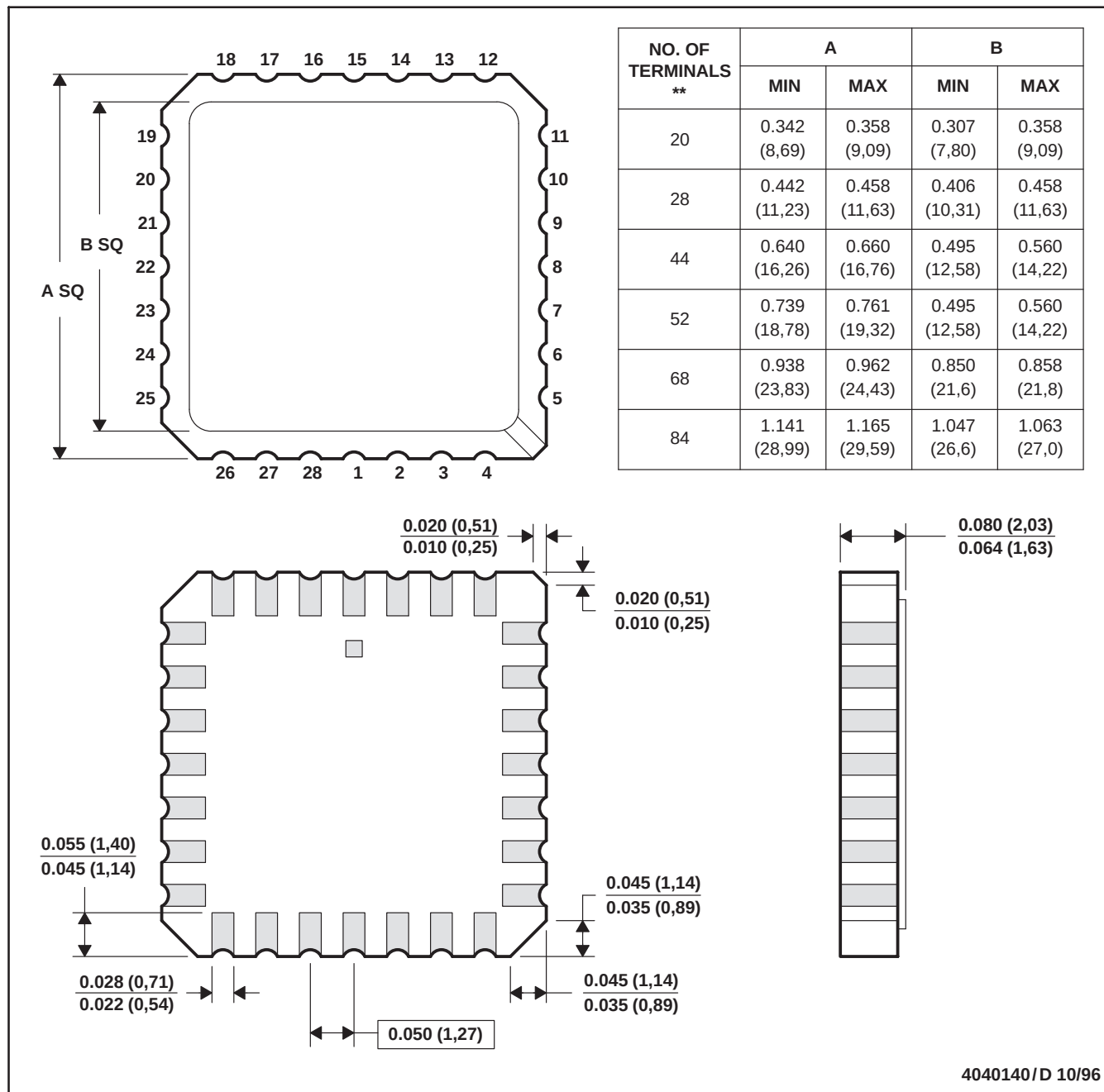


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

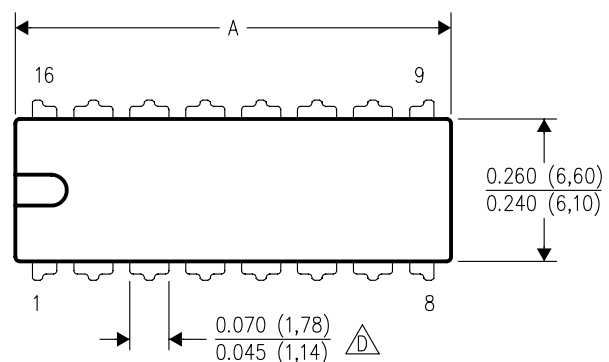


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

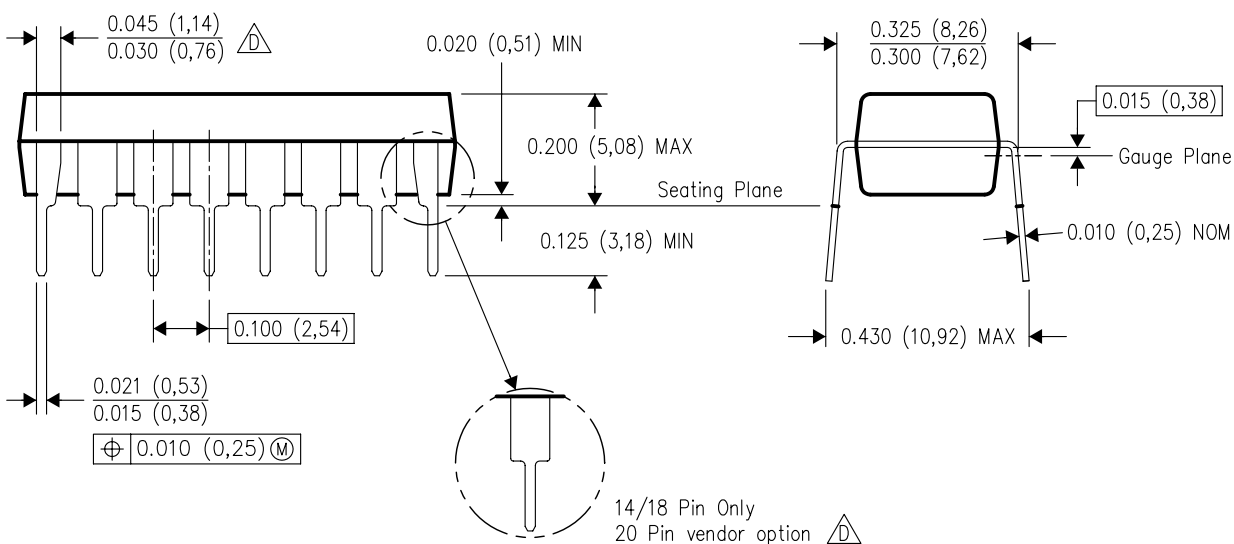
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



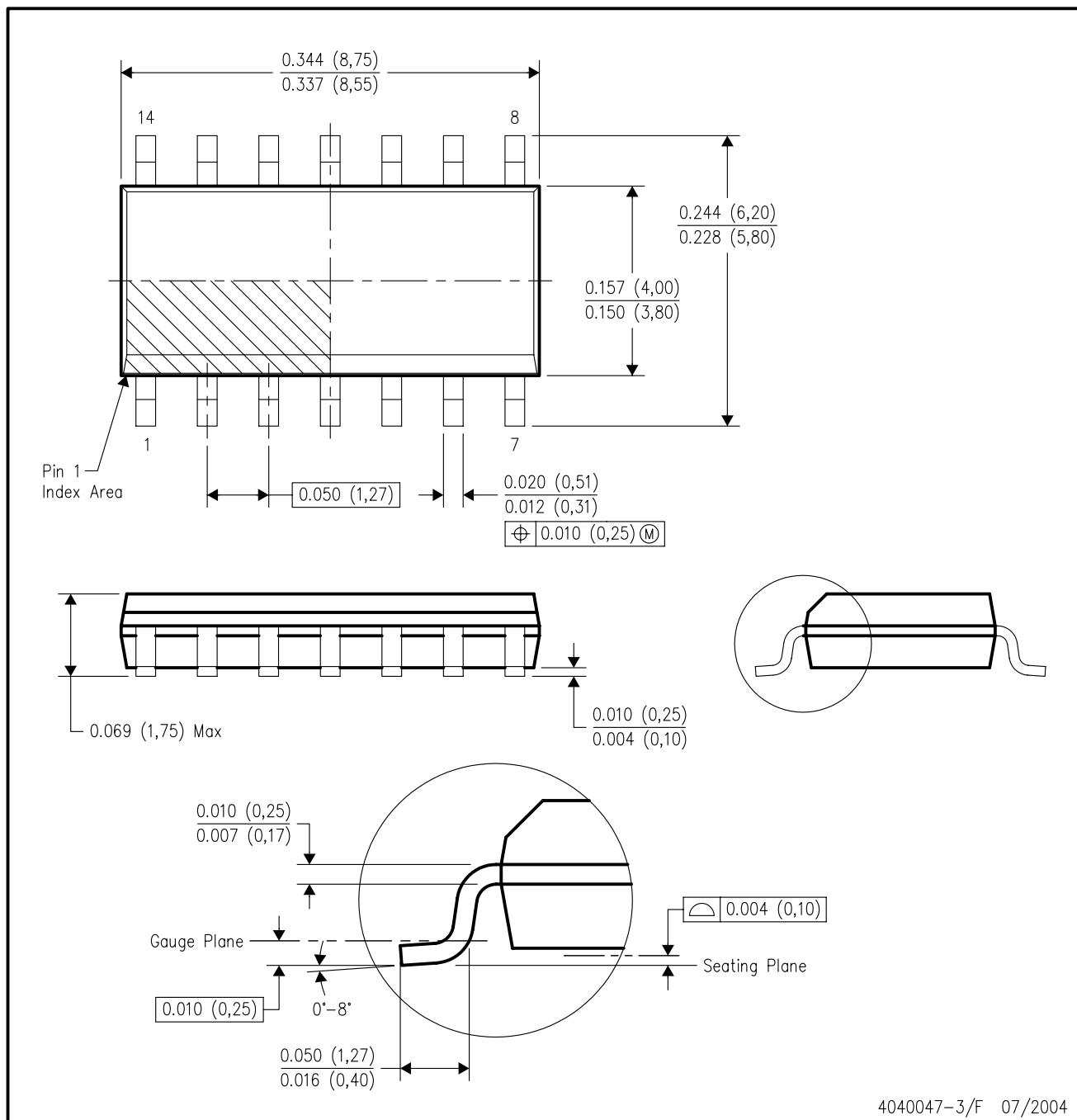
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



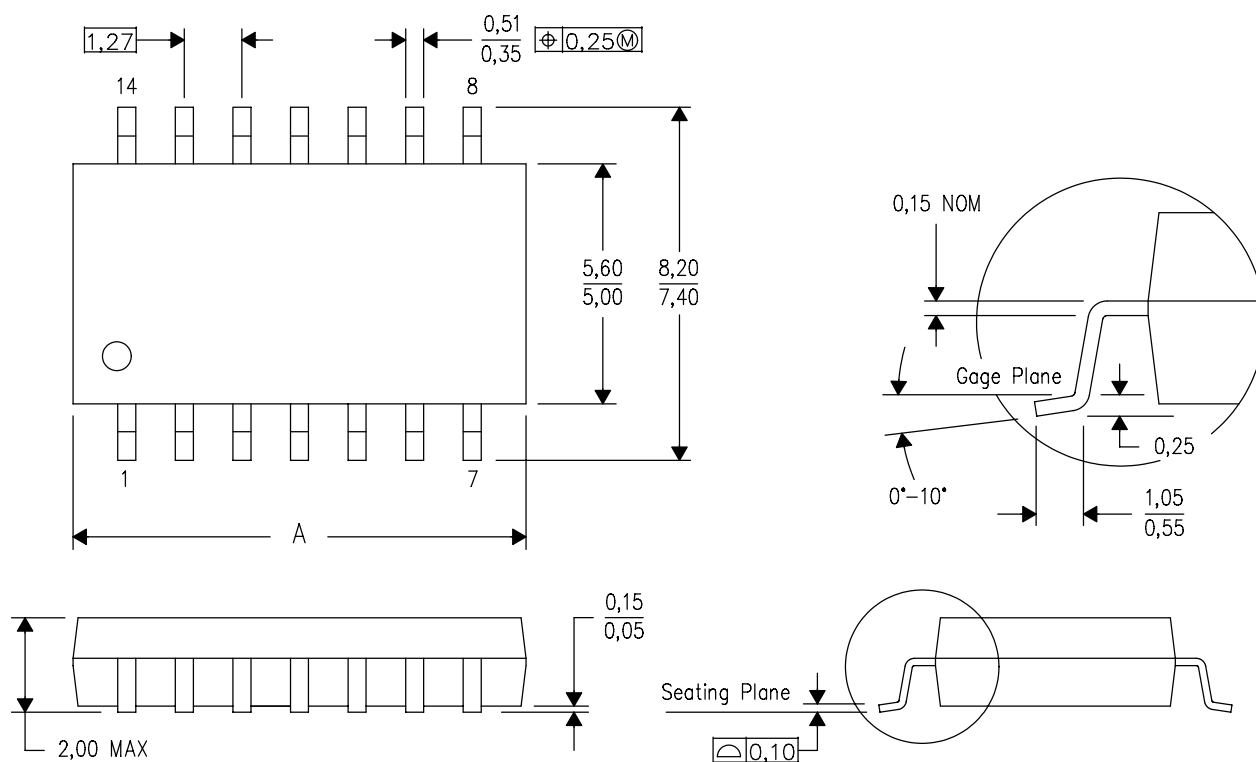
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments
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