

# MC74HC14A

## Hex Schmitt-Trigger Inverter

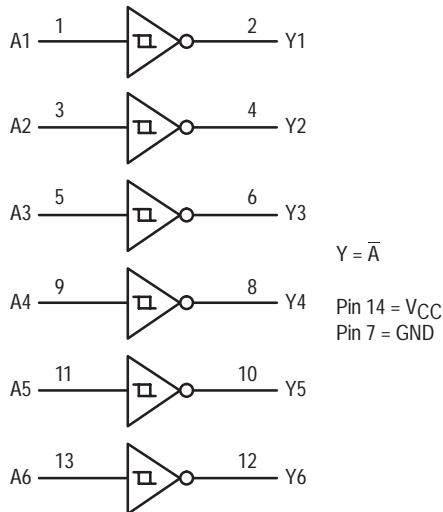
### High-Performance Silicon-Gate CMOS

The MC74HC14A is identical in pinout to the LS14, LS04 and the HC04. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

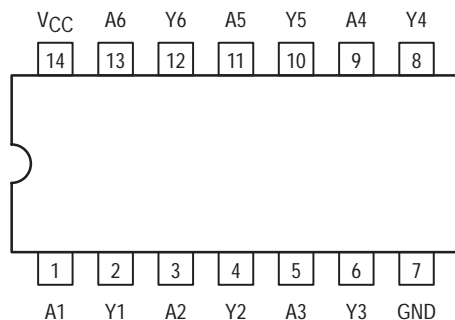
The HC14A is useful to “square up” slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the HC14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 60 FETs or 15 Equivalent Gates

#### LOGIC DIAGRAM



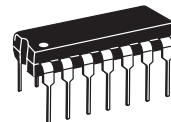
#### Pinout: 14-Lead Packages (Top View)



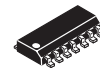
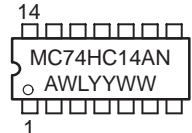
ON Semiconductor

<http://onsemi.com>

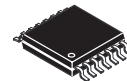
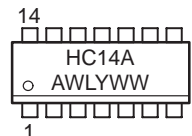
#### MARKING DIAGRAMS



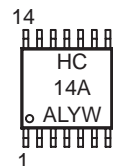
PDIP-14  
N SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

#### FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

#### ORDERING INFORMATION

Device	Package	Shipping
MC74HC14AN	PDIP-14	2000 / Box
MC74HC14AD	SOIC-14	55 / Rail
MC74HC14ADR2	SOIC-14	2500 / Reel
MC74HC14ADT	TSSOP-14	96 / Rail
MC74HC14ADTR2	TSSOP-14	2500 / Reel

# MC74HC14A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T <sub>stg</sub>	Storage Temperature Range	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature Range, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise/Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	No Limit*	ns
		V <sub>CC</sub> = 4.5 V	0	No Limit*	
		V <sub>CC</sub> = 6.0 V	0	No Limit*	

\*When V<sub>in</sub> = 50% V<sub>CC</sub>, I<sub>CC</sub> > 1mA

# MC74HC14A

## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	1.50	1.50	1.50	V
			3.0	2.15	2.15	2.15	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	1.0	0.95	0.95	V
			3.0	1.5	1.45	1.45	
			4.5	2.3	2.25	2.25	
			6.0	3.0	2.95	2.95	
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	0.9	0.95	0.95	V
			3.0	1.4	1.45	1.45	
			4.5	2.0	2.05	2.05	
			6.0	2.6	2.65	2.65	
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	0.3	0.3	0.3	V
			3.0	0.5	0.5	0.5	
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>H</sub> max Note 2	Maximum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	1.20	1.20	1.20	V
			3.0	1.65	1.65	1.65	
			4.5	2.25	2.25	2.25	
			6.0	3.00	3.00	3.00	
V <sub>H</sub> min Note 2	Minimum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	0.20	0.20	0.20	V
			3.0	0.25	0.25	0.25	
			4.5	0.40	0.40	0.40	
			6.0	0.50	0.50	0.50	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> ≤ V <sub>T-</sub> min  I <sub>out</sub>   ≤ 20μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V <sub>in</sub> ≤ V <sub>T-</sub> min     I <sub>out</sub>   ≤ 2.4mA	3.0	2.48	2.34	
I <sub>out</sub>   ≤ 4.0mA	4.5	3.98	3.84	3.70			
I <sub>out</sub>   ≤ 5.2mA	6.0	5.48	5.34	5.20			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> ≥ V <sub>T+</sub> max  I <sub>out</sub>   ≤ 20μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V <sub>in</sub> ≥ V <sub>T+</sub> max     I <sub>out</sub>   ≤ 2.4mA	3.0	0.26	0.33	
I <sub>out</sub>   ≤ 4.0mA	4.5	0.26	0.33	0.40			
I <sub>out</sub>   ≤ 5.2mA	6.0	0.26	0.33	0.40			
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0μA	6.0	1.0	10	40	μA

1. Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

2. V<sub>H</sub>min > (V<sub>T+</sub> min) - (V<sub>T-</sub> max); V<sub>H</sub>max = (V<sub>T+</sub> max) - (V<sub>T-</sub> min).

# MC74HC14A

## AC CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input $t_r = t_f = 6\text{ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
$C_{in}$	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

$C_{PD}$	Power Dissipation Capacitance (Per Inverter)*	Typical @ 25°C, $V_{CC} = 5.0\text{V}$		pF
		22		

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

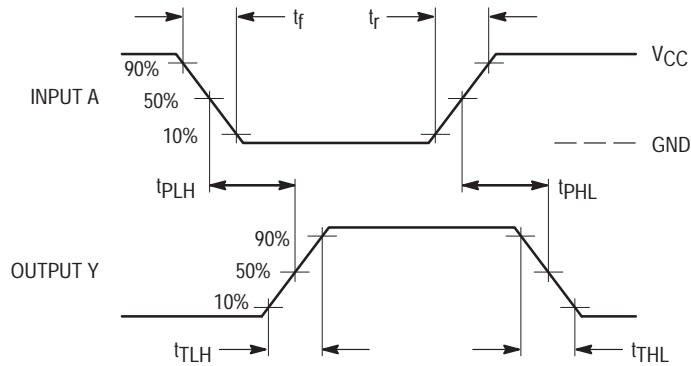
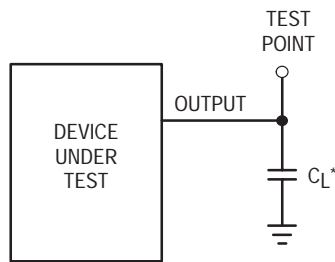


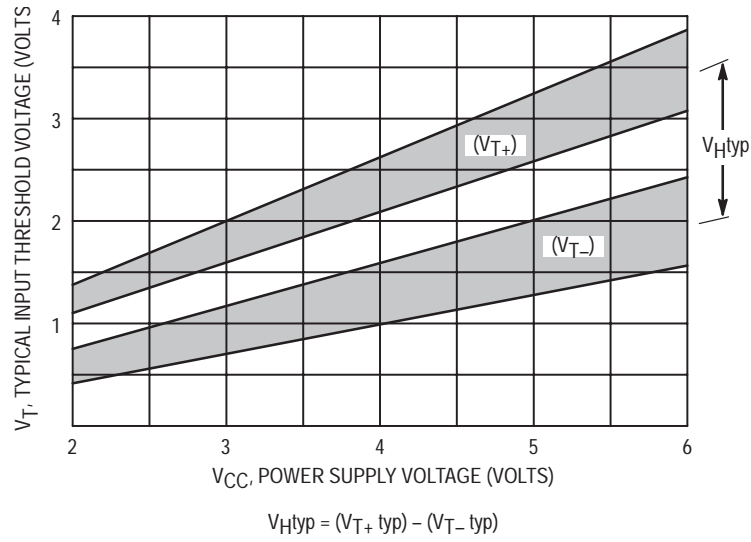
Figure 1. Switching Waveforms



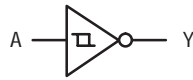
\*Includes all probe and jig capacitance

Figure 2. Test Circuit

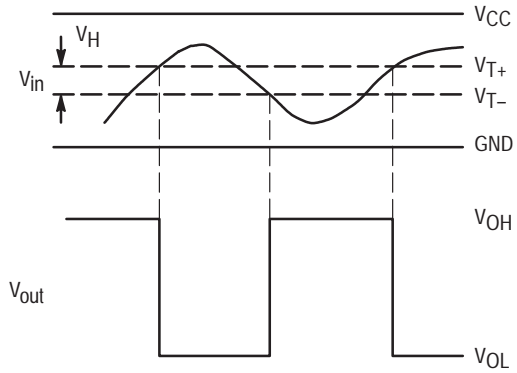
# MC74HC14A



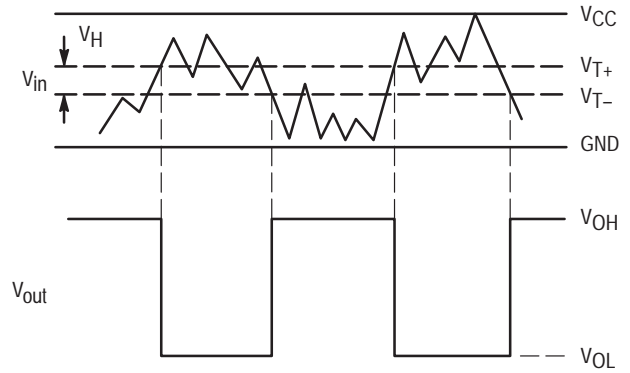
**Figure 3. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$  versus Power Supply Voltage**



(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

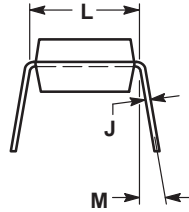
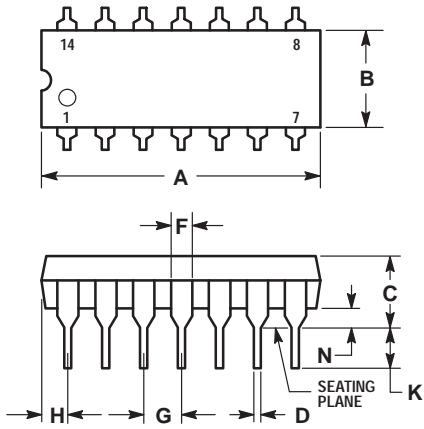


**Figure 4. Typical Schmitt-Trigger Applications**

# MC74HC14A

## PACKAGE DIMENSIONS

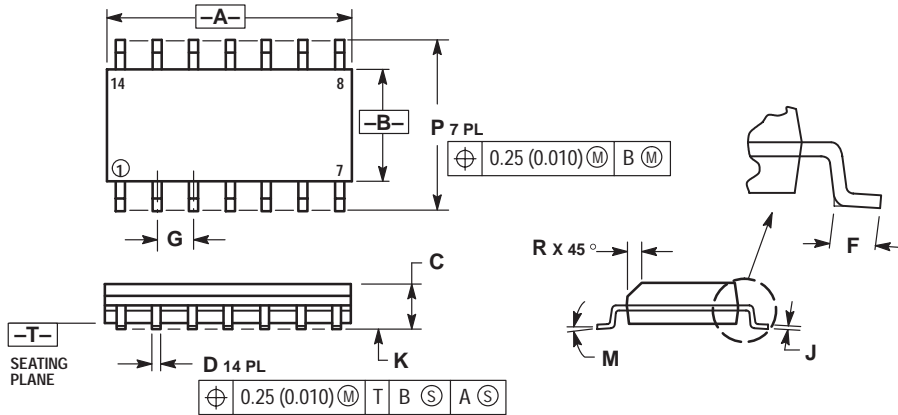
**PDIP-14  
N SUFFIX  
CASE 646-06  
ISSUE L**



- NOTES:
- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  - ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

**SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE F**



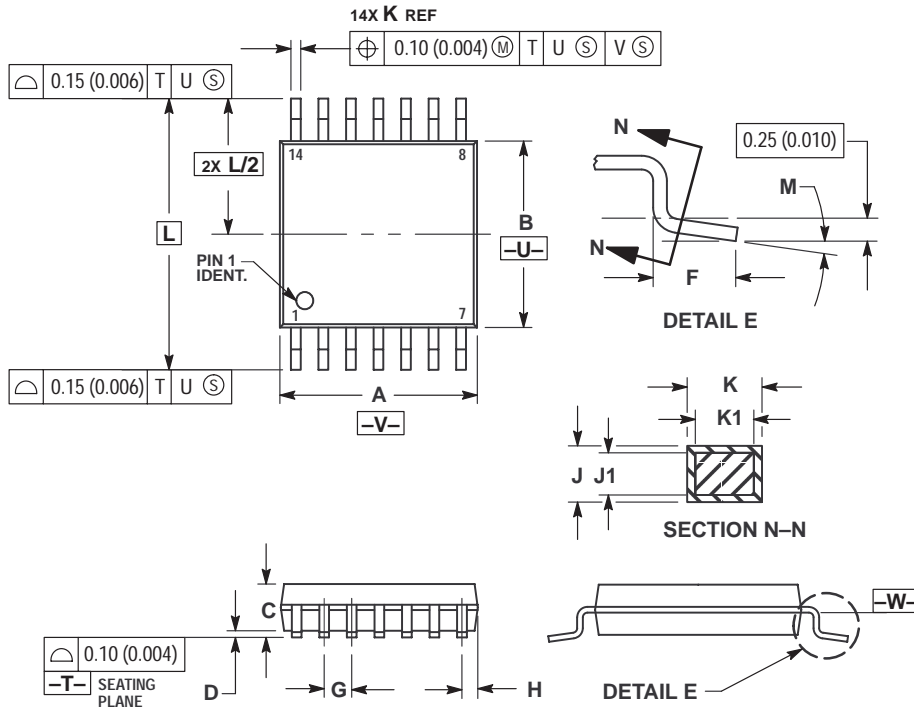
- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

# MC74HC14A

## PACKAGE DIMENSIONS

TSSOP-14  
DT SUFFIX  
CASE 948G-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### **NORTH AMERICA Literature Fulfillment:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, England, Ireland

### **CENTRAL/SOUTH AMERICA:**

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

**Phone:** 81-3-5740-2745  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.