# LTC1562

# Very Low Noise, Low Distortion Active RC Quad Universal Filter

March 1998

## FEATURES

- Four 2nd Order Filter Sections in 16-Pin PDIP or 20-Pin SSOP, 10kHz to 150kHz Center Frequency
- Butterworth, Chebyshev, Elliptic, or Equiripple Delay Response
- Lowpass, Bandpass, Highpass Responses
- 103dB Typical S/N, ±5V Supply (Q = 1)
- 97dB Typical S/N, Single 5V Supply (Q = 1)
- 96dB S/(N + THD) at ±5V Supply, 20kHz Input
- Rail-to-Rail Input and Output Voltages
- DC Accurate to 3mV (Typ)
- ±0.5% Typical Center Frequency Accuracy
- "Zero-Power" Shutdown Mode
- Single or Dual Supply, 5V to 10V Total
- Resistor-Programmable $f_0$, Q, Gain

## APPLICATIONS

- High Resolution Systems (14 Bits to 18 Bits)
- Antialiasing Filters
- Smoothing or Reconstruction Filters
- Data Communications, Equalizers
- Dual or I-and-Q Channels (Two Matched 4th Order Filters in One Package)
- Linear Phase Filtering
- Replacing LC Filter Modules

## DESCRIPTION

The LTC®1562 is a low noise, low distortion active RC filter with rail-to-rail inputs and outputs, optimized for a center frequency ($f_0$) of 10kHz to 150kHz. It contains four independent 2nd order filter blocks, which can be cascaded in any combination, such as one 8th order or two 4th order filters. Each block's response is programmed with three external resistors for center frequency, Q and gain, using simple design formulas. Each 2nd order block provides lowpass and bandpass outputs. Highpass response is available if an external capacitor replaces one of the resistors. Allpass and elliptic responses can also be realized.

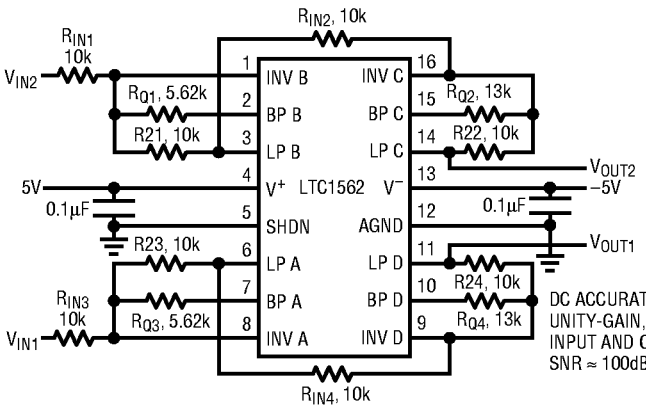
The LTC1562 is designed for applications where dynamic range is important. For example, by cascading 2nd order sections in pairs, the user can configure the IC as a dual 4th order Butterworth lowpass filter with 94dB signal-to-noise ratio from a single 5V power supply. Low level signals can exploit the built-in gain capability of the LTC1562. Varying the gain of a section can achieve a dynamic range as high as 118dB with a ±5V supply.

Other cutoff frequency ranges can be provided upon request. Please contact LTC Marketing.



## TYPICAL APPLICATION

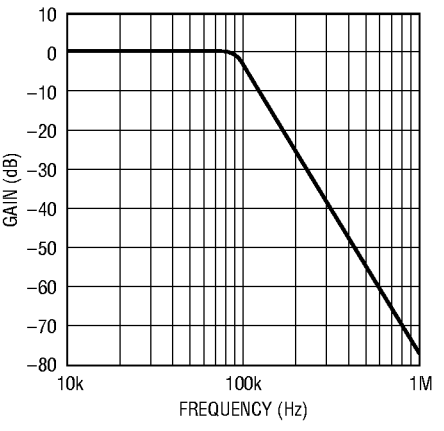
**Dual 4th Order 100kHz Butterworth Lowpass Filter**




DC ACCURATE, NONINVERTING, UNITY-GAIN, RAIL-TO-RAIL INPUT AND OUTPUTS. PEAK SNR ≈ 100dB WITH ±5V SUPPLIES

1562 TA01

**Frequency Response**

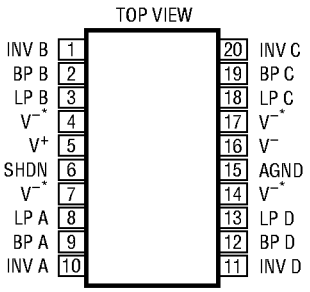



1562 TA02

## ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ($V^+$ to $V^-$) ..... 11V
Maximum Input Voltage
at Any Pin ..... $(V^- - 0.3V) \leq V \leq (V^+ + 0.3V)$
Storage Temperature Range ..... –65°C to 150°C
Operating Temperature Range
LTC1562C ..... 0°C to 70°C
LTC1562I ..... –40°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION



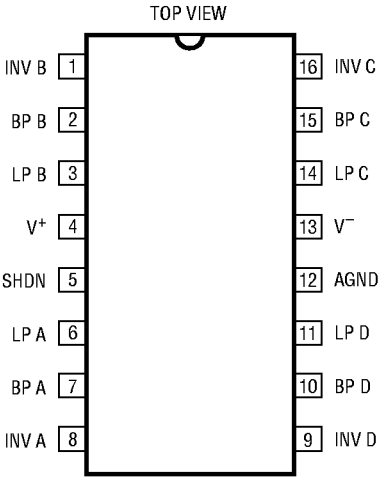

G PACKAGE
20-LEAD PLASTIC SSOP

*G PACKAGE PINS 4, 7, 14, 17 ARE SUBSTRATE/SHIELD CONNECTIONS AND MUST BE TIED TO $V^-$

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 136°C/W

ORDER PART NUMBER

LTC1562CG
LTC1562ACG
LTC1562IG
LTC1562AIG




N PACKAGE
16-LEAD PDIP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 90°C/W

ORDER PART NUMBER

LTC1562CN

(CONSULT MARKETING, ENGINEERING SAMPLES ONLY)

Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

**$V_S$ = ±5V, outputs unloaded, $T_A$ = 25°C, SHDN pin to logic "low" (pages 3, 4), unless otherwise noted. AC specs are for a single 2nd order section, $R_{IN}$ = R2 = $R_Q$ =10k ±0.1%, $f_O$ = 100kHz.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_S$ | Total Supply Voltage | | | 4.75 | | 10.5 | V |
| $I_S$ | Supply Current | $V_S$ = ±2.375V, $R_L$ = 5k, $C_L$ = 30pF, Outputs at 0V | | | 17.3 | 19.5 | mA |
| | | $V_S$ = ±5V, $R_L$ = 5k, $C_L$ = 30pF, Outputs at 0V | | | 19 | 21.5 | mA |
| | | $V_S$ = ±2.375V, $R_L$ = 5k, $C_L$ = 30pF, Outputs at 0V | ● | | | 23.5 | mA |
| | | $V_S$ = ±5V, $R_L$ = 5k, $C_L$ = 30pF, Outputs at 0V | ● | | | 25.5 | mA |
| | Output Voltage Swing | $V_S$ = ±2.375V, $R_L$ = 5k, $C_L$ = 30pF | ● | 4.2 | 4.6 | | $V_{P-P}$ |
| | | $V_S$ = ±5V, $R_L$ = 5k, $C_L$ = 30pF | ● | 9.5 | 9.8 | | $V_{P-P}$ |
| $V_{OS}$ | DC Offset Magnitude, LP Outputs | $V_S$ = ±2.375V, Input at AGND Voltage | ● | | 3 | 15 | mV |
| | | $V_S$ = ±5V, Input at AGND Voltage | ● | | 3 | 15 | mV |
| | DC AGND Reference Point | $V_S$ = Single 5V Supply | | | 2.5 | | V |
| | Center Frequency ($f_O$) Error (Note 1) | | | | | | |
| | LTC1562 (Note 2) | $V_S$ = ±5V, LP Output $R_L$ = 5k, $C_L$ = 30pF | | | 0.5 | 1.2 | % |
| | LTC1562A (Note 3) | $V_S$ = ±5V, LP Output $R_L$ = 5k, $C_L$ = 30pF | | | 0.3 | | % |
| $H_L$ | LP Passband Gain | $V_S$ = ±2.375V, $f_{IN}$ = 10kHz, LP Output $R_L$ = 5k, $C_L$ = 30pF | ● | 0 | +0.05 | +0.1 | dB |

## ELECTRICAL CHARACTERISTICS

**$V_S$ = ±5V, outputs unloaded, $T_A$ = 25°C, SHDN pin to logic "low" (pages 3, 4), unless otherwise noted. AC specs are for a single 2nd order section, $R_{IN}$ = R2 = $R_Q$ =10k ±0.1%, $f_O$ = 100kHz.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $H_B$ | BP Passband Gain | $V_S$ = ±2.375V, $f_{IN}$ = $f_O$, LP Output $R_L$ = 5k, $C_L$ = 30pF | ● | | +0.2 | +0.5 | dB |
| | Q Accuracy | $V_S$ = ±2.375V, LP Output $R_L$ = 5k, $C_L$ = 30pF | | | +3 | | % |
| | Wideband Output Noise | $V_S$ = ±2.375V, BW = 200kHz, Input AC GND<br>$V_S$ = ±5V, BW = 200kHz, Input AC GND | | | 24<br>24 | | $\mu V_{RMS}$<br>$\mu V_{RMS}$ |
| | Input-Referred Noise, Gain = 100 | BW = 200kHz, $f_O$ = 100kHz, Q = 1, Input AC GND | | | 4.5 | | $\mu V_{RMS}$ |
| THD | Total Harmonic Distortion, LP Output | $f_{IN}$ = 20kHz, 2.8$V_{P-P}$. LP and BP Outputs $R_L$ = 5k, $C_L$ = 30pF | | | –96 | | dB |
| | | $f_{IN}$ = 100kHz, 2.8$V_{P-P}$. LP and BP Outputs $R_L$ = 5k, $C_L$ = 30pF | | | –78 | | dB |
| | Shutdown Supply Current | SHDN Pin to $V^+$<br>SHDN Pin to $V^+$, $V_S$ = ±2.375V | | | 1.5<br>1.0 | 5 | µA<br>µA |
| | Shutdown-Input Logic Threshold | | | | 2.5 | | V |
| | Shutdown-Input Bias Current | SHDN Pin to 0V | | | –10 | –20 | µA |
| | Shutdown Delay | SHDN Pin Steps from 0V to $V^+$ | | | 20 | | µs |
| | Shutdown Recovery Delay | SHDN Pin Steps from $V^+$ to 0V | | | 100 | | µs |
| | Inverting Input Bias Current, Each Biquad | | | | 5 | | pA |

The ● denotes specifications that apply over the full operating temperature range.

**Note 1:** $f_O$ change from ±5V to ±2.375 supplies is –0.15% typical, $f_O$ temperature coefficient, –40°C to 85°C, is 25ppm/°C typical.

**Note 2:** This data sheet reflects initial production limits that will be tightened in the final data sheet.

**Note 3:** The LTC1562A, with tighter guaranteed $f_O$, will soon be available. Contact LTC Marketing.

## PIN FUNCTIONS

**Power Supply Pins:** The $V^+$ and $V^-$ pins should be bypassed with 0.1µF capacitors to an adequate analog ground or ground plane. These capacitors should be connected as closely as possible to the supply pins. In the 20-lead SSOP package, the additional pins 4, 7, 14 and 17 are internally connected to $V^-$ (Pin 16) and should also be tied to the same point as Pin 16 for best shielding. Low noise linear supplies are recommended. Switching supplies are not recommended as they will lower the filter dynamic range.

**Analog Ground (AGND):** The AGND pin is the midpoint of a resistive voltage divider, developing a potential halfway between the $V^+$ and $V^-$ pins, with an equivalent series resistance nominally 7kΩ. This serves as an internal ground reference. Filter performance will reflect the quality of the analog signal ground and an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, the AGND pin should be connected to the ground plane. For single supply operation, the AGND pin should be bypassed to the ground plane with at least a 0.1µF capacitor (at least 1µF for best AC performance).

**Shutdown (SHDN):** When the SHDN input goes high or is open-circuited, the LTC1562 enters a "zero-power" shutdown state and only junction leakage currents flow. The AGND pin and the amplifier outputs (see Figure 1) assume a high impedance state and the amplifiers effectively disappear from the circuit. (If an input signal is applied to a complete filter circuit while the LTC1562 is in shutdown, some signal will normally flow to the output through passive components around the inactive op amps.)

A small pull-up current source at the SHDN input *defaults the LTC1562 to the shutdown state if the SHDN pin is left floating.* Therefore, the user *must* connect the SHDN pin

## PIN FUNCTIONS

to a logic "low" (0V for ±5V supplies, $V^-$ for 5V total supply) for normal operation of the LTC1562. (This convention permits true "zero-power" shutdown since not even the driving logic must deliver current while the part is in shutdown.)

**INV A, INV B, INV C, INV D:** Each of the INV pins is a virtual-ground summing point for the corresponding 2nd order section. For each section, all three external resistors $R_{IN}$, R2, $R_Q$ connect to the INV pin as shown in Figure 1 and described further in the Applications Information. Note that the INV pins are sensitive internal nodes of the filter and will readily receive any unintended signals that are capacitively coupled into them. Capacitance to the INV nodes will also affect the frequency response of the filter sections. For these reasons, printed circuit connections to the INV pins must be kept as short as possible, less than one inch (2.5cm) total and surrounded by a ground plane.

**LP A, LP B, LP C, LP D:** Output Pins. Provide a lowpass, bandpass or other response depending on external circuitry (see Applications Information section). Each LP pin also connects to the R2 resistor of the corresponding 2nd order filter section (see Figure 1 and Applications Information). Each output is designed to drive a nominal net load of 5kΩ and 30pF, which includes the loading due to the external R2. Distortion performance improves when the outputs are loaded as lightly as possible.

**BP A, BP B, BP C, BP D:** Output Pins. Provide a bandpass, highpass or other response depending on external circuitry (see Applications Information section). Each BP pin also connects to the $R_Q$ resistor of the corresponding 2nd order filter section (see Figure 1 and Applications Information). Each output is designed to drive a nominal net load of 5kΩ and 30pF, which includes the loading due to the external $R_Q$. Distortion performance improves when the outputs are loaded as lightly as possible.

## BLOCK DIAGRAMS

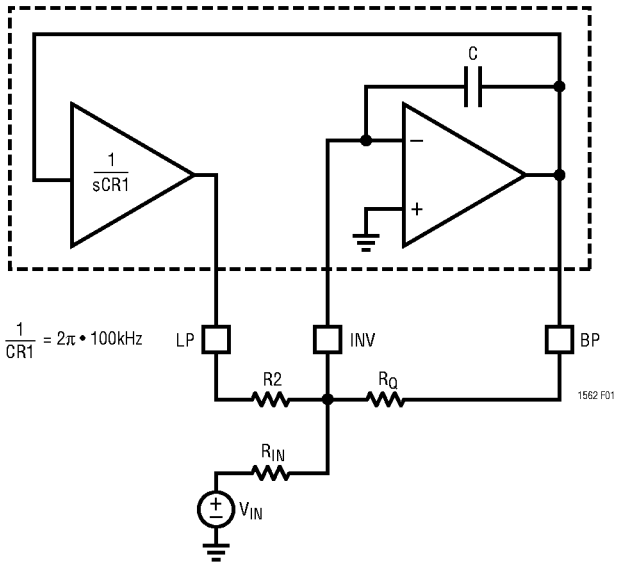



**Figure 1. Equivalent Circuit of a Single 2nd Order Section (Inside Dashed Line) Shown in a Simple Application. External Resistors R2, $R_{IN}$ and $R_Q$ in This Example Set up a Lowpass Response from $V_{IN}$ to the LP Output and a Bandpass Response from $V_{IN}$ to the BP Output**

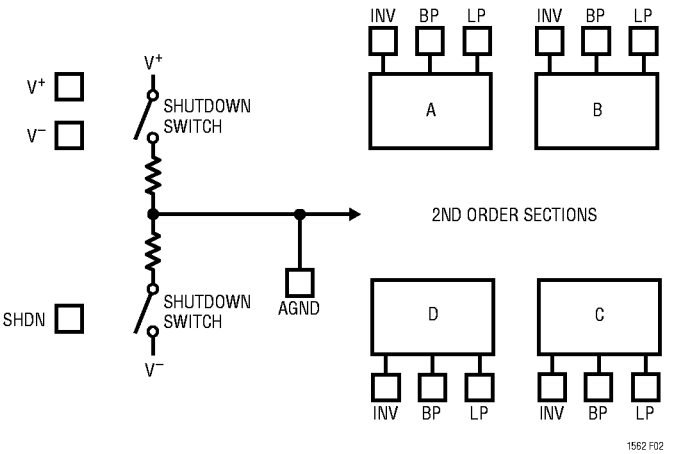



**Figure 2. Overall Block Diagram Showing Four 3-Terminal 2nd Order Sections**

## APPLICATIONS INFORMATION

### Functional Description

The LTC1562 contains four matched, 2nd order, 3-terminal universal continuous-time filter blocks, each with a virtual-ground input node (INV) and two rail-to-rail outputs. In the most basic application, one such block and three external resistors provide 2nd order lowpass and bandpass filtering functions simultaneously (Figure 1). The three external resistors program $f_0$, Q and gain. A combination of internal precision components and an external resistor R2 sets the center frequency $f_0$ of each 2nd order block. The LTC1562 is trimmed at manufacture so that $f_0$ will be 100kHz ±0.5% if the external resistor R2 is exactly 10k.

However, lowpass/bandpass filtering is only one specific application for the 2nd order building blocks in the LTC1562. Highpass response results if the external input resistor $R_{IN}$ of Figure 1 is replaced by a capacitor $C_{IN}$ (which sets only gain, not critical frequencies) as described below. Responses with zeroes (e.g., elliptic or notch responses) are available by feedforward connections with multiple 2nd order blocks (see Typical Applications). Moreover, the virtual-ground input gives each 2nd order section the built-in capability for analog operations such as gain (preamplification), summing and weighting of multiple inputs, or accepting current or charge signals directly. **These Operational Filter™ frequency-selective building blocks are nearly as versatile as operational amplifiers.**

### Setting $f_0$, Q and Gain

Standard all-pole transfer functions characterize the response of each 2nd order filter section. The responses from $V_{IN}$ in Figure 1 to the LP and BP outputs are, respectively,

$$H_{LP}(s) = \frac{-H_L\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

$$H_{BP}(s) = \frac{-H_B(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

The external resistors R2, $R_{IN}$ and $R_Q$ set the filter parameters $\omega_0 = 2\pi f_0$, Q, $H_L$ and $H_B$ as follows:

$$f_0 = \frac{1}{2\pi\sqrt{R1R2}\,C} = \left(\sqrt{\frac{10k\Omega}{R2}}\right)(100kHz)$$

$$\text{or, } R2 = \left(\frac{100kHz}{f_0}\right)^2(10k\Omega)$$

$$Q = \frac{R_Q}{\sqrt{R1R2}} \quad H_L = \frac{R2}{R_{IN}} \quad H_B = \frac{R_Q}{R_{IN}}$$

Note that R1 (=10k) and C (=159pF) are internal to the LTC1562 while R2, $R_{IN}$ and $R_Q$ are external. The usual design procedure is to first determine R2 from the required $f_0$, then determine $R_Q$ to set Q once R2 is known, and finally determine $R_{IN}$ to set gain.

The $f_0$ range is approximately 10kHz to 150kHz, limited mainly by the magnitudes of the external resistors required. As shown above, R2 varies with the inverse square of $f_0$. This relationship desensitizes $f_0$ to R2's tolerance (by a factor of 2 incrementally), but it also implies that R2 has a wider range than $f_0$. ($R_Q$ and $R_{IN}$ also tend to scale with R2.) At high $f_0$ these resistors fall below 5k, heavily loading the outputs of the LTC1562 and leading to increased THD and other effects. At the other extreme, a lower $f_0$ limit of 10kHz reflects an arbitrary upper resistor limit of 1MΩ. The LTC1562's MOS input circuitry can accommodate higher resistor values than this, but junction leakage current from the input protection circuitry may cause DC errors.

The 2nd order transfer functions $H_{LP}(s)$, $H_{BP}(s)$ and $H_{HP}(s)$ (below) are all inverting so that, for example, at DC the lowpass gain is $-H_L$. If two such sections are cascaded, these phase inversions cancel. Thus, the filter in the application schematic on the first page of this data sheet is a dual DC preserving, noninverting, rail-to-rail lowpass filter, approximating two "straight wires with frequency selectivity."

Operational Filter is a trademark of Linear Technology Corporation.

## APPLICATIONS INFORMATION

### Highpass Option

If a capacitor of value $C_{IN}$ replaces the resistor $R_{IN}$, then a standard all-pole highpass response becomes available between $V_{IN}$ and the "BP" output.

$$H_{HP}(s) = \frac{-H_H s^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

Here, the passband gain $H_H = C_{IN}/C$ where C is the internal capacitance, nominally 159pF. The expressions for $f_0$ and Q remain as above.

### Two Bandpass Options

There are two distinct ways to obtain a bandpass response $H_{BP}(s)$ from the LTC1562. In the basic circuit of Figure 1, where the only external components are resistors, the BP output has a bandpass response from $V_{IN}$. Alternatively, with an input capacitor $C_{IN}$ replacing $R_{IN}$, the BP output has a highpass response as described above, but simultaneously the LP output now has a bandpass response, with the same $H_{BP}(s)$ form as above. The bandpass gain parameter becomes $H_B = (R_Q/R1)(C_{IN}/159pF)$ where again R1 = 10k. $f_0$ and Q are controlled by R2 and $R_Q$ as always.

### Relative Signal Swings

The signal swings in each 2nd order section must be scaled so that neither output overloads (saturates), even if it is not used as a signal output. (Filter literature often calls this the "dynamics" issue.) For the LTC1562, the ratio of peak signal swings, LP output to BP output, is approximately equal to the ratio,

$$\frac{\left|H_{LP}(j\omega_0)\right|}{\left|H_{BP}(j\omega_0)\right|} = \frac{(100kHz)}{f_0}$$

Thus the "LP" output of the LTC1562 tends to have the higher swing of the two when $f_0$ is below 100kHz, and "BP" the higher swing when $f_0$ is above 100kHz. When an unused output has a larger signal swing than the output of interest, the section's gain or input amplitude must be scaled to avoid overdriving the unused output. The LTC1562 can still be used with high performance in such situations as long as this constraint is followed.

The following cases are the most convenient because the relative-signal-swing issue does not arise: the unused output's swing is naturally the lower of the two.

Lowpass response (all-resistor form, "LP" output) with $f_0 < 100kHz$

Bandpass response (capacitor-input form, "LP" output) with $f_0 < 100kHz$

Bandpass response (all-resistor form, "BP" output) with $f_0 > 100kHz$

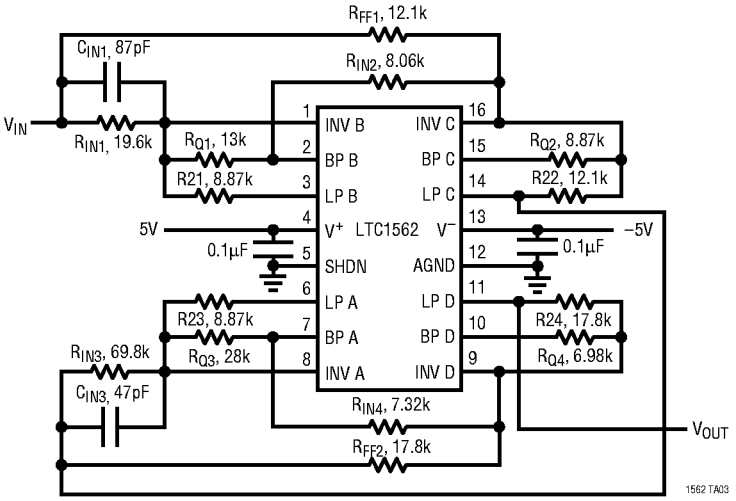
Highpass response (capacitor-input form, "BP" output) with $f_0 > 100kHz$

### Low Level or Wide Range Input Signals

The LTC1562 contains a built-in capability for low noise amplification of low level signals. The $R_{IN}$ resistor in each 2nd order section controls the block's gain. When set for unity passband gain, a 2nd order section can deliver an output signal more than 100dB above the noise level. If low level inputs require further dynamic range, reducing the value of $R_{IN}$ boosts the signal gain while reducing the input-referred noise. This feature can increase the SNR for low level signals. Varying or switching $R_{IN}$ ($C_{IN}$ for the highpass option) is also an efficient way to effect automatic gain control (AGC). From a system viewpoint, this technique boosts the ratio of maximum signal to minimum noise, for a typical 2nd order lowpass response (Q = 1, $f_0$ = 100kHz), to 118dB.

## TYPICAL APPLICATIONS (Pinout shown for the 16-pin PDIP)

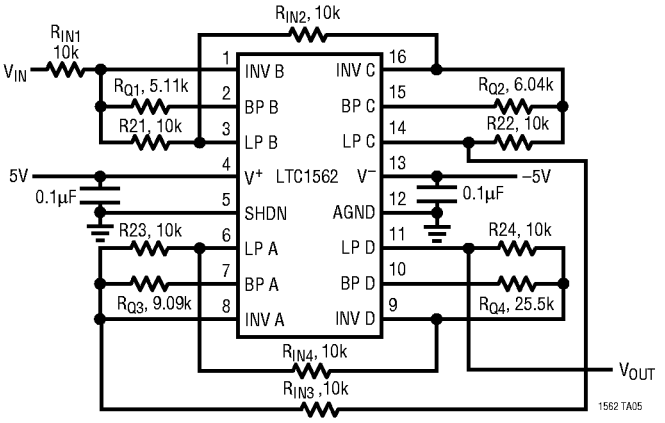
### 8th Order 100kHz Lowpass Elliptic Filter




ALL RESISTORS = 1% METAL FILM
$V_S$ = ±5V
TOTAL OUTPUT NOISE = 46µ$V_{RMS}$

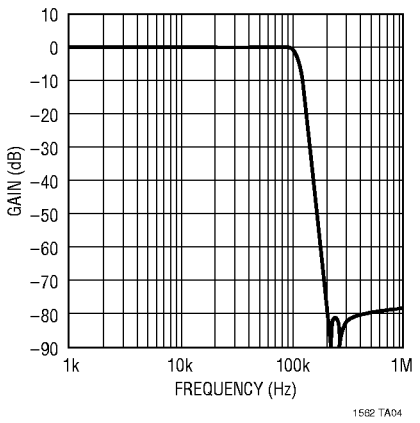
WITH $V_{IN}$ = 1.5$V_{RMS}$, $f_{IN}$ ≤ 30kHz
SIGNAL/(NOISE + THD) = 88dB
OUTPUT DC OFFSET = 5mV TYP

### 8th Order 100kHz Lowpass Butterworth Filter

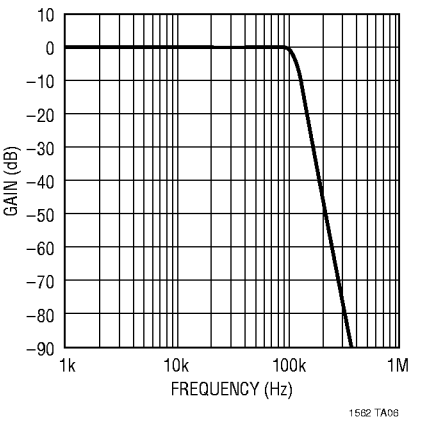



ALL RESISTORS = 1% METAL FILM
$V_S$ = ±5V
TOTAL OUTPUT NOISE = 40µ$V_{RMS}$
WITH $V_{IN}$ = 1.5$V_{RMS}$, SIGNAL/(NOISE + THD) ≅ 90dB
OUTPUT DC OFFSET = 10mV TYP

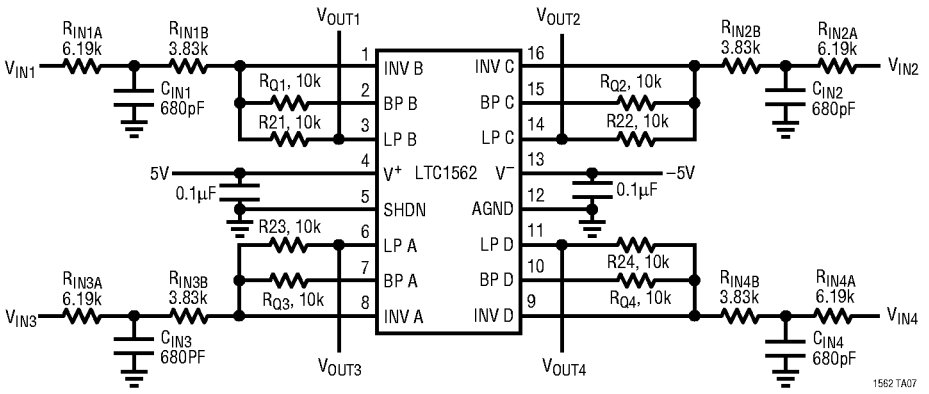
### Amplitude Response




### Amplitude Response



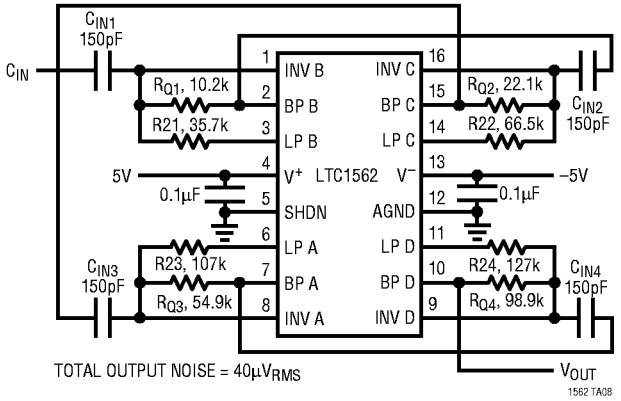

### Quad 3-Pole 100kHz Butterworth Lowpass Filter



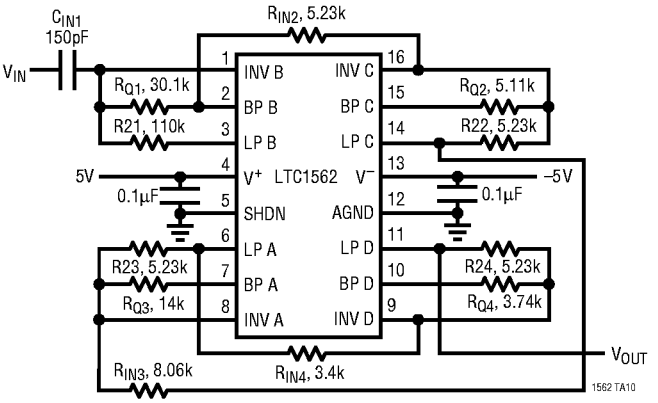

ALL RESISTORS = 1% METAL FILM
$V_S$ = ±5V

## TYPICAL APPLICATIONS (Pinout shown for the 16-pin PDIP)

**8th Order Highpass 0.05dB Ripple Chebyshev Filter**
**$f_{CUTOFF}$ = 30kHz**

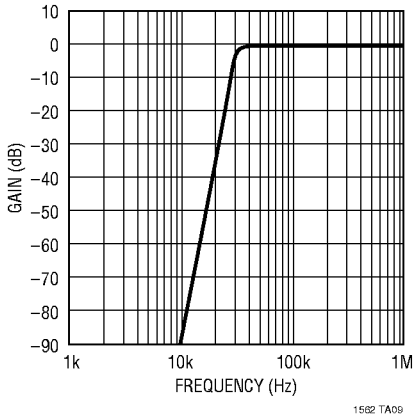



**2nd Order 30kHz Highpass Cascaded with 6th Order 138kHz Lowpass**

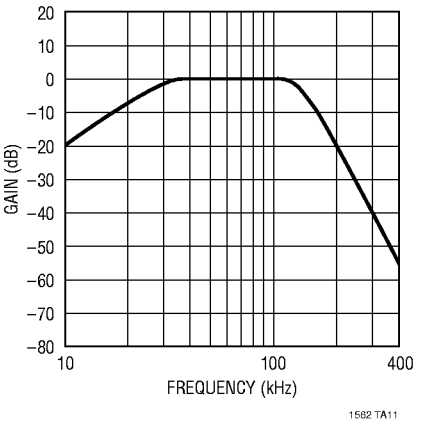



ALL RESISTORS = 1% METAL FILM

**Amplitude Response**




**Amplitude Response**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1560-1 | 5-Pole Elliptic Lowpass, $f_C$ = 1MHz/0.5MHz | No External Components, SO8 |



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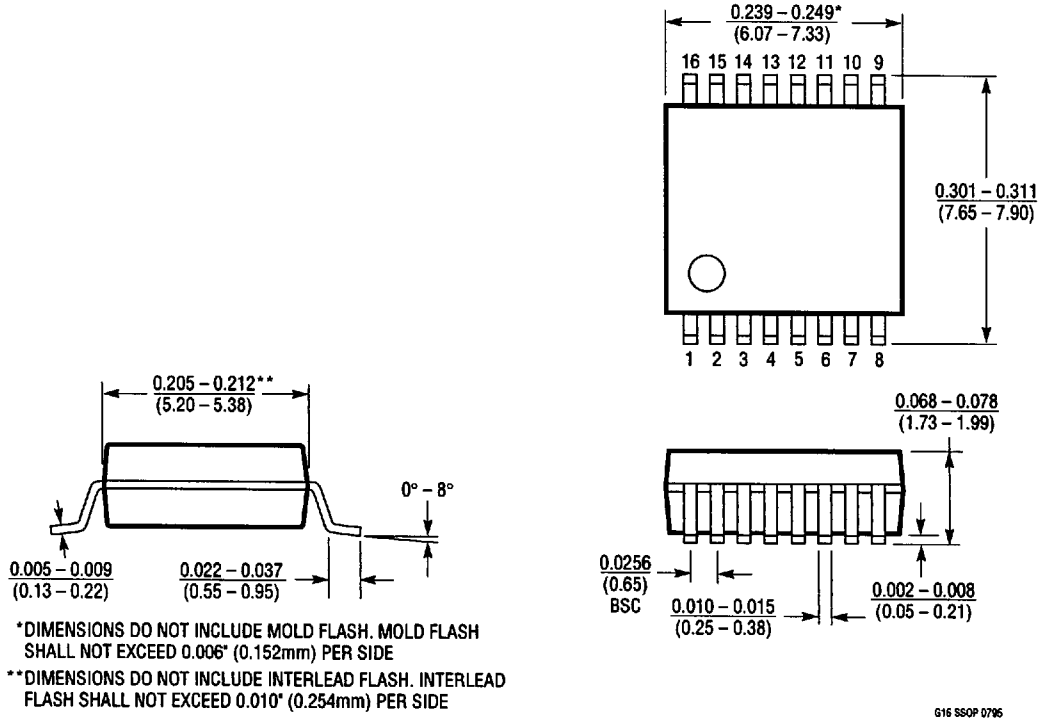
1562i LT/TP 0398 4K • PRINTED IN USA

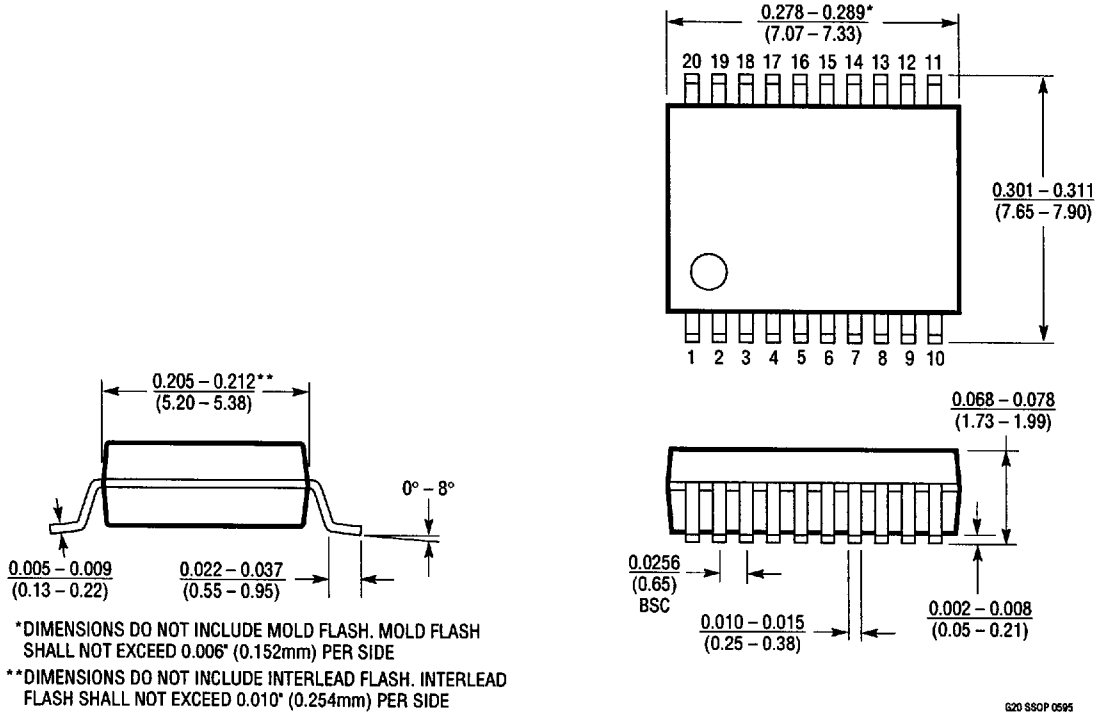
**G Package**
**16-Lead Plastic SSOP (0.209)**
(LTC DWG # 05-08-1640)




*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

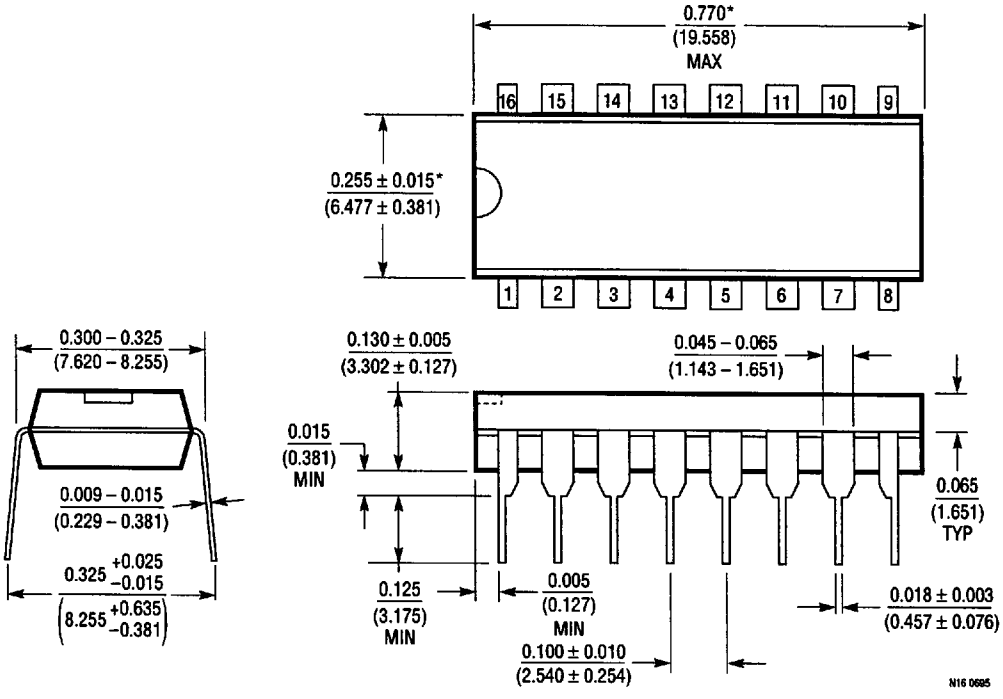
**G Package**
**20-Lead Plastic SSOP (0.209)**
(LTC DWG # 05-08-1640)




*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

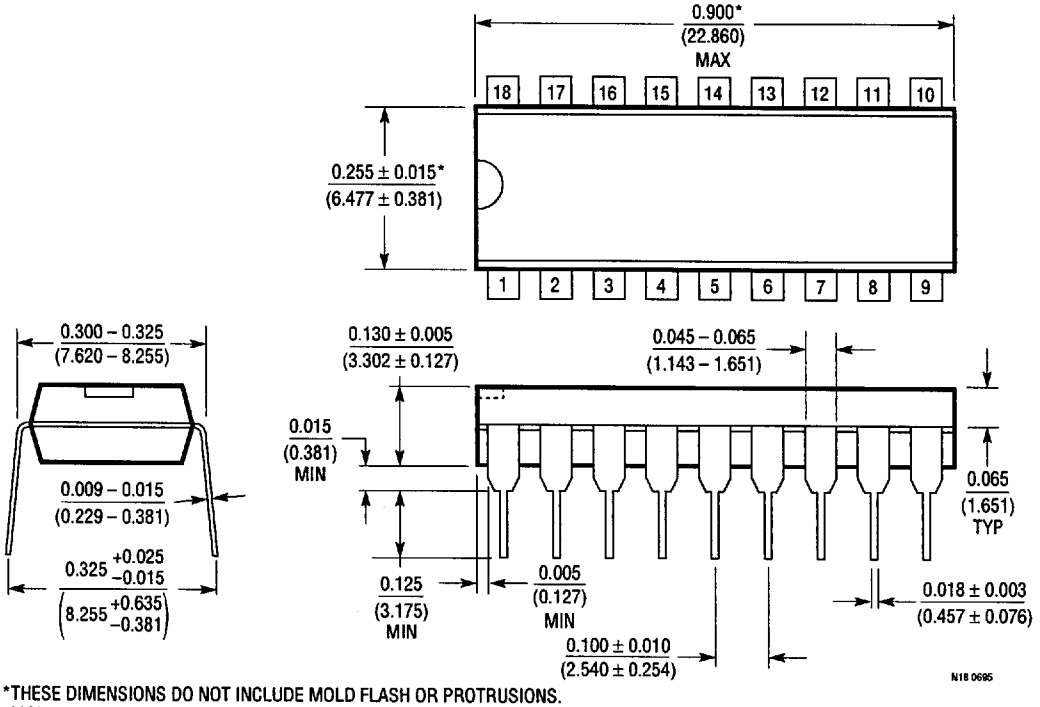
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

**N Package**
**16-Lead PDIP (Narrow 0.300)**
(LTC DWG # 05-08-1510)




*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

**N Package**
**18-Lead PDIP (Narrow 0.300)**
(LTC DWG # 05-08-1510)




*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)