Genesys Logic, Inc.

GL811E

USB 2.0 to ATA / ATAPI Bridge Controller

Datasheet
Revision 1.11
Nov. 27, 2003

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Revision History

Revision	Date	Description
1.00	06/13/2003	First formal release.
1.01	06/24/2003	Changed product name from GL811 to GL811E.
1.10	11/26/2003	1. Added some features in Chapter 2. 2. Added 64 pin LQFP data in pinouts, pin description and package dimension. 3. Added Chapter 8 “Ordering Infromation”.
1.11	11/27/2003	Changed pin# 38,39,21 name from IOADR0~2 to DA0~2.

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CHAPTER 1 GENERAL DESCRIPTION

The GL811E is a highly-compatible, low cost USB 2.0 to ATA / ATAPI bridge controller, which integrates Genesys Logic own design high speed UTMI (USB 2.0 Transceiver Macrocell Interface) transceiver.

As a one-chip solution which complies with Universal Serial Bus specification rev. 2.0 and ATA / ATAPI-6 specification rev 1.0, the GL811E can support various kinds of ATA / ATAPI device. There are totally 4 endpoints in the GL811E controller, Control (0), Bulk In (1), Bulk Out (2), and Interrupt (3). By complies with the USB Storage Class specification ver.1.0 (Bulk only protocol), the GL811E can support not only plug and play but also Windows XP/ 2000/ ME default driver.

The GL811E uses 12MHz crystal and slew-rate controlled pads to reduce the EMI issue. With 48-pin LQFP (9mmX9mm) package, the GL811E is the best cost/ performance solution to fit different situations in the USB 2.0 high speed storage class applications such as Hard Disk, CD-ROM, CD-R / RW and DVD-ROM.

CHAPTER 2 FEATURES

- Complies with Universal Serial Bus specification rev. 2.0.
- Complies with ATA/ATAPI-6 specification rev 1.0.
- Complies with USB Storage Class specification ver.1.0. (Bulk only protocol)
- Operating system supported: Win XP / 2000 / Me / 98 / 98SE; Mac OS 9.X / X.
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).
- Supports 4 endpoints: Control (0) / Bulk Read (1) / Bulk Write (2) / Interrupt (3).
- 64 / 512 bytes Data Payload for full / high speed Bulk Endpoint.
- Supports 8-bit/16-bit Standard PIO mode interface.
- Supports 16-bit Multiword DMA mode and Ultra DMA mode interface (Ultra 33 / 66).
- Embedded 7.5 MIPS RISC CPU.
- ROM size: 4k words; RAM size: 128 bytes.
- Supports Power Down mode and USB suspend indicator.
- Supports USB 2.0 TEST mode features.
- Supports 2 GPIO (GPIO5 & 6) for programmable AP (only for 64 pin package).
- Supports device power control for power on/off when running suspend mode (only for 64 pin package).
- Supports 32 bit and 48 bit LBA hard disk.
- Provides LED indicator for Full Speed and High Speed (only for 64 pin package).
- 12 MHz external clock to provide better EMI.
- 3.3V power input; 5V tolerance pad for IDE interface.
- Supports Wakeup ability.
- Available in 48-pin LQFP and 64-pin LQFP package.

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

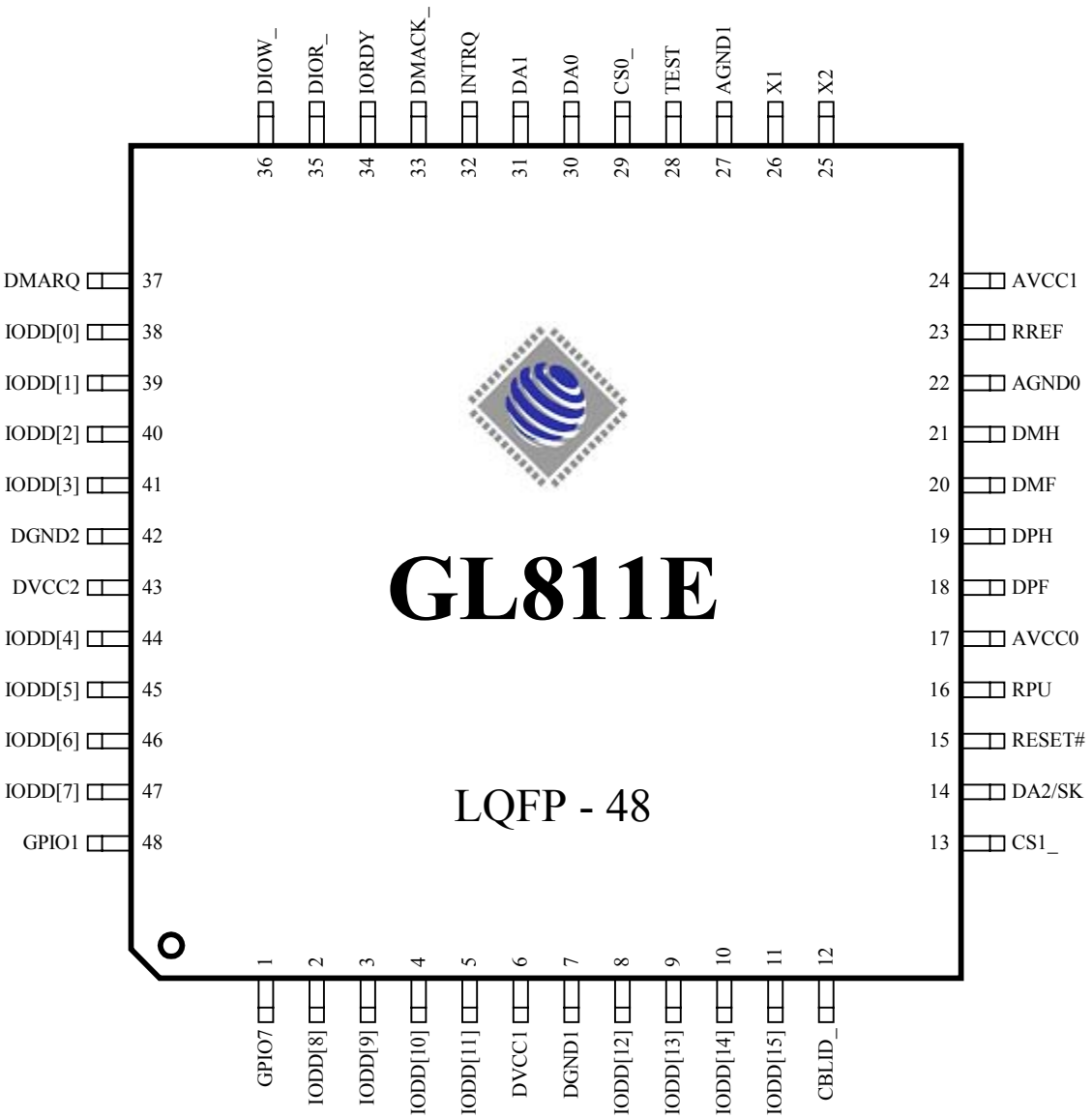


Figure 3.1 - 48 Pin LQFP Pinout Diagram

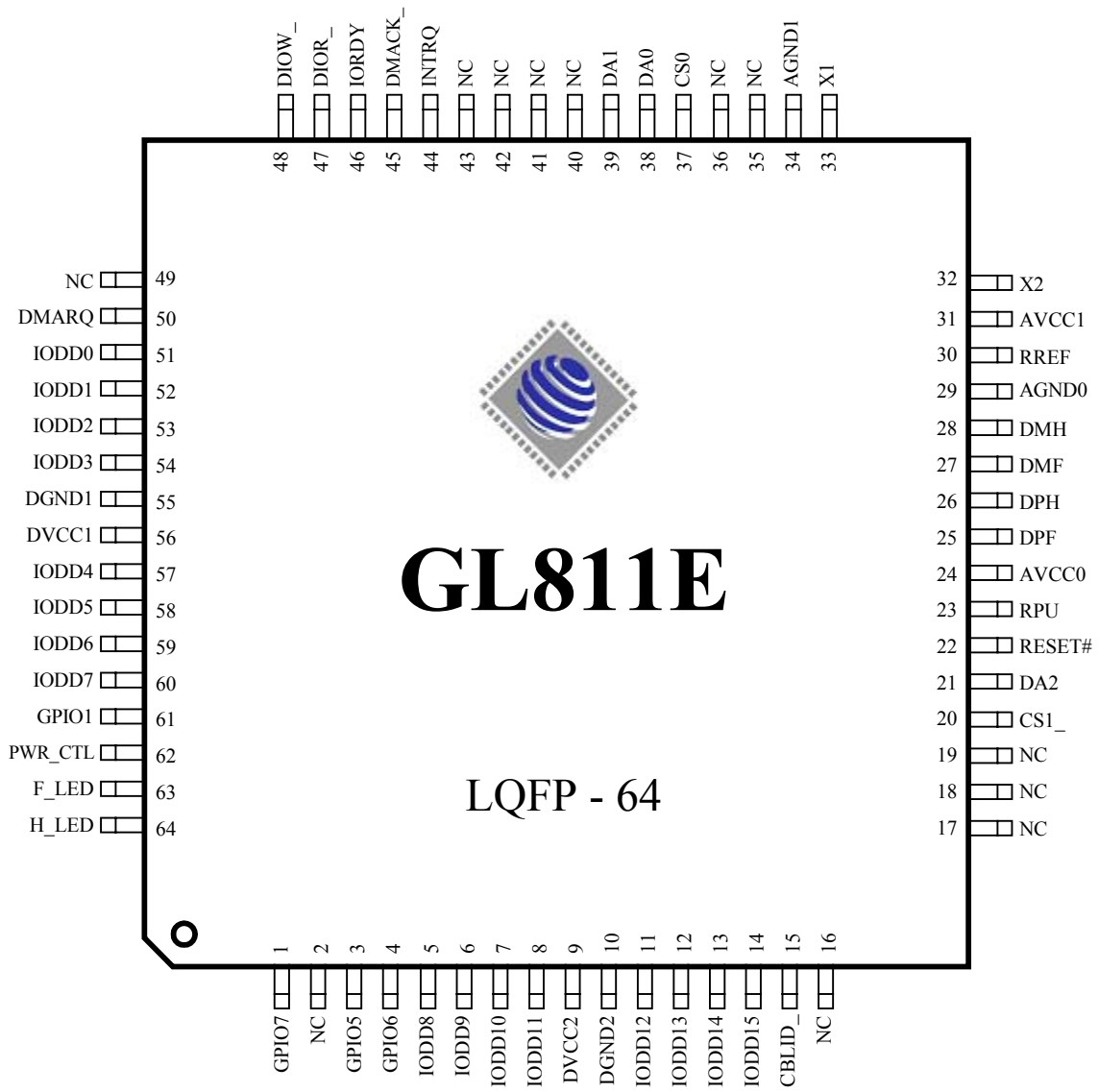


Figure 3.2 - 64 Pin LQFP Pinout Diagram

3.2 Pin Descriptions

Table 3.1 - Pin Descriptions

Pin Name	48Pin#	64 Pin#	I/O Type	Description
GPIO7	1	1	B (tri)	GPIO7 (**)
GPIO5~6	-	3,4	O	AP programmable
IODD[8:11]	2~5	5~8	B (tri)	IDE data bus 8~11
DVCC1~2	6,43	56,9	P	Digital VCC
DGND1~2	7,42	55,10	P	Digital ground
IODD[12:15]	8~11	11~14	B (tri)	IDE data bus 12~15
CBLID_	12	15	I (tri)	Cable select input
CS1_	13	20	O (tri)	Chip select 1
DA2/SK	14	-	O (tri)	IDE address 2 / Serial data clock for EEPROM
RESET#	15	22	I (pu)	Reset pin (***)
RPU	16	23	A	3.3v output
AVCC0~1	17,24	24,31	P	Analog VCC
DPF	18	25	B	Full speed DP
DPH	19	26	B	High speed DP
DMF	20	27	B	Full speed DM
DMH	21	28	B	High speed DM
AGND0~1	22,27	29,34	P	Analog ground
RREF	23	30	A	Reference resister connect (****)
X2	25	32	B	Crystal output
X1	26	33	I	Crystal input, 12Mhz
TEST	28	-	I (pd)	TEST mode input
CS0_	29	37	O (tri)	Chip select 0
DA0~1	30,31	38,39	O (tri)	IDE address 0~1
DA2	-	21	O (tri)	IDE address 2
INTRQ	32	44	I (tri)	IDE interrupt input
DMACK_	33	45	O (tri)	IDE acknowledge

IORDY	34	46	I (pu)	IDE ready
DIOR_	35	47	O (tri)	IDE read signal
DIOW_	36	48	O (tri)	IDE write signal
DMARQ	37	50	I (pd)	IDE request
IODD[0:3]	38~41	51~54	B (tri)	IDE data bus 0~3
IODD[4:7]	44~47	57~60	B (tri)	IDE data bus 4~7
GPIO1	48	61	B (tri)	GPIO1
PWR_CTL	-	62	O	Power control
F_LED	-	63	O	Full speed LED
H_LED	-	64	O	High speed LED
NC	-	2,16~19, 35,49,	-	No connection

(*) The different of I/O 8 type from I/O 16 type is the typical drive current. The typical drive current of I/O 8 type is 8 mA, and for I/O pad 16 is 16 mA.
(**) When operating in default mode: GPIO7 is the ATA/ ATAPI reset input,
(***) When Reset pin is pulled low, the IDE bus will be in tri-state.
(****) RREF must be connected with a 510 ohm resister to ground.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up
	tri	Tri-state

CHAPTER 4 BLOCK DIAGRAM

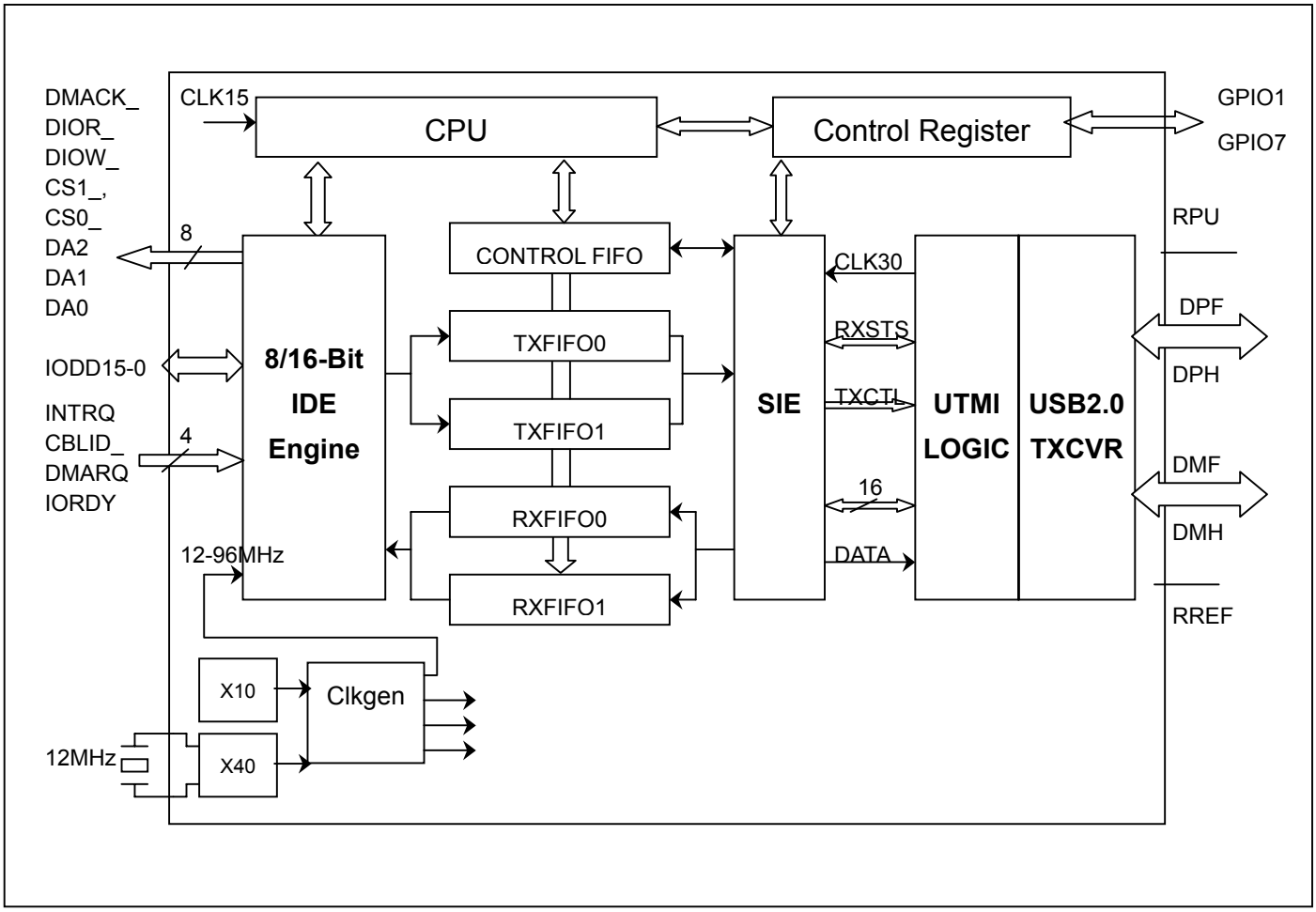


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

5.1 USB 2.0 TXCVR

The USB 2.0 Transceiver is the analog circuitry to handle the USB HS/FS signaling.

5.2 UTMI (USB 2.0 Transceiver Macrocell Interface) Logic

The UTMI Logic is compliant to Intel's UTMI specification 1.01. This block handles the low level USB protocol and signaling. The major jobs of UTMI Logic is data and clock recovery, NRZI encoding/decoding, Bit Stuffing/De-stuffing, USB2.0 test modes supporting and serial / parallel conversion.

5.3 SIE (Serial Interface Engine)

The SIE contains the USB packet ID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

5.4 PLL

10XPLL provides the 120MHz clock output for UTMI Logic block. UTMI operates in 120MHz for USB HS data processing. 40XPLL block will provide 480MHz for USB HS data transmission.

5.5 CLKGEN

CLKGEN is the clock generator block for the logic blocks. It generates 15MHz clock for micro controller, 12MHz for PIO mode, 48MHz for MDMA mode, 96MHz for UDMA mode, and 30MHz clock for UTMI, SIE, and FIFO.

5.6 CPU

The CPU is the control center of GL811E. It's an 8-bit micro controller operating in 15MHz, 7.5 MIPS. After receiving a USB command, it decodes the host command, then it re-assigns tasks to the IDE engine, GPIO, FIFO, and response proper data/status to USB host.

5.7 IDE Engine

The IDE engine is extended from standard ATA / ATAPI protocol. It supports PIO mode, multiword DMA mode, and ultra DMA mode data transfers.

5.8 FIFOs

Control FIFO is used as Control Read / Write FIFO. *TXFIFO0 / TXFIFO1* are two sets of 512-byte ping-pong FIFO for Bulk Read endpoint. It buffers data from IDE engine, and re-direct to USB SIE logic. *RXFIFO0 / RXFIFO1* are two sets of 512-byte ping-pong FIFO for Bulk Write endpoint. It buffers data from USB SIE logic, and re-direct to IDE engine.

5.9 Control Registers

Control Register configures GL811E to proper operation. For example, CPU can set register to generate wakeup event, enter suspend, transmits proper USB packet to host.

5.10 ATA/ATAPI

The GL811E complies with ATA/ATAPI-6 specification rev. 1.0. Please refer to the specifications for more information.

5.11 USB 2.0

The GL811E complies with Universal Serial Bus specification rev. 2.0, and it integrates Genesys Logic own design UTMI transceiver that fully complies with the USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC supply voltage	+3.0	+3.6	V
V_I	DC input voltage	-0.3	V_{CC} + 0.3	V
$V_{I/O}$	DC input voltage range for I/O	-0.3	V_{CC} + 0.3	V
$V_{AI/O}$	DC input voltage for USB D+/D- pins	-0.3	V_{CC} + 0.3	V
V_{ESD}	Static discharge voltage	4000		V
T_A	Ambient Temperature	0	100	°C

6.2 Temperature Conditions

Table 6.2 - Temperature Conditions

Item	Value
Storage Temperature	-50°C ~ 150 °C
Operating Temperature	0 °C ~ 70 °C

6.3 DC Characteristics

6.3.1 I/O 8 Type digital pins (For pad type I/O 8 @ V_{CC}=3.6V)

Table 6.3 - I/O 8 Type digital pins (For pad type I/O 8 @ V_{CC}=3.6V)

Parameter	Min.	Typ.	Max.	Unit
Current sink @ V_{OL} = 0.4V	7.79	10.83	14.09	mA
Current output @ V_{OH} = 2.4V (TTL high)	16.36	19.87	23.39	mA
Falling slew rate at 30 pF loading capacitance	0.26	0.50	0.80	V/ns
Rising slew rate at 30 pF loading capacitance	0.30	0.57	0.91	V/ns
Input high threshold voltage			1.64	V
Input low threshold voltage	1.36			V
Hysteresis voltage	-	0	-	V
Leakage current for pads with internal pull up or pull down resistor			46	μA
Pad internal pull down resister	51K	105K	152K	Ohms
Pad internal pull up resister	85K	168K	251K	Ohms
Supply current			109	mA

6.3.2 I/O 16 Type digital pins (For pad type I/O 16 @ V_{CC}=3.6V)

Table 6.4 - I/O 16 Type digital pins (For pad type I/O 16 @ V_{CC}=3.6V)

Parameter	Min.	Typ.	Max.	Unit
Current sink @ V_{OL} = 0.4V	16.20	21.90	27.68	mA
Current output @ V_{OH} = 2.4V (TTL high)	24.13	29.46	34.80	mA
Falling slew rate at 30 pF loading capacitance	0.51	0.93	1.35	V/ns
Rising slew rate at 30 pF loading capacitance	0.46	0.83	1.27	V/ns
Input high threshold voltage			2.15	V
Input low threshold voltage	0.89			V
Pad internal pull down resister	51K	105K	152K	Ohms

6.3.3 D+/ D- (For pad type u20mia @ V_{CC}=3.6V)

Table 6.5 - D+/ D- (For pad type u20mia @ V_{CC}=3.6V)

Parameter	Min.	Typ.	Max.	Unit
D+/D- static output LOW (R_L of 1.5K to V_{CC})	0		0.3	V
D+/D- static output HIGH (R_L of 15K to GND)	2.8		3.6	V
Differential input sensitivity	0.2			V
Single-ended receiver threshold	0.8		2.0	V
Transceiver capacitance			20	pF
Hi-Z state data line leakage	-10		+10	μA
Driver output resistance	28		43	Ohms

6.3.4 Switching Characteristics

Table 6.6 - Switching Characteristics

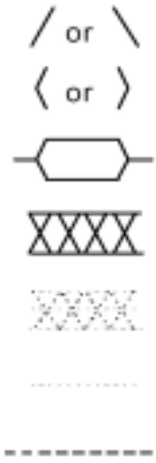
Parameter	Min.	Typ.	Max.	Unit
X1 crystal frequency	11.97	12	12.03	MHz
X1 cycle time		83.3		ns
D+/D- rise time with 50pF loading	4		20	ns
D+/D- fall time with 50pF loading	4		20	ns

6.4 AC Characteristics- ATA/ ATAPI

The GL811E complies with ATA / ATAPI-6 specification rev 1.0, which supports following data transfer modes:

1. PIO (Programmed Input/ Output) data transfer:
   PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.
2. DMA (Direct Memory Access) data transfer:
   DMA data transfer means of data transfer between device and host memory without host processor intervention.
   - Multiword DMA: Multiword DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED and PACKET commands. When a Multiword DMA transfer is enabled as indicated by IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data, this data transfer protocol shall be used for the data transfers associated with these commends. (Please refer to the ATA / ATAPI-6 specification rev 1.0 for more information.)
   - Ultra DMA: Ultra DMA Is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED and PACKET commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. (Please refer to the ATA / ATAPI-6 specification rev 1.0 for more information.)

Following listed the symbols and their respective definitions that are used in the timing diagram:

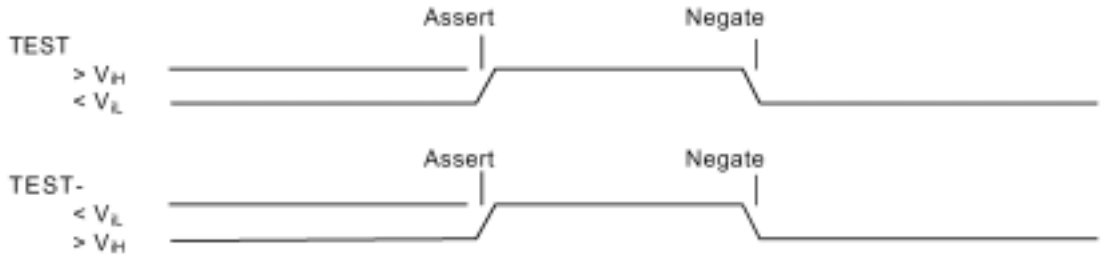


- Signal transition (asserted or negated)
- Data transition (asserted or negated)
- Data valid
- Undefined but not necessarily released
- Asserted, negated or released
- Released
- The “other” condition if a signal is shown with no change

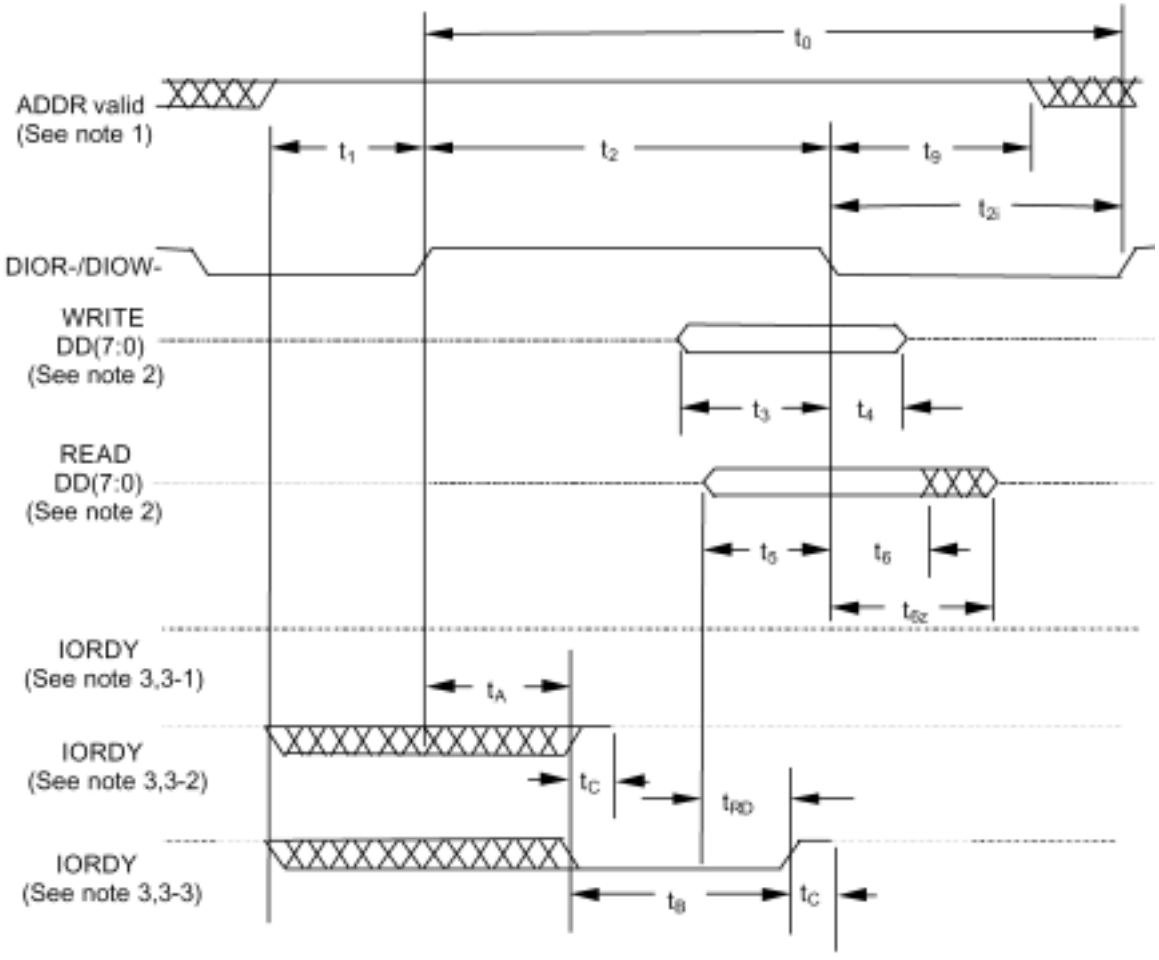
All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted. The following illustrates the representation of a signal named Test going from negated to asserted and back to negated, based on the polarity of the signal.



6.4.1 Register Transfers



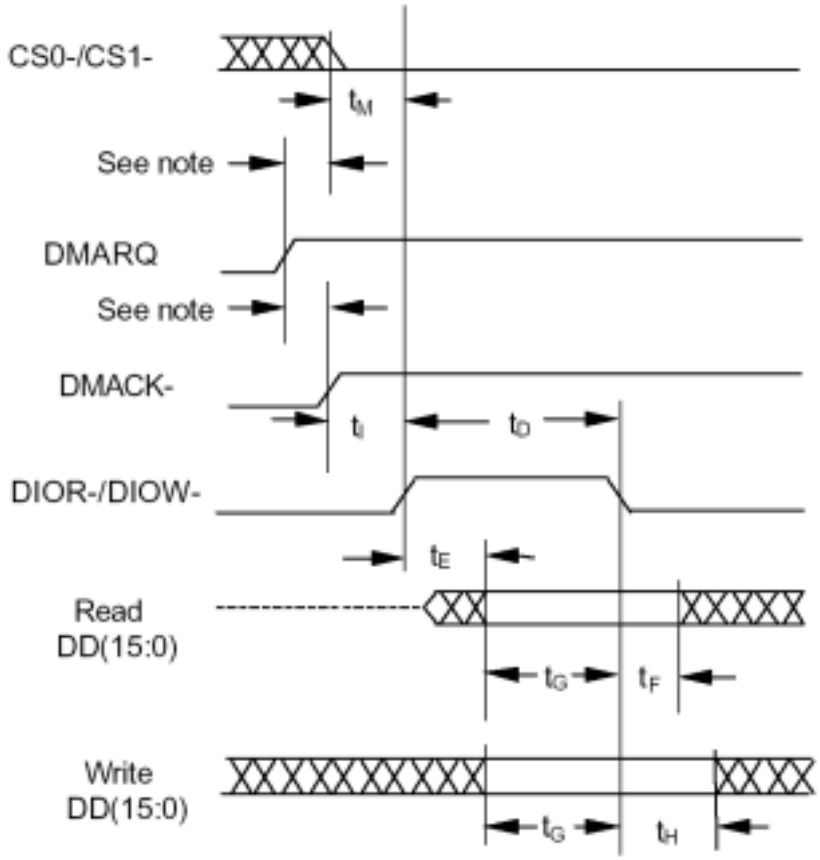
Notes:

1. Device address consists of signals CS0_, CS1_ and DA(2:0).
2. Data consists of IODD(7:0).
3. The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR_ or DIOW_. The assertion and negation of IORDY are described as following:
   3.1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
   3.2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
   3.3 Device negates IORDY before t_A, IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is released. For cycles where a wait is generated and DIOR_ is asserted, the device shall read data on IODD(0:7) for t_{RD} before asserting IORDY.
4. DMACK_ shall remain negated during a register transfer.

Register transfer timing parameters		Timing (ns)
t_0	Cycle time	2000
t_1	Address valid to DIOR_/ DIOW_ setup	1000
t_2	DIOR_/ DIOW_ pulse width 8-bit	300
t_{2i}	DIOR_/ DIOW_ recovery time	900
t_3	DIOW_ data setup	80
t_4	DIOW_ data hold	40
t_5	DIOR_ data setup	-
t_6	DIOR_ data hold	-
t_{6Z}	DIOR_ data tristate	-
t_9	DIOR_/ DIOW_ to address valid hold	900
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	
t_A	IORDY Setup time	-
t_B	IORDY Pulse Width	-
t_C	IORDY assertion to release (max)	-

6.4.2 Multiword DMA data transfer

Register transfer timing parameters		Timing (ns)
t_0	Cycle time	120
t_D	DIOR_/ DIOW_ asserted pulse width	80
t_E	DIOR_ data access	-
t_F	DIOR_ data hold	-
t_G	DIOR_/ DIOW_ data setup	40
t_H	DIOW_ data hold	18
t_I	DMACK to DIOR_/ DIOW_ setup	18
t_J	DIOR_/ DIOW_ to DMACK hold	20
t_{KR}	DIOR_ negated pulse width	36
t_{KW}	DIOW_ negated pulse width	36
t_{LR}	DIOR_ to DMARQ delay	-
t_{LW}	DIOW_ to DMARQ delay	-
t_M	CS(1:0) (max) valid to DIOR_/ DIOW_	36
t_N	CS(1:0) hold	18
t_Z	DMACK_ to read data released	-



Note:
The host shall not assert DMACK_ or negate both CS0_ and CS1_ until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK_ or the negation of both CS0_ and CS1_ is not defined.

Figure 6.1 - Initiating a Multiword DMA Data Burst

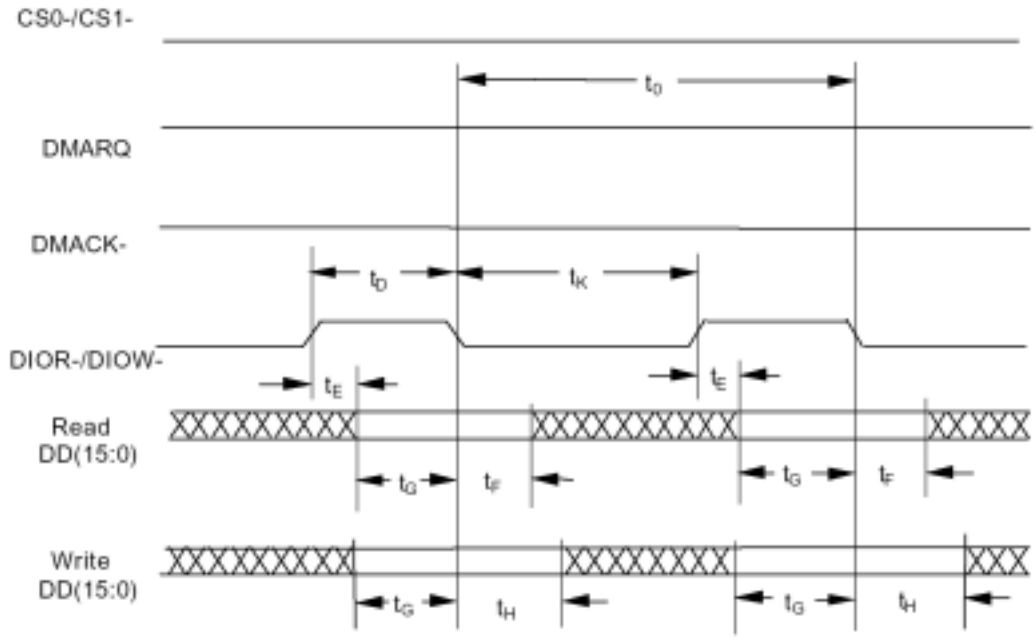
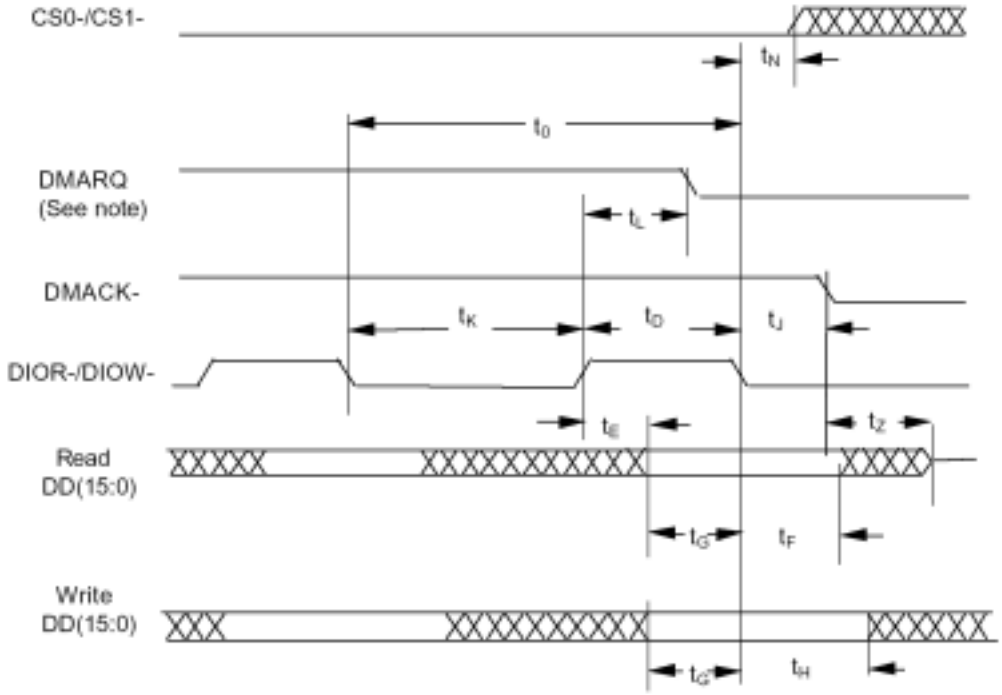
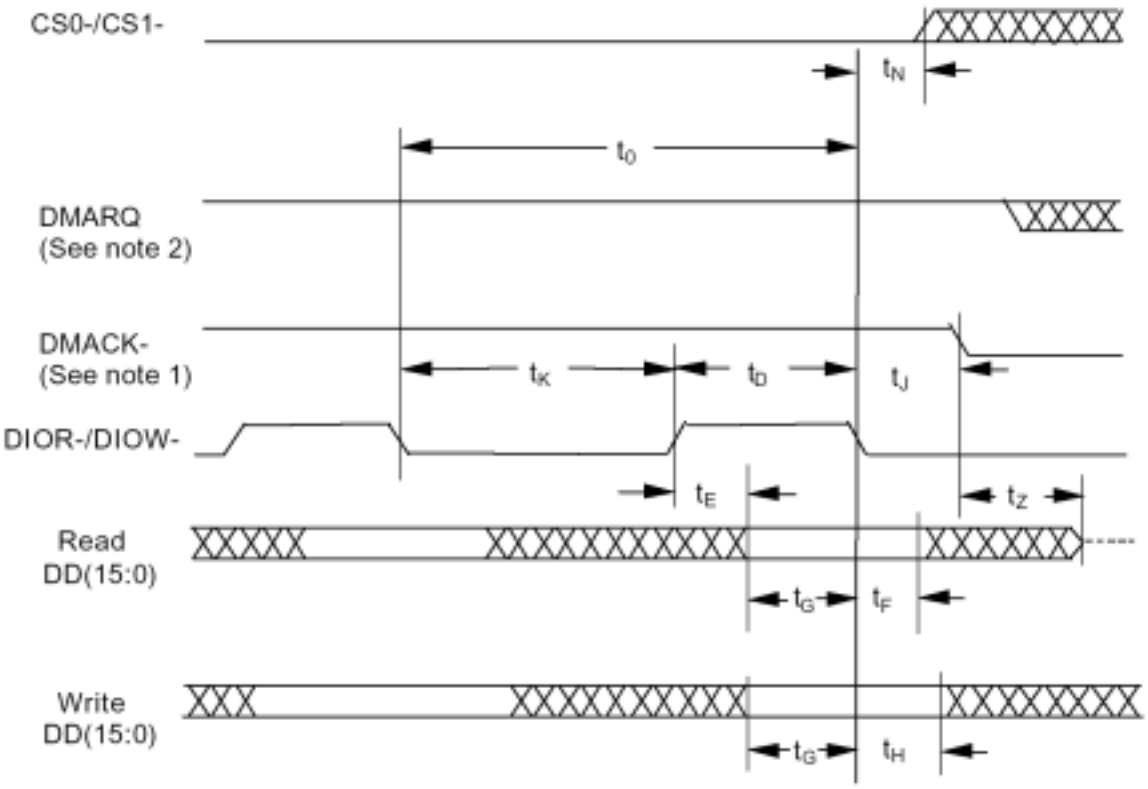


Figure 6.2 - Sustaining a Multiword DMA Data Burst



Note:
To terminate the data burst, the Device shall negate DMARQ within the t_L of the assertion of the current DIOR_ or DIOW_ pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR_ or DIOW_ pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation.

Figure 6.3 - Device Terminating a Multiword DMA Data Burst



Note:

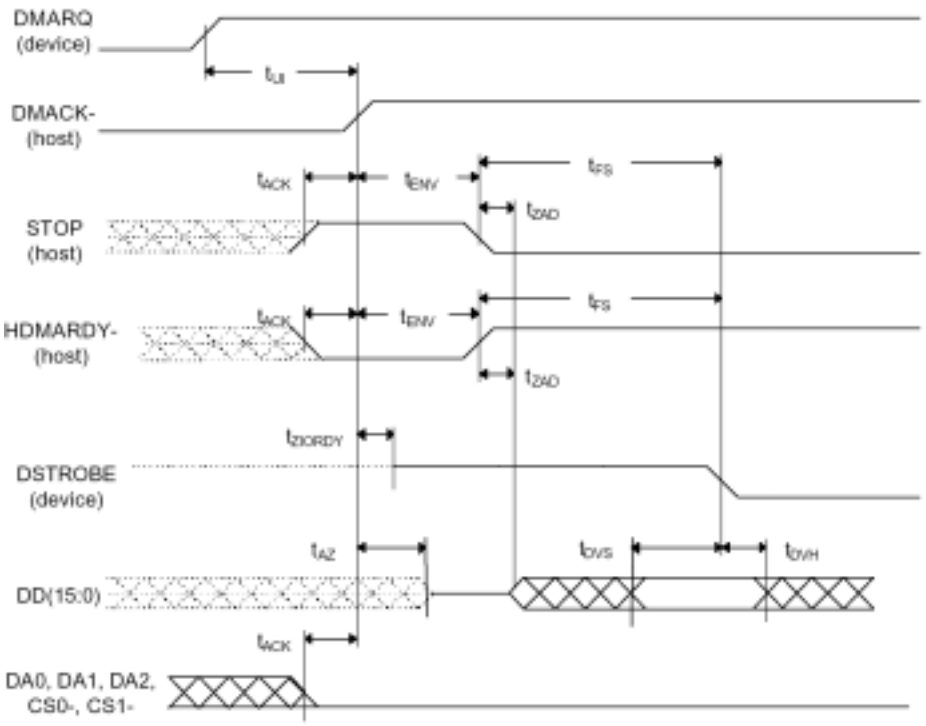
1. To terminate the transmission of a data burst, the Host shall negate DMACK_ within the specified time after a DIOR_ or DIOW_ pulse. No further DIOR_ or DIOW_ pulses shall be asserted for this burst.
2. If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK_ or may negate DMARQ at any time after detecting that DMACK_ has been negated.

Figure 6.4 - Host terminating a Multiword DMA Data Burst

6.4.3 Ultra DMA data transfer

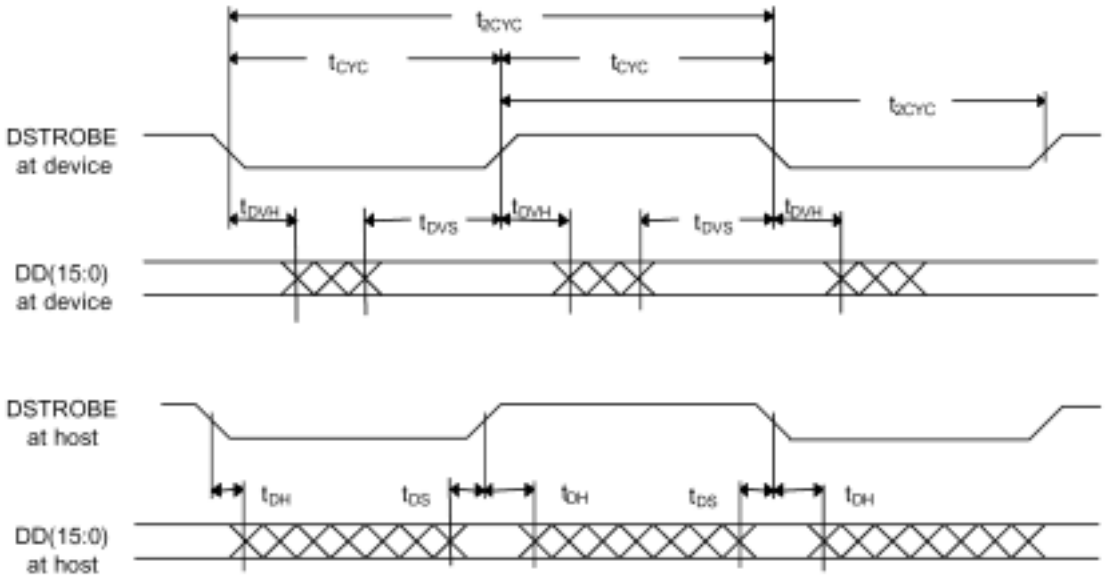
Table 6.7 - Ultra DMA data burst timing requirements

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Comment
	min	max	min	max	min	max	min	max	Min	max	
$t_{2CYCTYP}$	240		160		120		90		60		Typical sustained average two cycle time
t_{CYC}	112		73		54		39		25		Cycle time allowing for asymmetry and clock variations
t_{2CYC}	230		154		115		86		57		Two cycle time allowing for clock variations
t_{DS}	15		10		7		7		5		Data setup time at recipient
t_{DH}	5		5		5		5		5		Data hold time at recipient
t_{DVS}	70		48		30		20		6		Data valid setup time at sender
t_{DVH}	6		6		6		6		6		Data valid hold time at sender
t_{FS}	0	230	0	200	0	170	0	130	0	120	First STORBE time
t_{LI}	0	150	0	150	0	150	0	100	0	100	Limited interlock time
t_{MLI}	20		20		20		20		20		Interlock time with minimum
t_{UI}	0		0		0		0		0		Unlimited interlock time
t_{AZ}		10		10		10		10		10	Maximum time allowed for output drivers to release
t_{ZAH}	20		20		20		20		20		Minimum delay time required for output
t_{ZAD}	0		0		0		0		0		Drivers to assert or negate
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Envelope time
t_{SR}		50		30		20		NA		NA	STROBE to DMARDY_ time
t_{RFS}		75		70		60		60		60	Ready to final STROBE time
t_{RP}	160		125		100		100		100		Minimum time to assert STOP or negate DMARQ
t_{IORDYZ}		20		20		20		20		20	Maximum time before releasing IORDY
t_{ZIORDY}	0		0		0		0		0		Minimum time before driving STROBE
t_{ACK}	20		20		20		20		20		Setup and hold times for DMACK_
t_{SS}	50		50		50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP



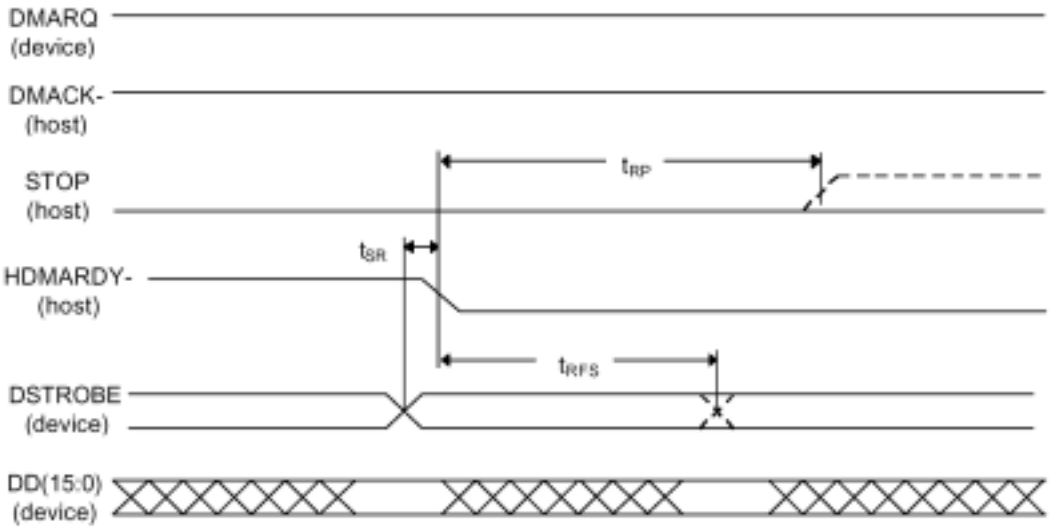
Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are not in efficient until DMARQ and DMACK are asserted.

Figure 6.5 - Initiating an Ultra DMA Data-In Burst



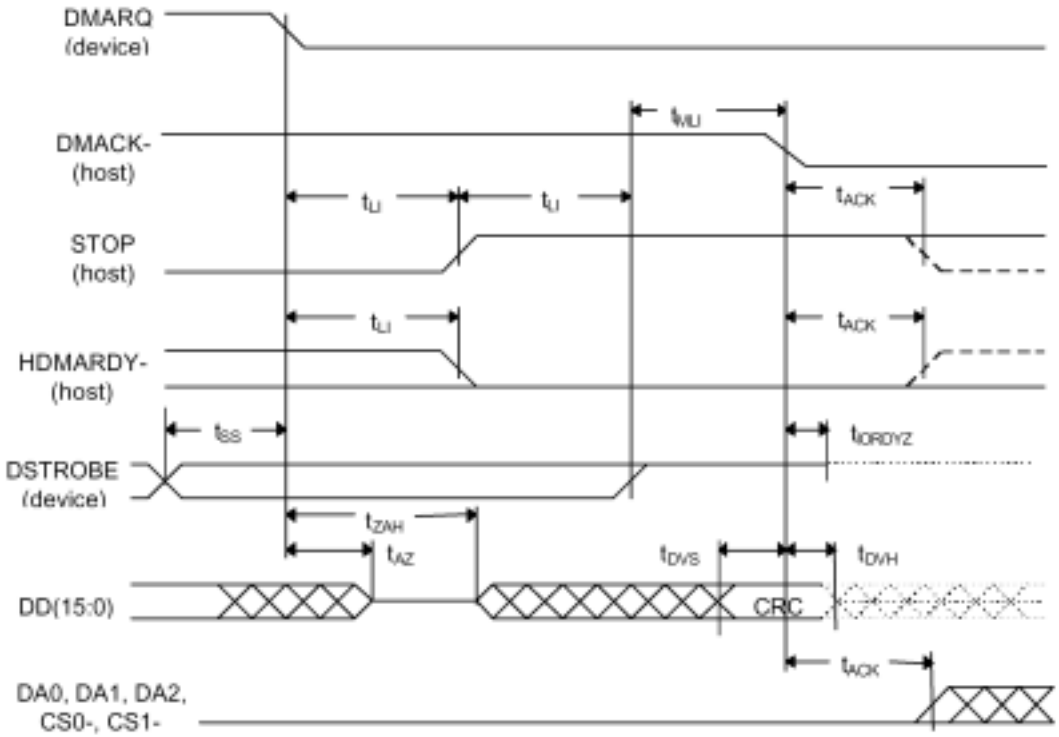
Notes:
IODD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 6.6 - Sustained Ultra DMA Data-In Burst



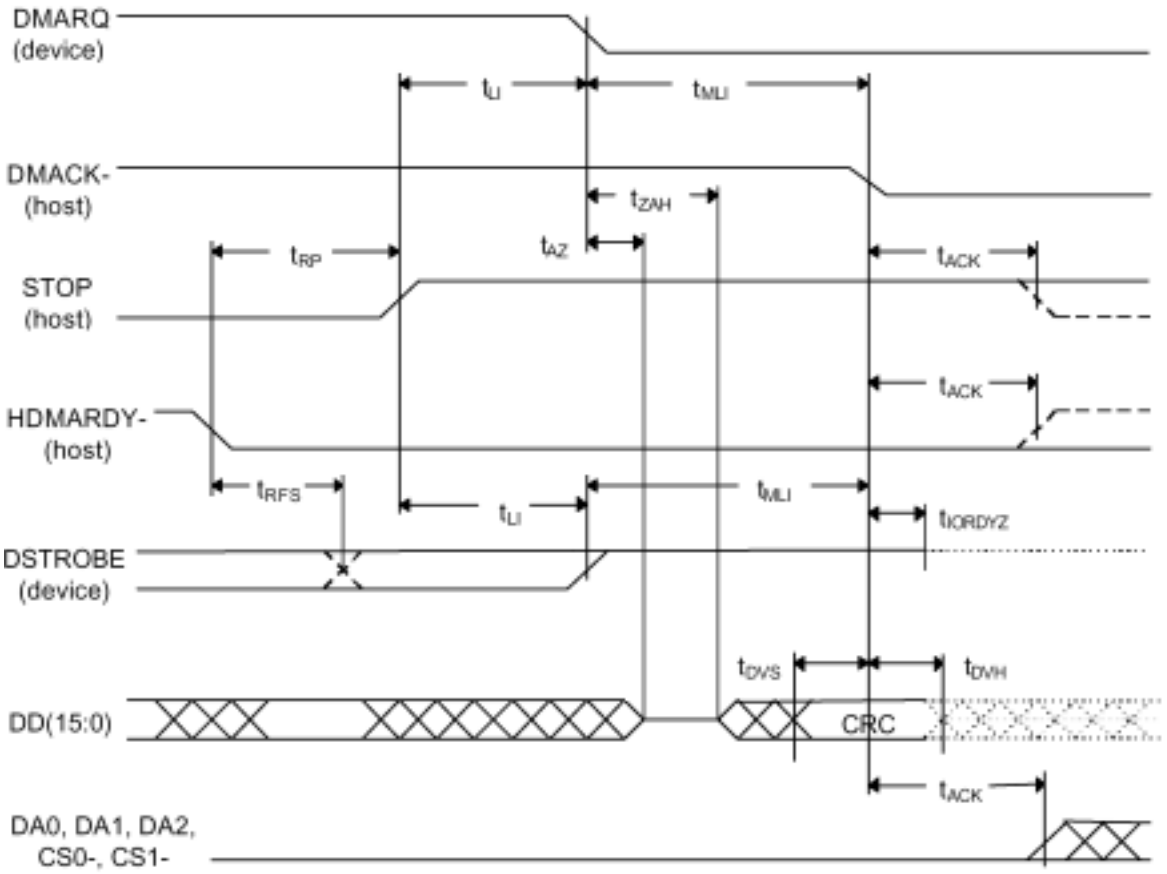
Notes:
1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after HDMARDY_ is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the device.

Figure 6.7 - Host Pausing an Ultra DMA Data-In Burst



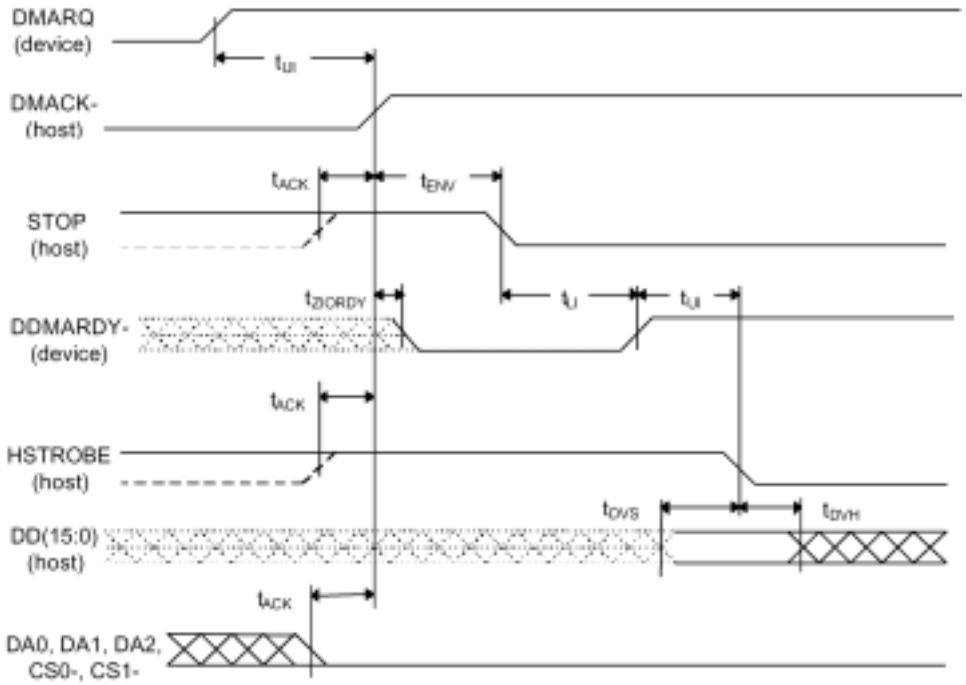
Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.8 - Device Terminating an Ultra DMA Data-In Burst



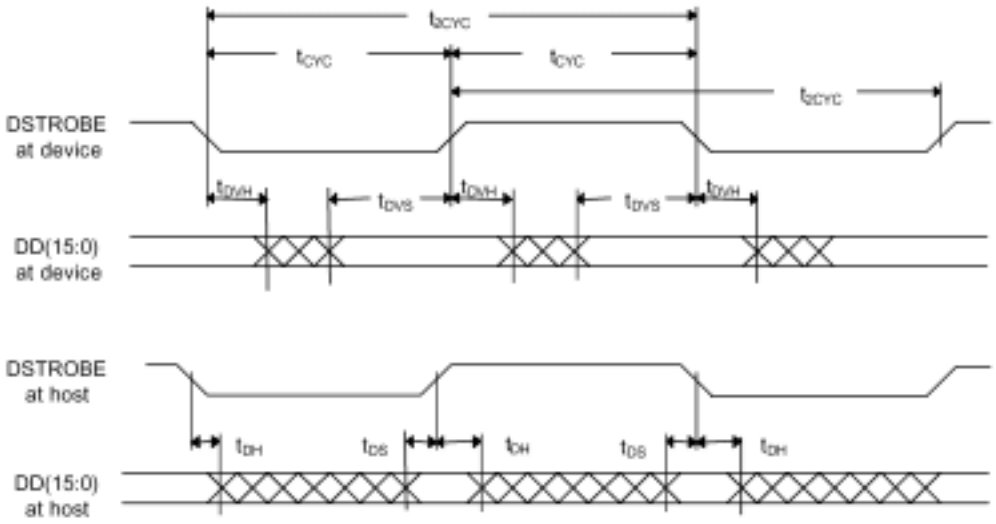
Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.9 - Host Terminating an Ultra DMA Data-In Burst



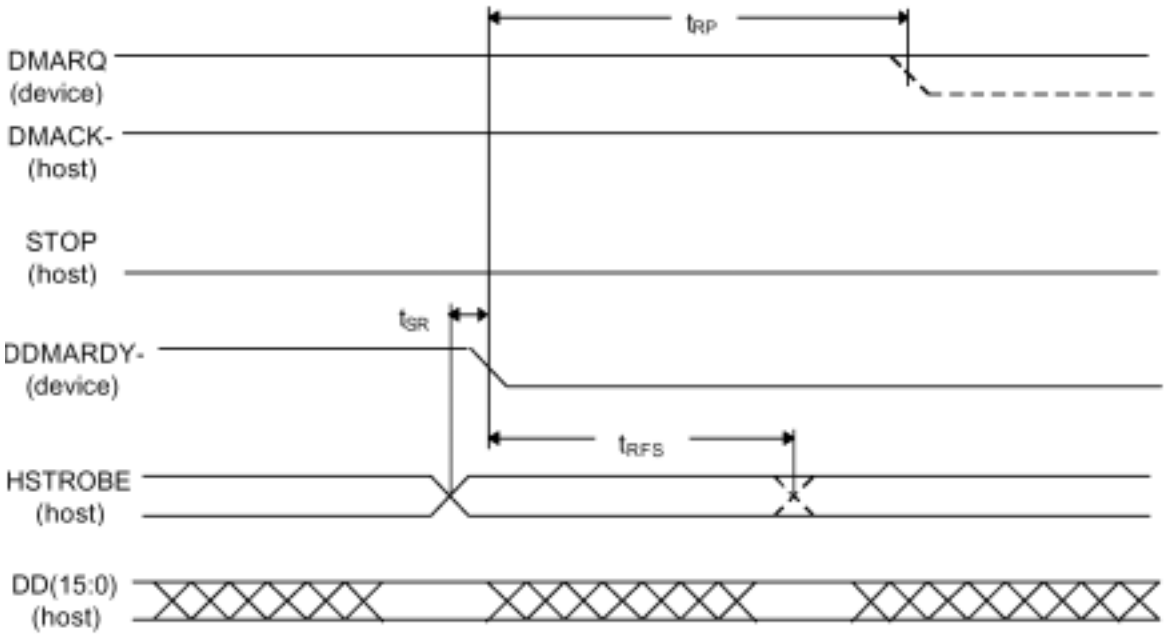
Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 6.10 - Initiating an Ultra DMA Data-Out Burst



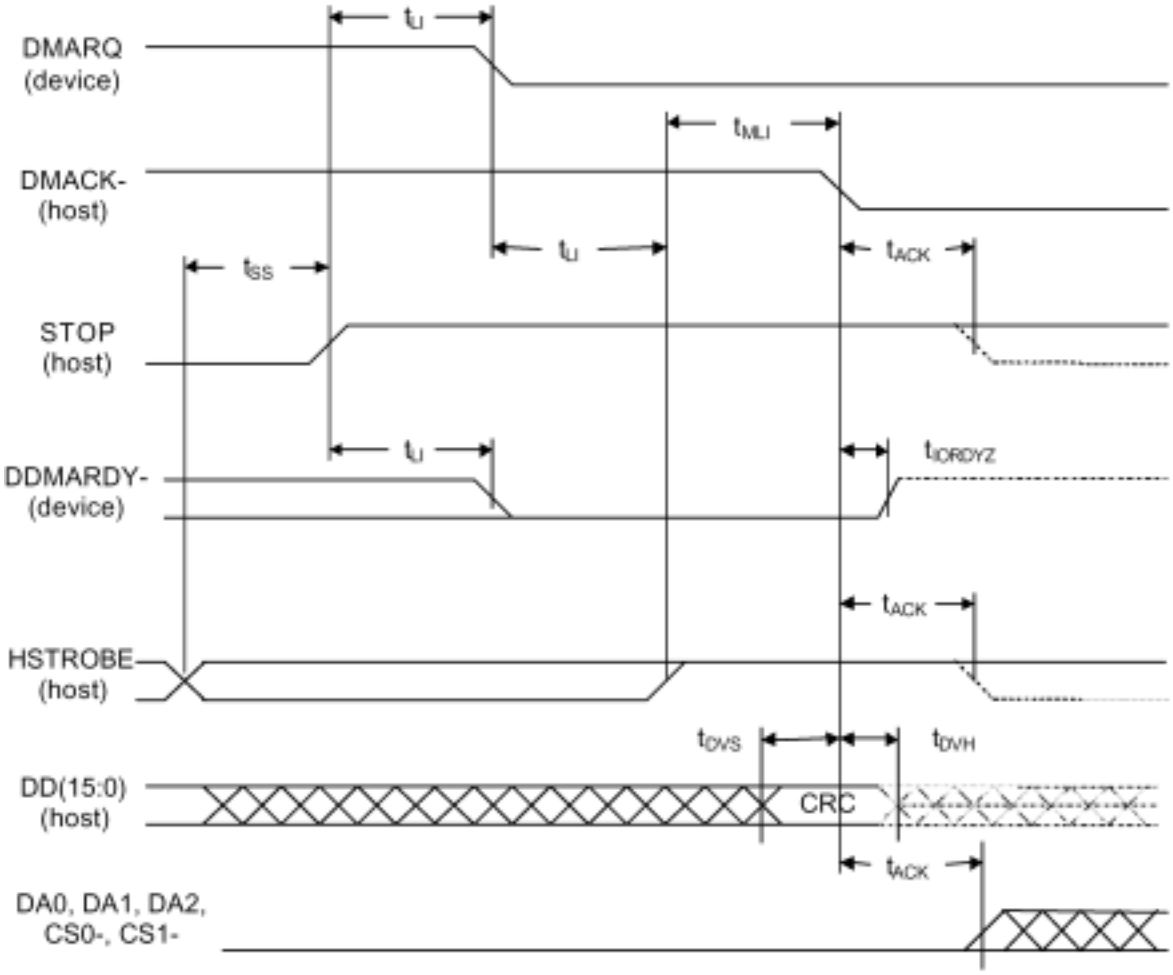
Notes:
IODD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the devicet until some time after they are driven by the host.

Figure 6.11 - Sustained Ultra DMA Data-Out Burst



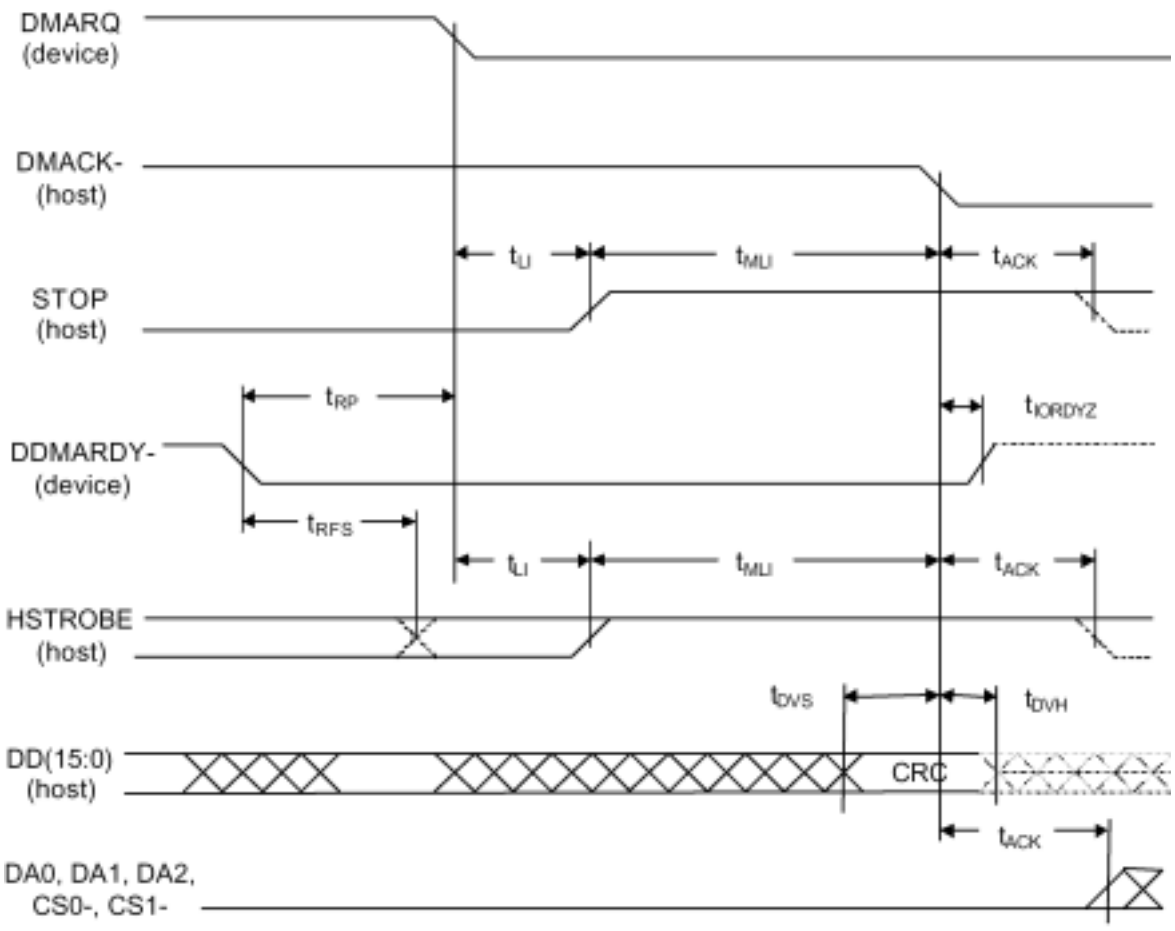
Notes:
1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after DDMARDY_ is negated.
2. If the t_{SR} timing is not satisfied, the device may receive zero, one, or two more data words from the host.

Figure 6.12 - Device Pausing an Ultra DMA Data-Out Burst



Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.13 - Host terminating an Ultra DMA data-out burst



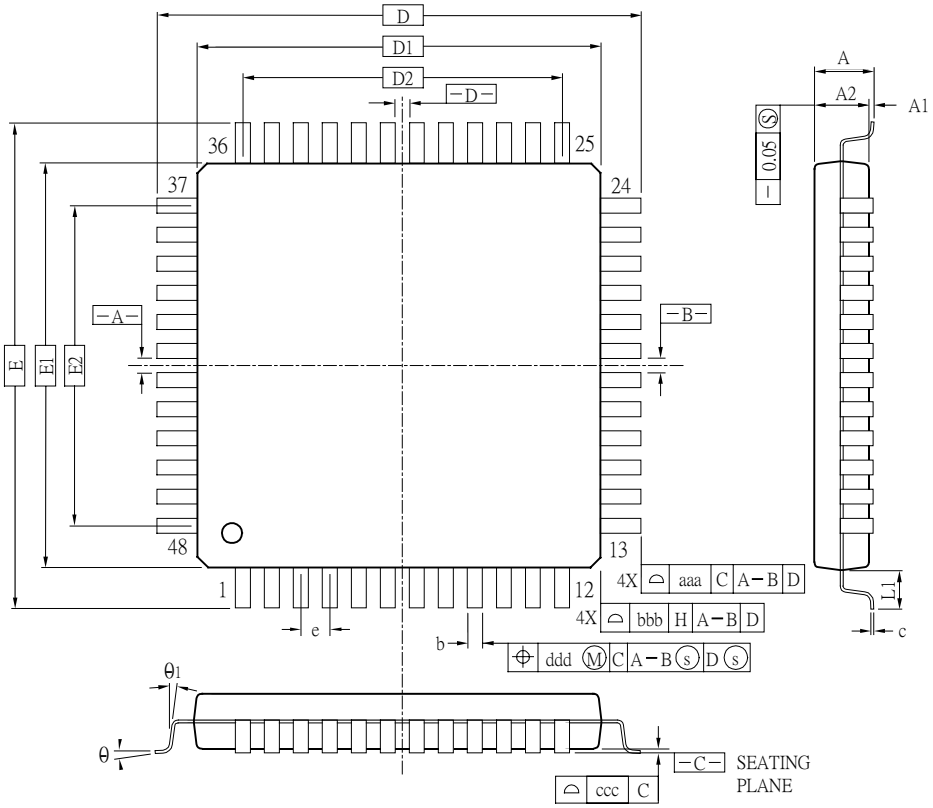
Notes:
The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

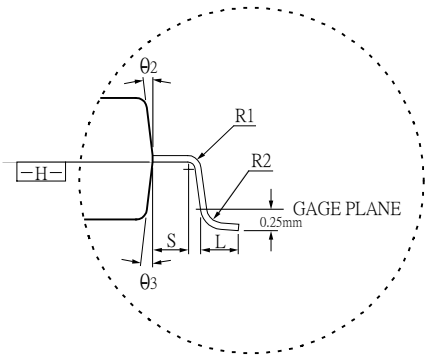
Figure 6.14 - Device Terminating an Ultra DMA Data-Out Burst

6.5 AC Characteristics - USB 2.0

The GL811E conforms to all timing diagrams and specifications for Universal Serial Bus specification rev. 2.0. Please refer to this specification for more information.

CHAPTER 7 PACKAGE DIMENSION





CONTROL DIMENSIONS ARE IN MILLIMETERS.

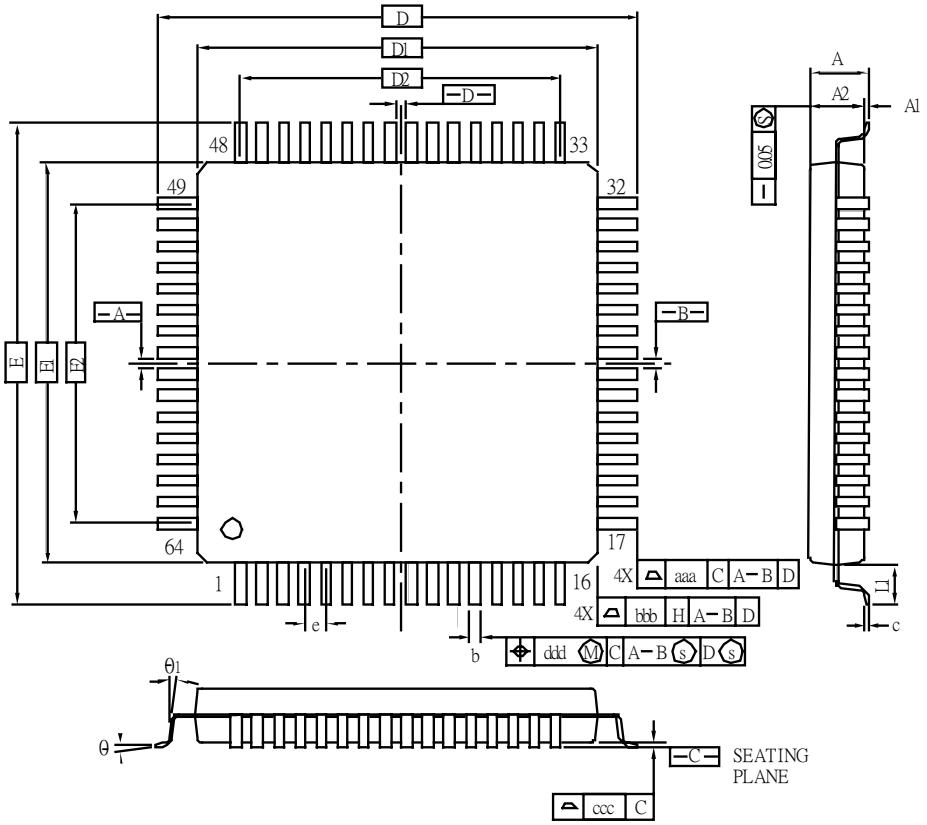
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

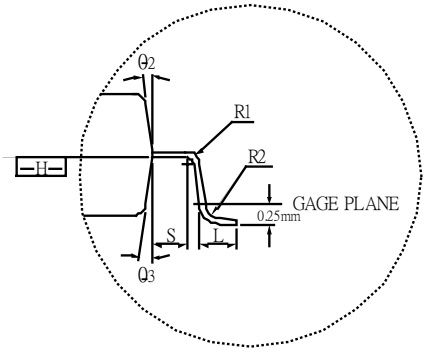
NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 7.1 - GL811E 48 Pin LQFP Package





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00BASIC			0.472BASIC		
E	12.00BASIC			0.472BASIC		
D1	10.00BASIC			0.393BASIC		
E1	10.00BASIC			0.393BASIC		
D2	7.50BASIC			0.295BASIC		
E2	7.50BASIC			0.295BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50BASIC			0.020BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 7.2 - GL811E 64 Pin LQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Status
GL811E	48-pin LQFP	
GL811E	64-pin LQFP	