

8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Description

The CXA1096M is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

Features

- Resolution 8-bit $\pm 1/2$ LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz (-3 dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 390mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/-5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Over range output



Structure

Bipolar silicon monolithic IC

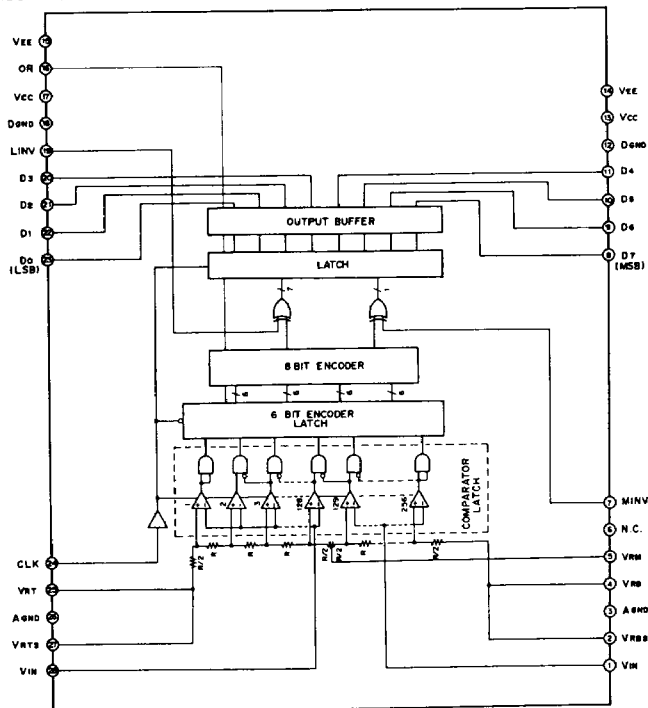
Applications

- Digital TV
- High speed signal processing

Function

8-bit, 20MSPS flash A/D converter

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

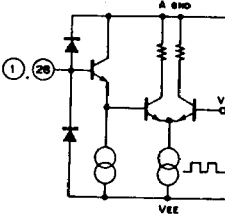
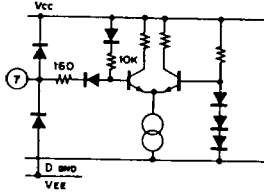
• Supply voltage	VCC—DGND	0 to +6	V
	VEE—AGND	0 to -6	V
	AGND—DGND	0 to +6	V
• Input voltage(analog)	VIN	VEE to AGND +0.3	V
• Input voltage (reference)	VRT, VRB, VRM	VEE to AGND +0.3	V
	VRT - VRB	2.5	V
• Input current (VRM)	IVRM	-3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV	DGND-0.5 to VCC	V
• Storage temperature	Tstg	-55 to +150	°C
• Allowable power dissipation	PD	0.83	W

Recommended Operating Conditions

• Supply voltage (Single supply)	VCC, AGND	4.75 to 5.25	V
	DGND, VEE	0	V
(Dual supply)	VCC	4.75 to 5.25	V
	VEE	-5.5 to -4.75	V
	DGND, AGND	0	V
	VRT	AGND -0.1 to AGND +0.1	V
• Reference input	VRB	AGND -2.2 to AGND -1.8	V
	VIN	VRB to VRT	
• Analog input			
• Clock pulse width	TPW1	35 (Min.)	ns
	TPW0	10 (Min.)	ns
• Operating temperature	Topt	-20 to +75	°C

Pin Description and Equivalent Circuit

No.	Symbol	Voltage	Equivalent circuit	Description
8 to 11 20 to 23	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
16	OR			Over range output pin
12, 18	Dgnd	GND		Digital GND Separated from Agnd
13, 17	Vcc	5V (Typ)		Digital power supply
14, 15	Vee	GND (Single supply) - 5V (Dual supply)		Analog power supply
19	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Input-Output Reference and Output Format) when open "1" is maintained
24	CLK	TTL		Clock input pin
25	VRT	5V (Typ) (Single supply)		Reference voltage (Top)
27	VRTS	GND (Dual supply)		Reference voltage sense (Top)
4	VRB	3V (Typ.) (Single supply) - 2V (Typ.) (Dual supply)		Reference voltage (Bottom)
2	VRBS			Reference voltage sense (Bottom)
5	VRM	4V (Typ.) (Single supply) - 1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity

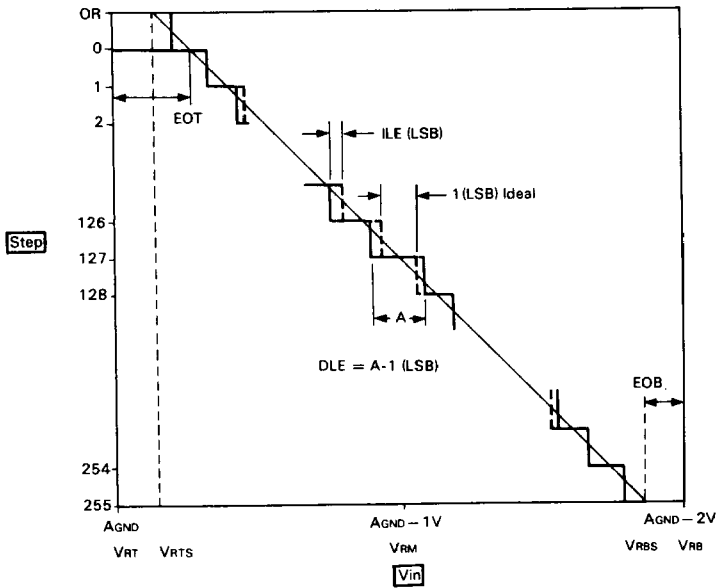
No.	Symbol	Voltage	Equivalent circuit	Description
3, 26	AGND	5V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
1, 28	VIN	VRT to VRB		Analog input Pin 1 and 28 should be connected together.
7	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

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Input-Output Reference and Output Format

Vin	Step	MINV	1	1	0	0		
		LINV	1	0	1	0	OR MSB	LSB
AGND	0	0	000...00	0 011...11	0 100...00	0 111...11	OR MSB	LSB
		1	000...00	1 011...11	1 100...00	1 111...11	OR MSB	LSB
		1	000...01	1 011...10	1 100...01	1 111...10	OR MSB	LSB
AGND -1V	127	1	011...11	1 000...00	1 111...11	1 100...00	OR MSB	LSB
		128	1 100...00	1 111...11	1 000...00	1 011...11	OR MSB	LSB
AGND -2V	254	1	111...10	1 100...01	1 011...10	1 000...01	OR MSB	LSB
		255	1 111...11	1 100...00	1 011...11	1 000...00	OR MSB	LSB
		1	111...11	1 100...00	1 011...11	1 000...00	OR MSB	LSB

1: VIH, VOH
0: VIL, VOL



**Electrical Characteristics
(Single supply)**

VCC = +5V, DGND = 0V, AGND = +5V, VEE = 0V,
VRT = +5V, VRB = +3V, Ta = 25°C

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	
Maximum conversion rate	Fc	VIN = 5 to 3V FIN = Fc/4 - 1 kHz	20			MSPS	
Supply current	ICC + IEE		56	71	91	mA	
Reference pin current	IREF		11	15	18	mA	
Analog input bandwidth	BW		8			MHz	
Analog input capacitance	CIN	VIN = 4V + 0.07Vms		30	35	pF	
Analog input bias current	IIN	VIN = 4V	15	50	110	μA	
Reference resistance (VRT to VRB)	RREF			130		Ω	
Offset voltage	VRT	EOT	8	13	19	mV	
	VRB	EOB	0	5	11	mV	
Digital input voltage	VIH		2.0			V	
	VIL				0.8	V	
Digital input current	IiH	VCC = Max.	VIH = 2.7V	0	-100	-150	μA
	IiL		VIL = 0.5V	-0.1	-0.32	-0.5	mA
Digital output voltage	VOH	VCC = Min.	IOH = -500μA	2.7	3.4		V
	VOL		IOL = 3mA			0.5	V
Output data delay	TDLH	LOAD 1		15	19	22	ns
	TDHL			22	27	31	ns
Non linearity	EL	Fc = 20 MSPS VIN = 5 to 3V			± 1/2	LSB	
Differential non linearity	ED				± 1/2	LSB	
Differential gain error	DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS			1.5	%	
Differential phase error	DP				0.5	deg.	
Aperture jitter	EAP			30		ps	
Sampling delay	tds		5	7	9	ns	

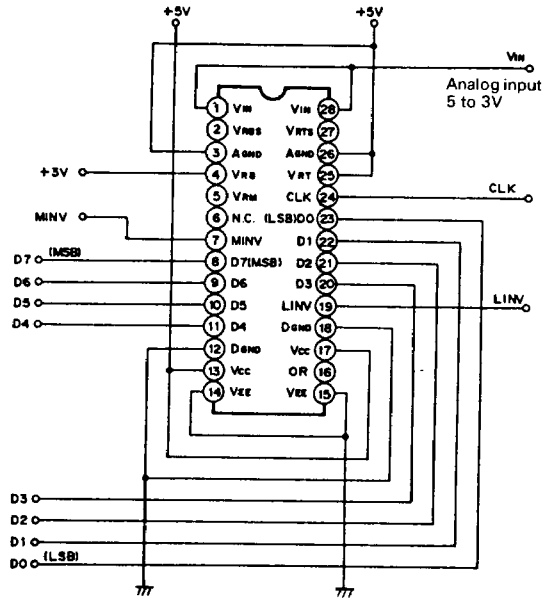
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Electrical Characteristics
(Dual supply)
 $V_{CC} = +5V$, $DGND = 0V$, $AGND = 0V$, $V_{EE} = -5V$,
 $V_{RT} = 0V$, $V_{RB} = -2V$, $T_a = 25^\circ C$

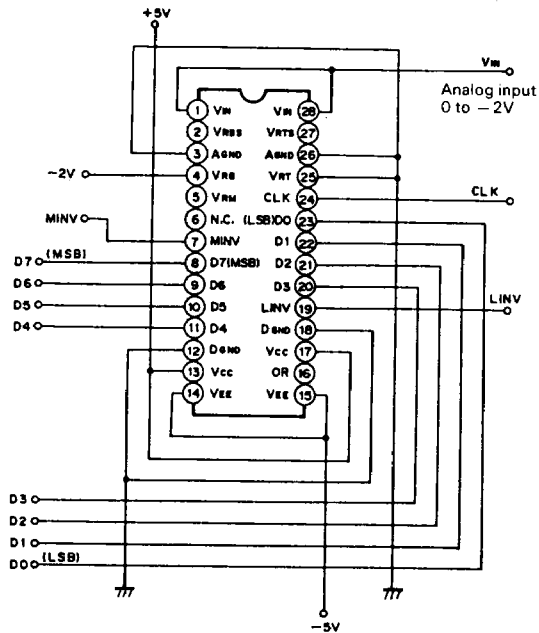
Item	Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate	FC	$V_{IN} = 0$ to $-2V$ $F_{IN} = F_C/4 - 1$ kHz		20			MSPS
Supply current	I_{CC}			7	10	14	mA
	I_{EE}			50	62	78	mA
Reference pin current	I_{REF}			11	15	18	mA
Analog input bandwidth	BW			8			MHz
Analog input capacitance	C_{IN}	$V_{IN} = -1V + 0.07V_{rms}$			30	35	pF
Analog input bias current	I_{IN}	$V_{IN} = -1V$		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})	R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}		8	13	19	mV
	V_{RB}	E_{OB}		0	5	11	mV
Digital input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Digital input current	I_{IH}	$V_{CC} = \text{Max.}$	$V_{IH} = 2.7V$	0	-100	-150	μA
	I_{IL}		$V_{IL} = 0.5V$	-0.1	-0.32	-0.5	mA
Digital output voltage	V_{OH}	$V_{CC} = \text{Min.}$	$I_{OH} = -500\mu A$	2.7	3.4		V
	V_{OL}		$I_{OL} = 3mA$			0.5	V
Output data delay	T_{DLH}	LOAD 1		15	19	22	ns
	T_{DHL}			22	27	31	ns
Non linearity	EL	$F_C = 20$ MSPS $V_{IN} = 0$ to $-2V$				$\pm 1/2$	LSB
Differential non linearity	ED					$\pm 1/2$	LSB
Differential gain error	DG	NTSC 40 IRE mod. ramp, $F_C = 14.3$ MSPS				1.5	%
Differential phase error	DP					0.5	deg.
Aperture jitter	EAP				30		ps
Sampling delay	tds			5	7	9	ns

Application Circuit and Electrical Characteristics Test Circuit
Single supply

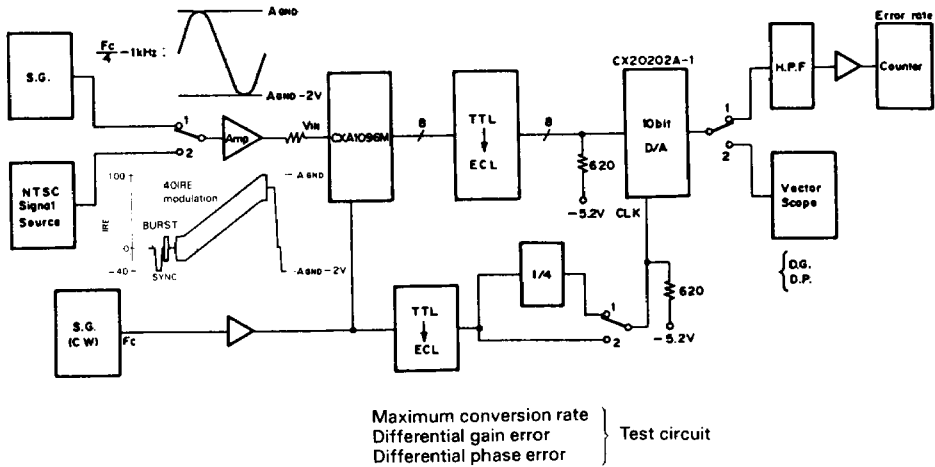
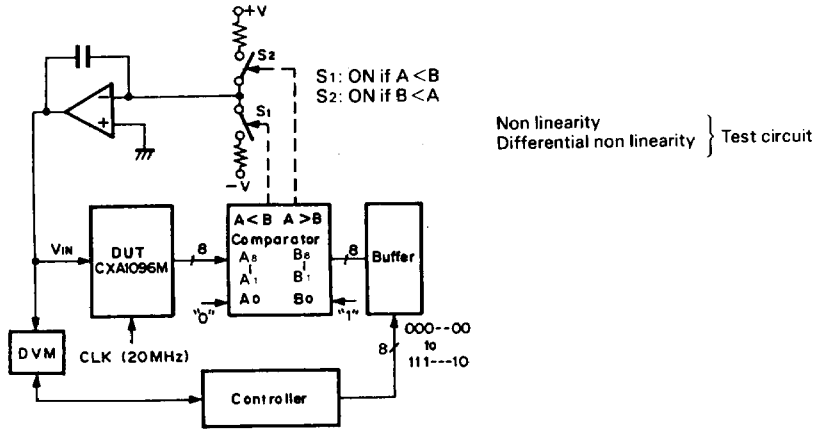
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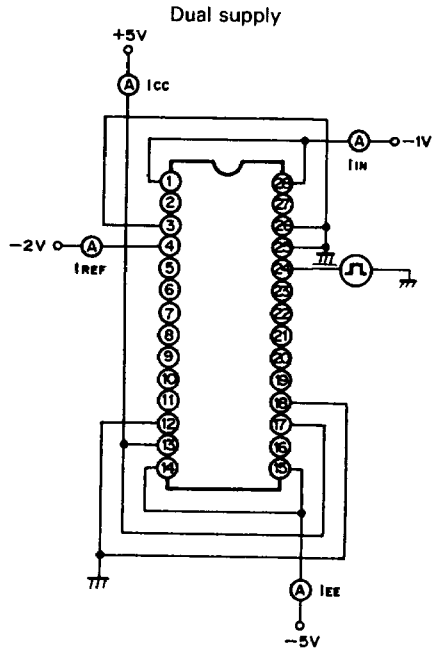
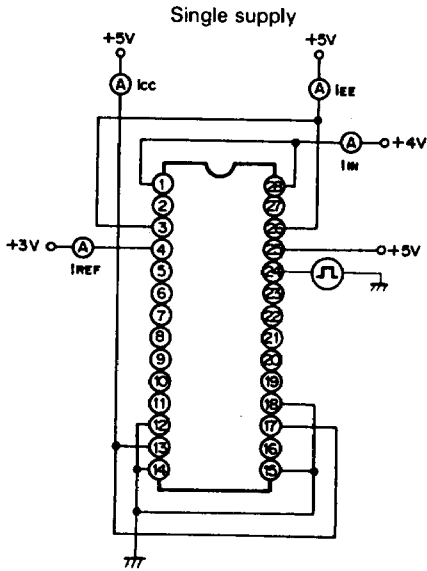
Dual supply



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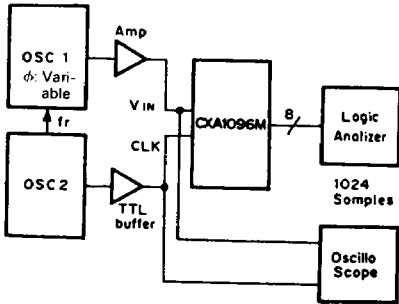
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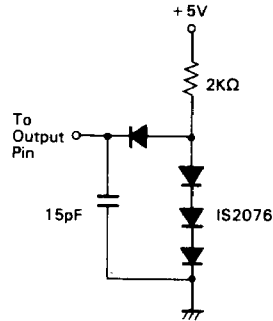
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Note) VIN pin is connected to VRT pin for ICC and IEE measurement.

Supply current
 Analog input bias current
 Reference pin current } Test circuit

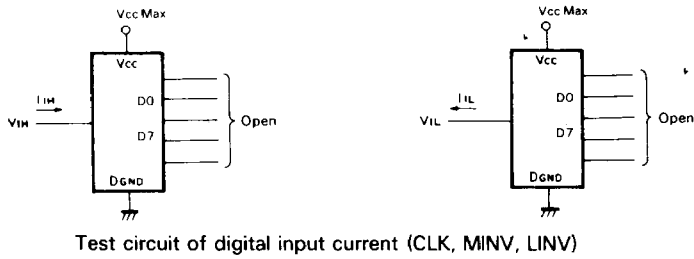
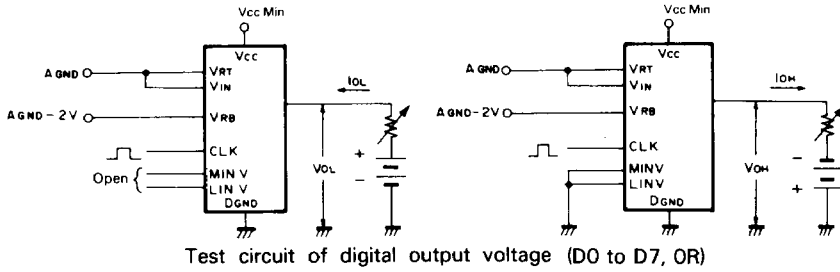


Aperture jitter
 Sampling delay } Test circuit

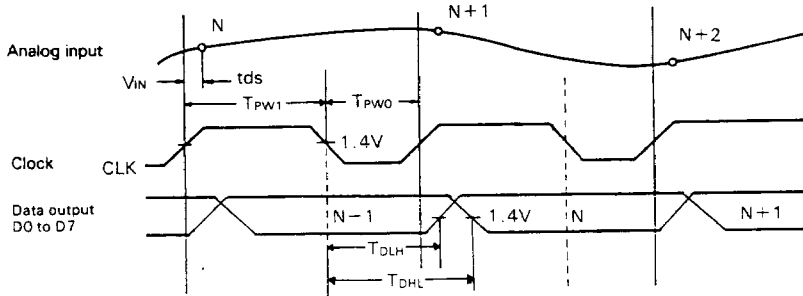


LOAD1 Test Load for Output data delay

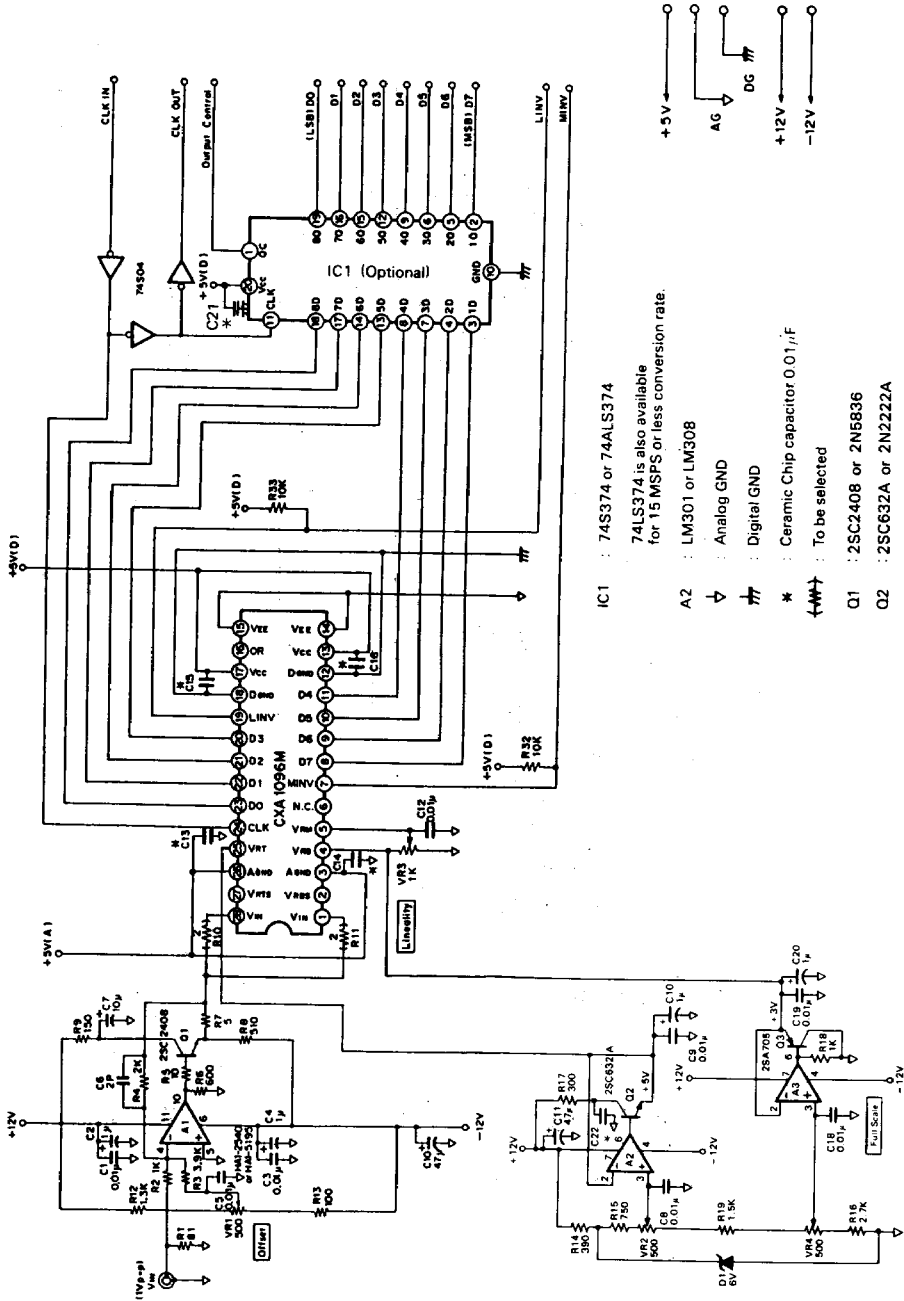
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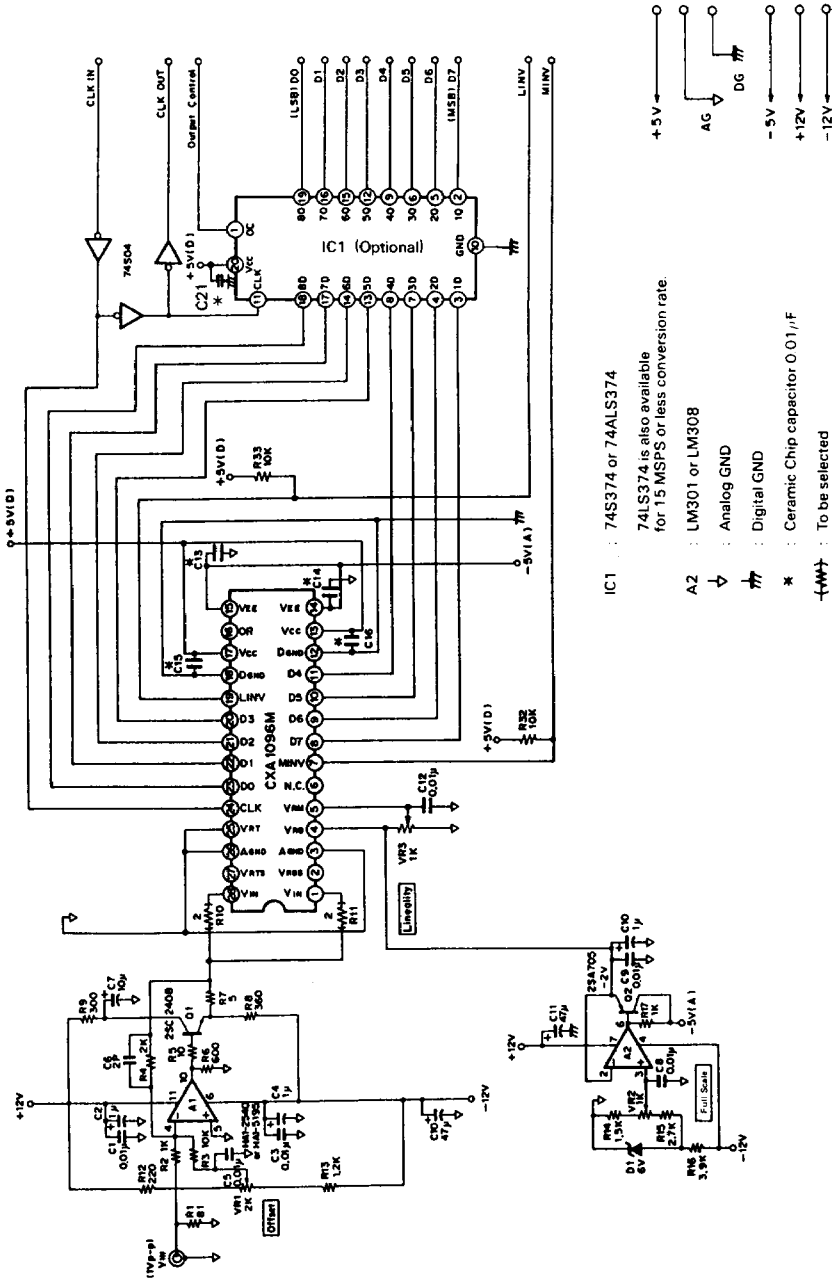
Timing Chart



Application Circuit (Single supply)



Application Circuit (Dual supply)



IC1 : 74S374 or 74ALS374

74ALS374 is also available for 15 MSPS or less conversion rate.

A2 : LM301 or LM308

∇ : Analog GND

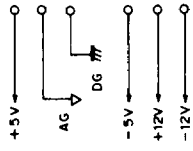
⏏ : Digital GND

* : Ceramic Chip capacitor 0.01 μ F

-(∇) : To be selected

Q1 : 2SC2408 or 2N5836

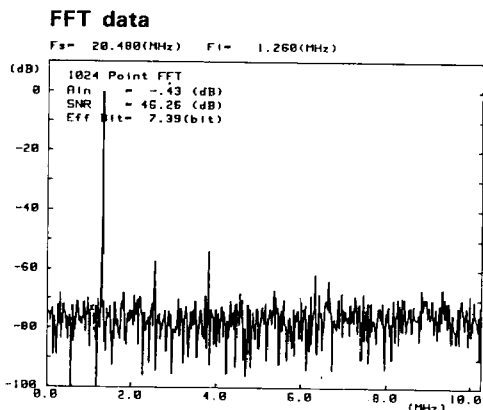
Q2 : 2SA705 or 2N2907A



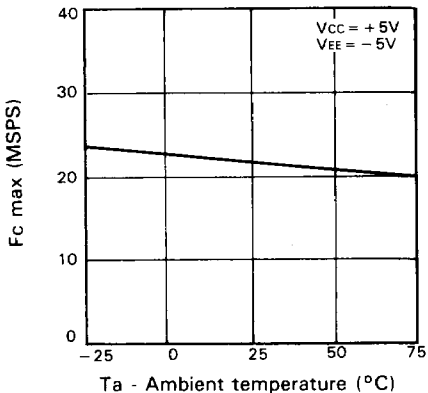
Notes on Application

- Each of DGND pins (12, 18) and each of VCC Pins (13, 17) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.
- Layout of the analog and digital sections should be separated to reduce noise effect.
VEE pins to AGND and VCC pins to DGND should be bypassed as closely as possible by means of $1\mu\text{F}$ and $0.01\mu\text{F}$ capacitors.
For the $0.01\mu\text{F}$, a ceramic chip capacitor should be used.
- The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power.
Pins VIN (1, 28) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
The amplifier output and A/D input should be connected as closely as possible.
- Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of $1\mu\text{F}$ and $0.01\mu\text{F}$ capacitors.
Through bypassing VRM pin with a $0.01\mu\text{F}$ capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.
- CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.
- Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the negative going edge with a short delay time (TDLH, TDHL).
If digital data will be latched externally, it should be latched at the negative going edge. (See the Timing Chart)
- It is recommended to connect free pins to AGND for prevention of noise effect.

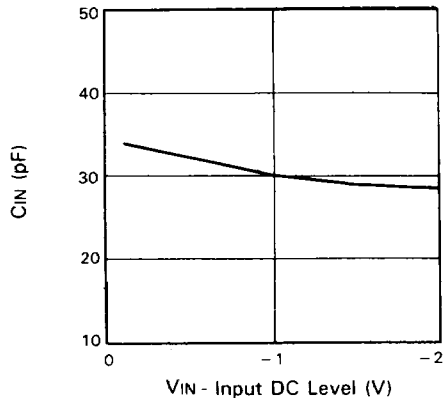
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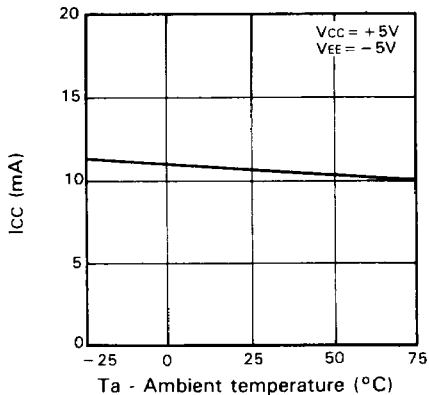
Fc max vs. Ambient temperature



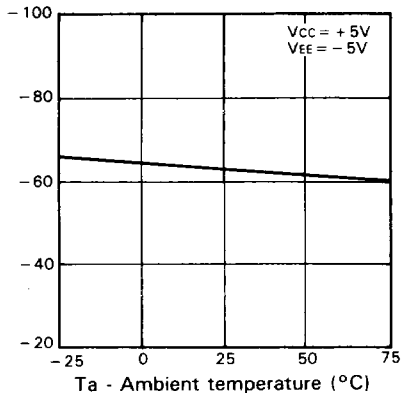
CIN vs. VIN - Input DC level



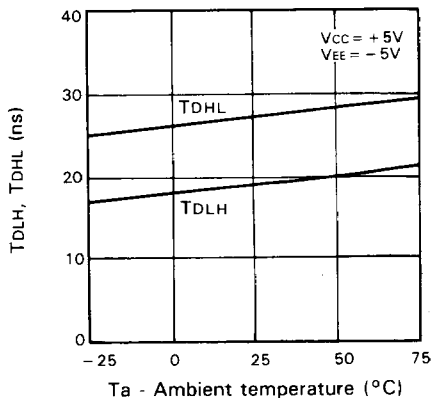
ICC vs. Ambient temperature



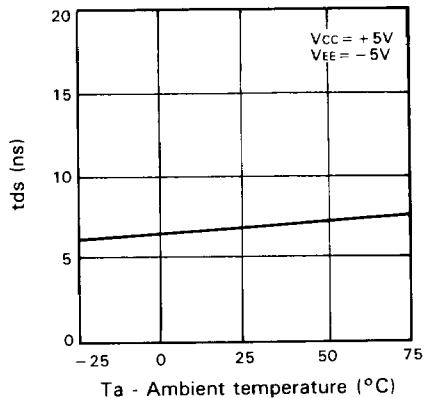
IEE vs. Ambient temperature



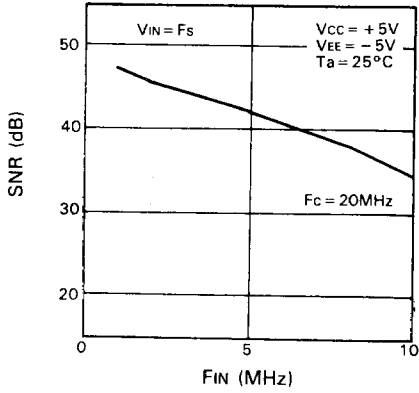
TDLH, TDHL vs. Ambient temperature



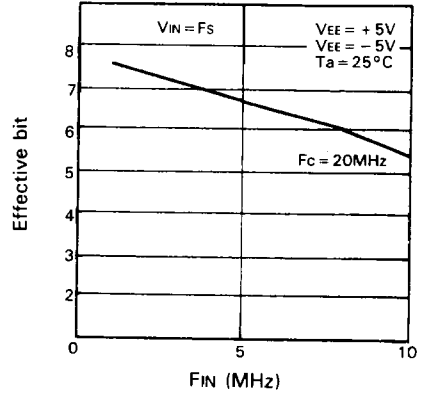
tds vs. Ambient temperature



SNR vs. F_{IN}

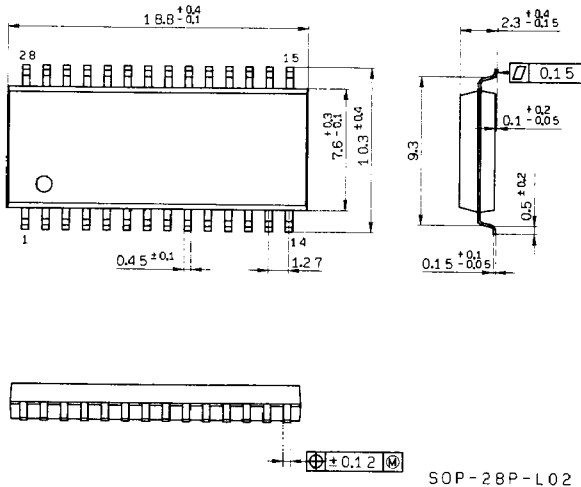


Effective bit vs. F_{IN}



Package Outline Unit : mm

28pin SOP(Plastic) 375mil 0.6g



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