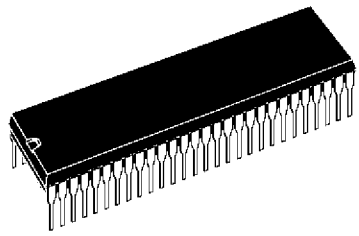
SGS-THOMSON MICROELECTRONICS

ST90R28

ROMLESS HCMOS MCU WITH RAM

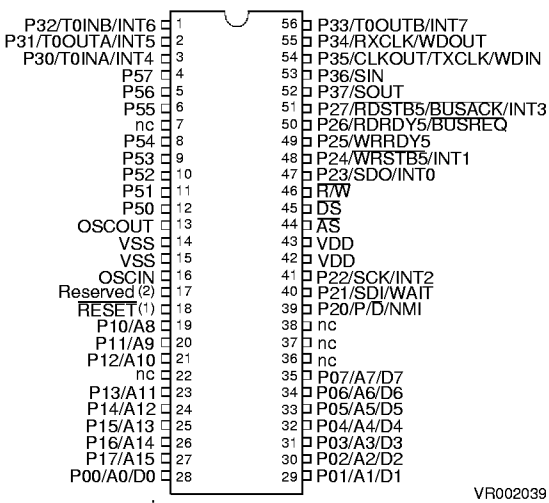
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time:500ns (12MHz internal)
- ROMless to allow maximum external memory flexibility
- Internal Memory :
  RAM 256 bytes
  224 general purpose registers available as RAM, accumulators or index pointers (register file)
- 56-pin Plastic Dual-In-Line package
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- One 16 bit Multifunction Timer, with an 8 bit prescaler and 12 operating modes
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile development tools, including assembler, linker, C-compiler, archiver, graphic orinted debugger and hardware emulators
- Real Time Operating System



PSDIP56

(Ordering Information at the end of the Datasheet)

Figure 1. 56-Pin PDIP Package)



1.1 GENERAL DESCRIPTION

The ST90R28 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ST90R28 is fully compatible with the ST902x ROM version and this datasheet will thus provide only information specific to the ROMLESS device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST902x ROM-BASED DEVICE.

The ROMLESS ST90R28 can be configured as a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

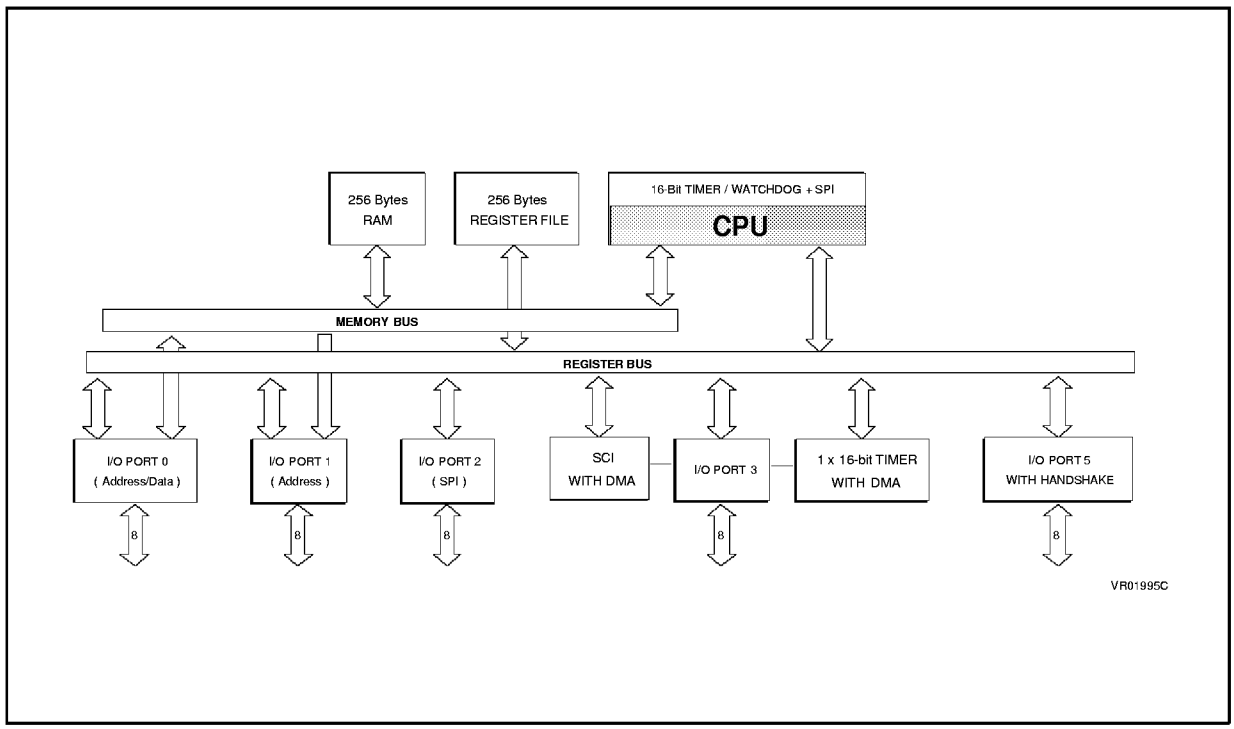
The nucleus of the ST90R28 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R28 with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer with an 8 bit Prescaler and 12 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Figure 1-2. Block Diagram



GENERAL DESCRIPTION (Continued)

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

1.2 PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90R28 accesses on-chip Data memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for memory transactions. R/$\overline{W}$ is low when writing to program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

AD0-AD7, (P0.0-P0.7) *Address/Data Lines (Input/Output, TTL or CMOS compatible).* 8 lines providing a multiplexed address and data bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

A8-A15 *Address Lines (Output, TTL or CMOS compatible).* 8 lines providing non-multiplexing address bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 40 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

1.3 I/O PORT ALTERNATE FUNCTIONS

Each pin of the I/O ports of the ST90R28 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pins.

1.4 MEMORY

The memory of the ST90R28 is functionallydivided into two areas, the Register File and Memory. The

PIN DESCRIPTION (Continued)

Table 1-1. I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function	Alternate Function	Pin Assignment SDIP56
P0.0	A0/D0	I/O	Address/Data bit 0 mux	28
P0.1	A1/D1	I/O	Address/Data bit 1 mux	29
P0.2	A2/D2	I/O	Address/Data bit 2 mux	30
P0.3	A3/D3	I/O	Address/Data bit 3 mux	31
P0.4	A4/D4	I/O	Address/Data bit 4 mux	32
P0.5	A5/D5	I/O	Address/Data bit 5 mux	33
P0.6	A6/D6	I/O	Address/Data bit 6 mux	34
P0.7	A7/D7	I/O	Address/Data bit 7 mux	35
P1.0	A8	O	Address bit 8	19
P1.1	A9	O	Address bit 9	20
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	23
P1.4	A12	O	Address bit 12	24
P1.5	A13	O	Address bit 13	25
P1.6	A14	O	Address bit 14	26
P1.7	A15	O	Address bit 15	27
P2.0	NMI	I	Non-Maskable Interrupt	39
P2.0	P/$\overline{D}$	O	Program/Data Space Select	39
P2.1	SDI	I	SPI Serial Data In	40
P2.1	$\overline{WAIT}$	I	External Wait Input	40
P2.2	INT2	I	External Interrupt 2	41
P2.2	SCK	O	SPI Serial Clock	41
P2.3	INT0	I	External Interrupt 0	47
P2.3	SDO	O	SPI Serial Data Out	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{WRSTB5}$	I	Handshake Write Strobe P5	48
P2.5	WRRDY5	O	Handshake Write Ready P5	49
P2.6	RDRDY5	O	Handshake Read Ready P5	50

PIN DESCRIPTION (Continued)

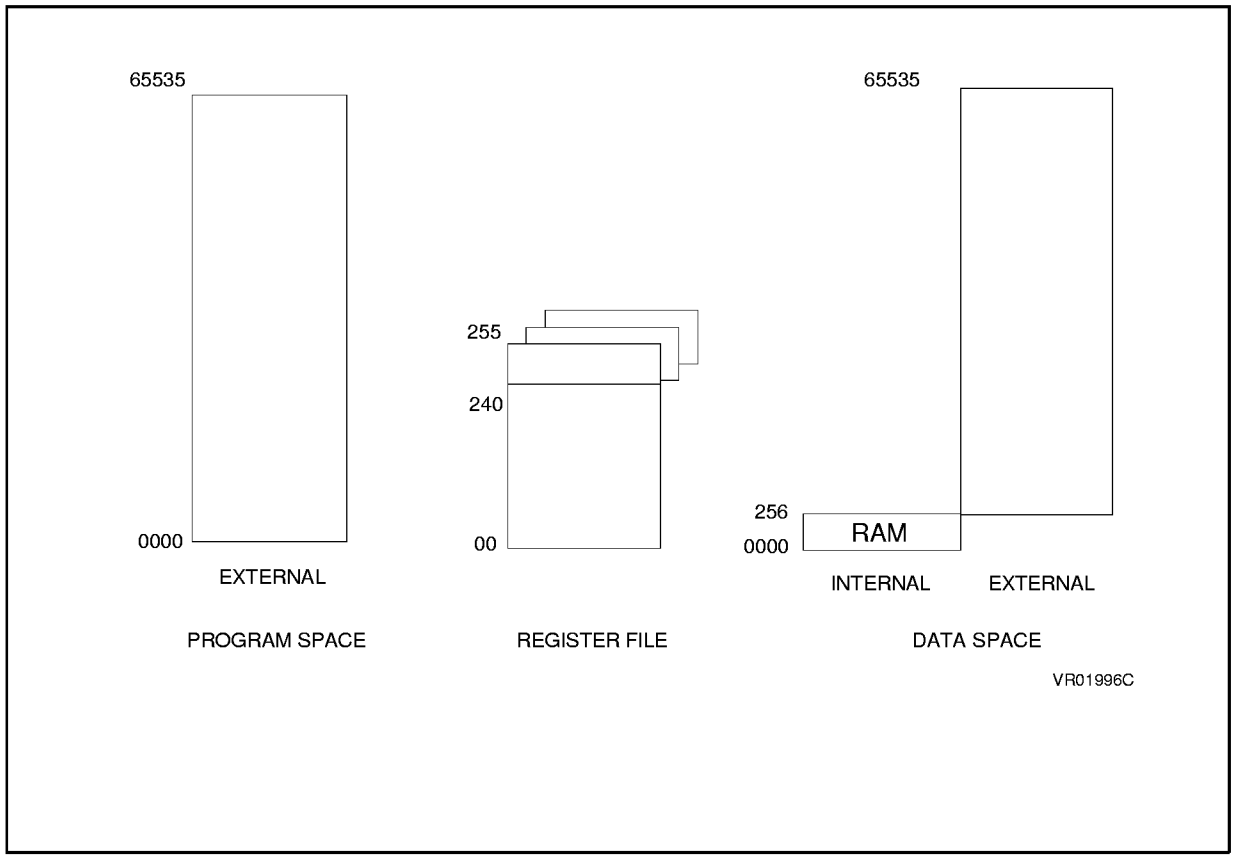
Table 17.1. I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function	Alternate Function	Pin Assignment SDIP56
P2.6	$\overline{\text{BUSREQ}}$	I	External Bus Request	50
P2.7	INT3	I	External Interrupt 1	51
P2.7	$\overline{\text{RDSTB5}}$	I	Handshake Read Strobe P5	51
P2.7	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	51
P3.0	INT4	I	External Interrupt 4	3
P3.0	T0INA	I	MF Timer 0 Input A	3
P3.1	INT5	I	External Interrupt 5	2
P3.1	T0OUTA	O	MF Timer 0 Output A	2
P3.2	INT6	I	External Interrupt 6	1
P3.2	T0INB	I	MF Timer 0 Input B	1
P3.3	INT7	I	External Interrupt 7	56
P3.3	T0OUTB	O	MF Timer 0 Output B	56
P3.4	RXCLK	I	SCI Receive Clock Input	55
P3.4	WDOUT	O	T/WD Output	55
P3.5	CLKOUT	O	SCI Byte Sync Clock Output	54
P3.5	TXCLK	I	SCI Transmit Clock Input	54
P3.5	WDIN	I	T/WD Input	54
P3.6	SIN	I	SCI Serial Input	53
P3.7	SOUT	O	SCI Serial Output	52
P5.0		O	I/O Handshake Port 5	12
P5.1		O	I/O Handshake Port 5	11
P5.2		O	I/O Handshake Port 5	10
P5.3		O	I/O Handshake Port 5	9
P5.4		O	I/O Handshake Port 5	8
P5.5		O	I/O Handshake Port 5	6
P5.6		O	I/O Handshake Port 6	5
P5.7		O	I/O Handshake Port 7	4

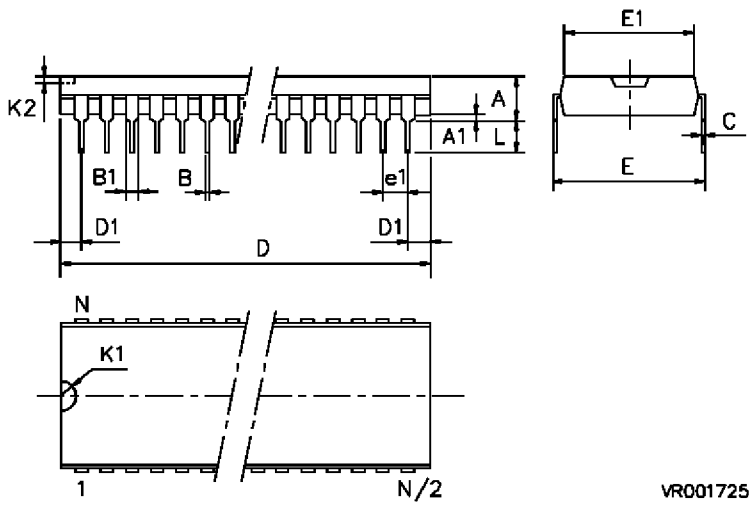
Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R28 addresses all program memory in the external PROGRAM space. The DATA space includes the 256 bytes of on-chip RAM memory at memory addresses 00h through 00FFh.

The External Memory spaces are addressed using the multiplexed address and data buses on Ports 0 and 1. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory.

Figure 1-3. Memory Spaces



56-Pin Plastic Shrink Dual In Line Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D		52.12			2.052	
D1	–	–	–	–	–	–
E			18.54			0.730
E1		13.72				0.540
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	2.54		3.81	.100		0.150
e1		1.78			0.070	
Number of Pins						
N	56					

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90R28B1	24MHz	0°C to + 70°C	PSDIP56
ST90R28B6		-40°C to + 85°C	PSDIP56