PROTEK DEVICES
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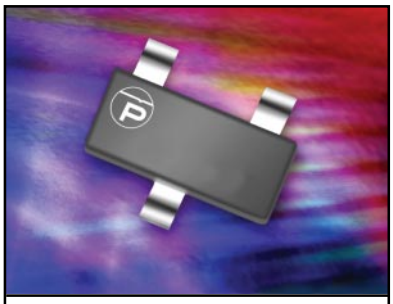
PLC497

ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS



SOT-23

✔ Low Voltage Wireless Equipment
✔ Sensor & Control Circuits
✔ Ethernet - 10/100 Base T
✔ FireWire

IEC COMPATIBILITY (EN61000-4)

✔ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
✔ 61000-4-4 (EFT): 40A - 5/50ns
✔ 61000-4-5 (Surge): 24A, 8/20µs - Level 2(Line-Ground) & Level 3(Line-Line)

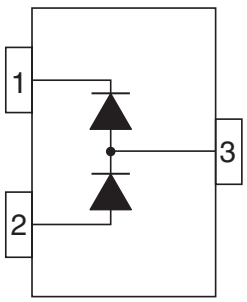
FEATURES

✔ 250 Watts Peak Pulse Power per Line (tp = 8/20µs)
✔ Unidirectional Configuration
✔ ESD Protection > 25 kilovolts
✔ Low Clamping Voltage < 5 Volts
✔ ***ULTRA LOW CAPACITANCE: 2.5pF***
✔ RoHS Compliant in Lead-Free Versions

MECHANICAL CHARACTERISTICS

✔ Molded JEDEC SOT-23
✔ Weight 8 milligrams (Approximate)
✔ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
✔ Solder Reflow Temperature:
Tin-Lead - Sn/Pb, 85/15: 240-245°C
Pure-Tin - Sn, 100: 260-270°C
✔ Flammability rating UL 94V-0
✔ 8mm Tape and Reel Per EIA Standard 481
✔ Device Marking: Marking Code

PIN CONFIGURATION



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power - t_p = 8/20µs (See Figure 1)	P_{PP}	250	W
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified								
PART NUMBER	DEVICE MARKING CODE	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE (See Note 1) @1mA $V_{(BR)}$ VOLTS	MAXIMUM REVERSE LEAKAGE CURRENT (See Note 1) @V_{WM} I_D µA	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2) @8/20µs V_C @ I_{PP}	MAXIMUM WORKING INVERSE BLOCKING VOLTAGE (See Note 2) V_{WB} VOLTS	INVERSE BLOCKING LEAKAGE CURRENT (See Note 2) @V_{WB} I_R µA	MAXIMUM CAPACITANCE (See Note 3) @0V, 1MHz C pF
PLC497	LC	1.0	1.3	20	5.0V @ 50A	75	1.0	2.5

Note 1: Apply positive voltage from pin2 to 1.
Note 2: Apply positive voltage from pin 1 to 2.
Note 3: Capcitance from pin 1 to 2 < 2.5pF.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

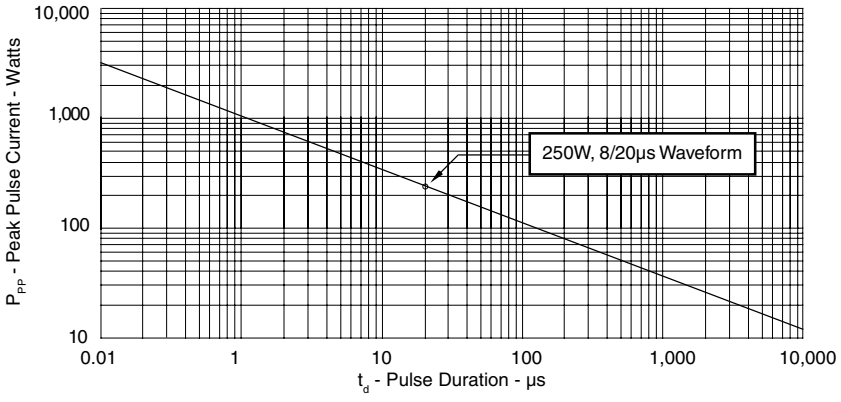
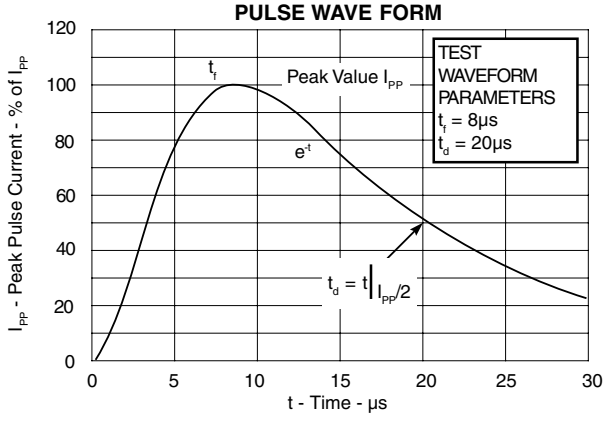


FIGURE 2
PULSE WAVE FORM



GRAPHS

FIGURE 3
POWER DERATING CURVE

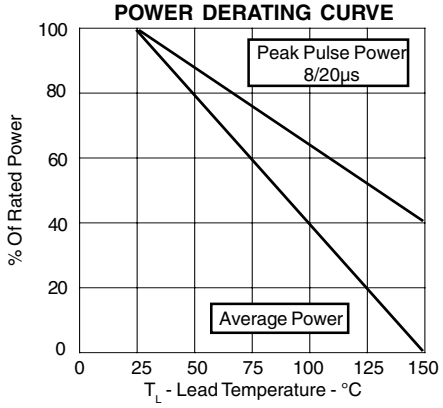
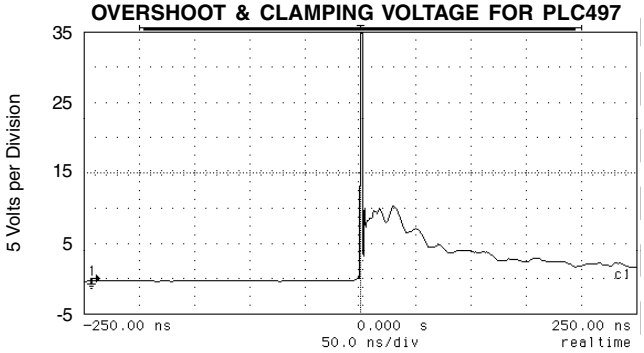
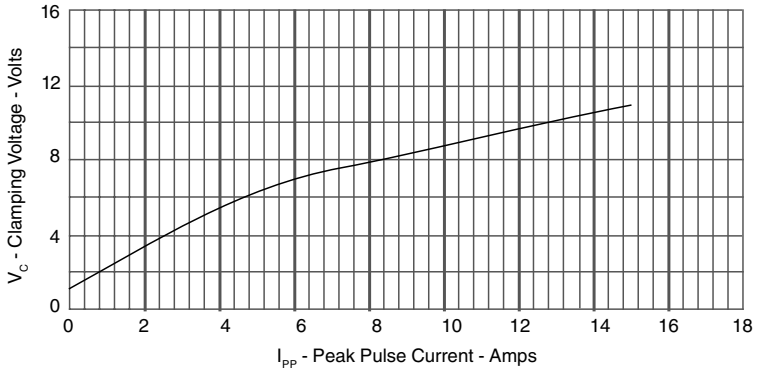


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR PLC497



ESD Test Pulse: 25 kilovolt, 1/30ns (waveshape)

FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR PLC497



APPLICATION NOTE

The PLC497 is an ultra low capacitance, bidirectional array that is designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product has a surge capability of 250 Watts P_{PP} per line for an 8/20µs wave form and offers ESD protection > 40kV.

DIFFERENTIAL-MODE CONFIGURATION (Figure 1)

The PLC497 is designed to protect one unidirectional line. Figure 1 shows a typical differential-mode (line to line) I/O port protection circuit application. To achieve bidirectional protection, two PLC497 units are placed in parallel with opposing polarities within the circuit layout.

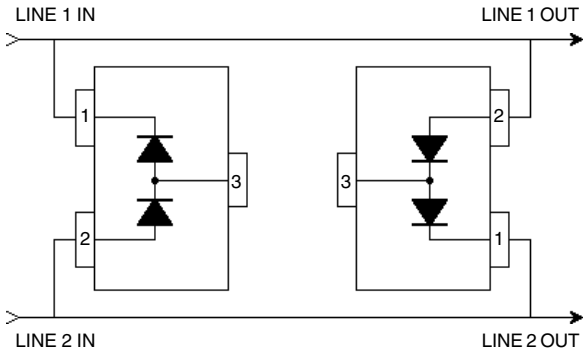
Circuit connectivity is as follows:
✔ Pins 1 and 2 of each device connected to datalines
✔ Pin 3 is not connected

COMMON-MODE CONFIGURATION (Figure 2)

The PLC497 can provide protection for sensor circuit applications. Figure 2 is a typical common-mode (line to ground) sensor circuit application. To achieve bidirectional protection in this application, a second pair of TVS devices is added in parallel with opposing polarities where pins 2 are connected to the line, pins 1 connected to ground and pins 3 unconnected.

Circuit connectivity is as follows:
✔ Pins 1 each device connected to datalines
✔ Pins 2 each device connected to ground
✔ Pin 3 is not connected

Figure 1. Typical Differential-Mode i/o Port Protection Circuit



CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

✔ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.

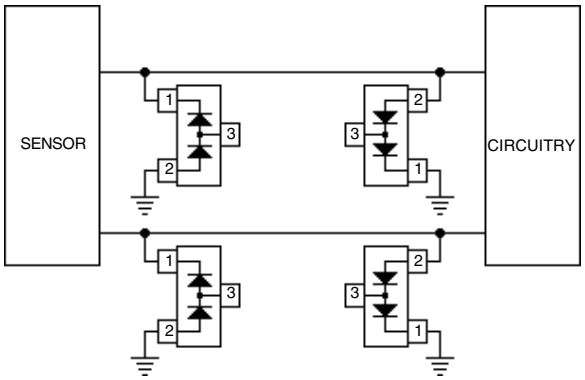
✔ The path length between the TVS device and the protected line should be minimized.

✔ All conductive loops including power and ground loops should be minimized.

✔ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.

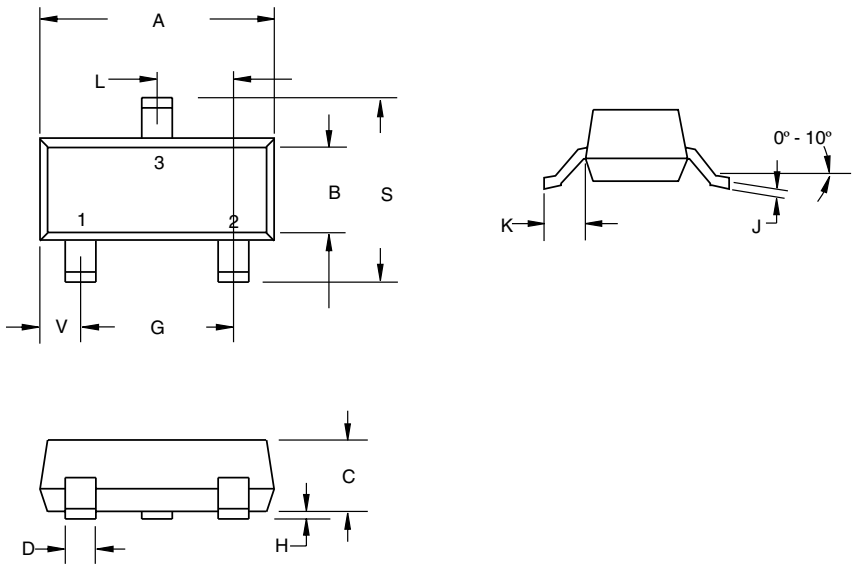
✔ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 2. Typical Common-Mode Sensor Protection Circuit



PACKAGE OUTLINE & DIMENSIONS

PACKAGE OUTLINE

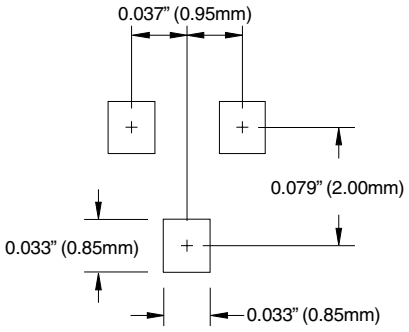


SOT-23

PACKAGE DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

MOUNTING PAD



NOTES

1. Dimensioning and tolerances per ANSI Y14.5M, 1985.
2. Controlling Dimension: Inches
3. Pin 3 is the cathode (Unidirectional Only).
4. Dimensions are exclusive of mold flash and metal burrs.

TAPE & REEL ORDERING NOMENCLATURE

1. Surface mount product is taped and reeled in accordance with EIA-481.
2. Suffix -T7 = 7 Inch Reel - 3,000 pieces per 8mm tape, i.e., *PLC497-T7*.
3. Suffix -T13 = 13 Inch Reel - 10,000 pieces per 8mm tape, i.e., *PLC497-T13*.
4. Suffix - LF = Lead-Free, Pure-Tin Plating, i.e., *PLC497-LF-T7*.

Outline & Dimensions: Rev 1 - 11/01, 06012

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