SONY

CXA3171N

4ch. Read/Write Amplifier for three terminal MIG Head of Hard Disk Drive

Description

The CXA3171N is a Read/Write Amplifier for the special three terminal MIG head of hard disk drive and designed to handle up to 4 channel heads.

Features

- Operate on single +5 V power supply
- Low power consumption
  Read : 95 mW
  Write : 115 mW + $I_W \times 5$
- Designed for special three terminal MIG heads
- Read amplifier emitter follower output featuring 420 times gain (typ).
- Differential input capacitance for Read : 6.7 pF (typ)
- Input noise : 0.46nV / $\sqrt{Hz}$ (typ)
- Differential Head voltage swing : 9 Vp-p (typ)
- Differential P-ECL write data input
- Built-in write unsafe detection circuit.
- Built-in Servo write function (2/4 ch).
- Built-in IC protection circuit for short of head and GND.
- Read data outputs are high impedance in write mode.
- Built-in supply voltage monitor circuit prohibits incorrect write during power on or abnormal voltage.
- Self switching damping resistance (R_D=420 Ω).

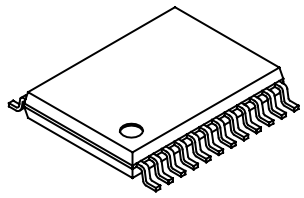
Function

Read, Write and Write unsafe detection for HDD, power supply ON/OFF detection.

Structure

Bipolar silicon monolithic IC

24 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	6	V
• Write current	I_W	23	mAo-p
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	800	mW
• WUS/SE pin input current	I_{SEH}	15	mA

Recommended Operating Conditions

• Supply voltage	V_{CC}	5.0 V±10	%
• Write current	I_W	10 to 22	mAo-p

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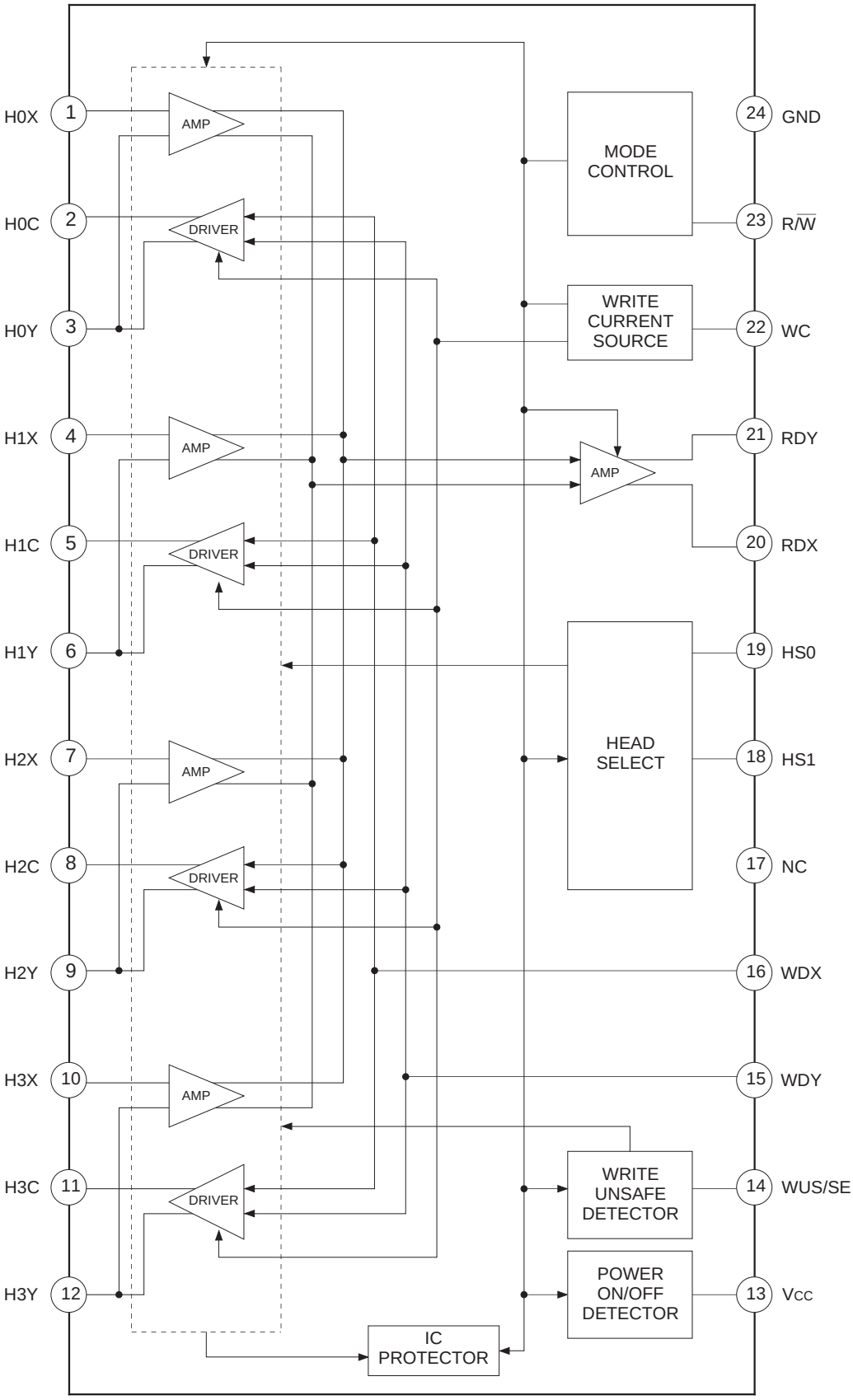
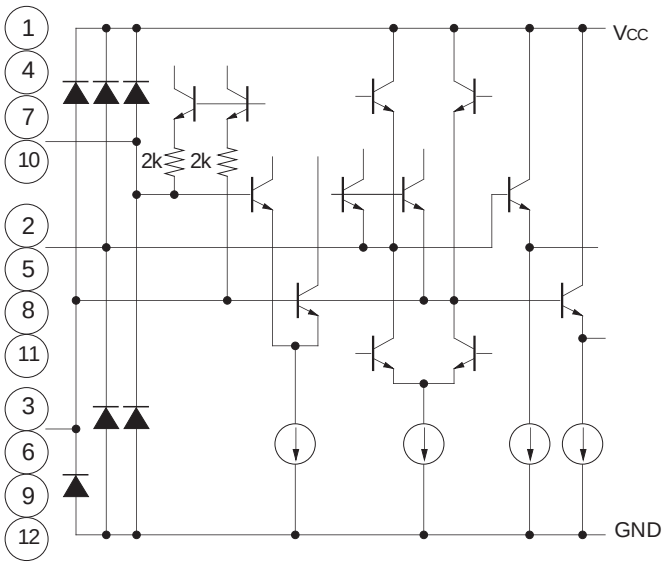
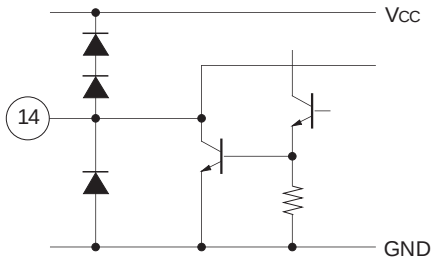
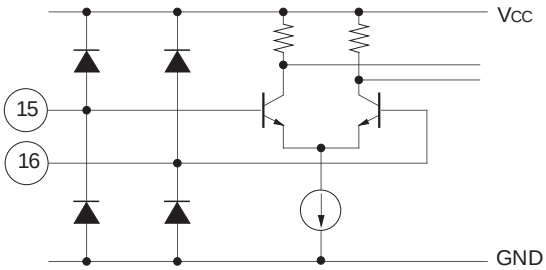
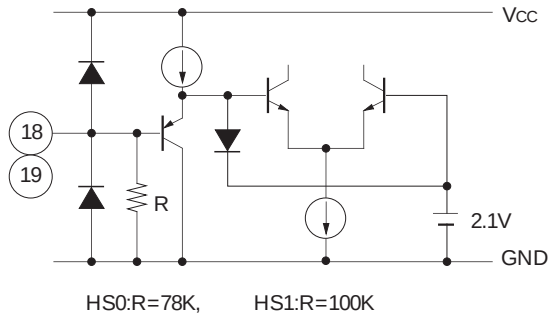
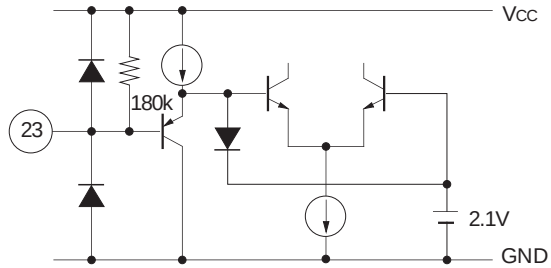
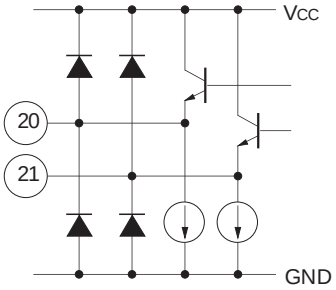
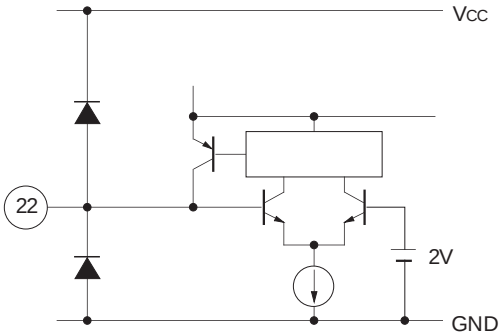

H0X
1
AMP
H0C
2
DRIVER
H0Y
3
H1X
4
AMP
H1C
5
DRIVER
H1Y
6
H2X
7
AMP
H2C
8
DRIVER
H2Y
9
H3X
10
AMP
H3C
11
DRIVER
H3Y
12
MODE CONTROL
WRITE CURRENT SOURCE
AMP
HEAD SELECT
WRITE UNSAFE DETECTOR
POWER ON/OFF DETECTOR
IC PROTECTOR
24
GND
23
R/W
22
WC
21
RDY
20
RDX
19
HS0
18
HS1
17
NC
16
WDX
15
WDY
14
WUS/SE
13
Vcc

Pin Description

No.	Symbol	Equivalent circuit	Description
24	GND		
1 2 3 4 5 6 7 8 9 10 11 12	H0X H0C H0Y H1X H1C H1Y H2X H2C H2Y H3X H3C H3Y		Head. 4 channels provided.
14	WUS/SE		Write unsafe detection output / Servo Enable signal input.
15 16	WDY WDX		Differential P-ECL write data input.
13	Vcc		5 V power supply.
17	NC		

No.	Symbol	Equivalent circuit	Description
18 19	HS1 HS0	 HS0:R=78K, HS1:R=100K	Head select signal input. Selects one of 4 heads according to Table 2.
23	R/$\overline{W}$		Read/Write signal input At “High” : Read, at “Low” : Write.
20 21	RDX RDY		Read Amplifier output.
22	WC		A setting resistor for the write current value is connected between this pin and GND.

Electrical Characteristics (Unless otherwise specified, V_{CC}=5 V, Ta=25 °C, Write current I_W=20 mA)

No.	Item	Symbol	SW conditions																	Measurement conditions	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17					
1-1	Current consumption for Read	I_R	a	a	a	a	a	a	a	a	e	b	a	a	b	a	a	b	b	Test point : I_2	12	19	28	mA
1-2	Current consumption for Write	I_{WR}	b	b	b	b	a	a	a	a	e	b	a	a	b	a	a	b	a	Test point : I_2	17 +I_W	23 +I_W	36 +I_W	mA
2-1	Digital input “Low” input voltage	V_{IL}																		Digital input : Pins 18, 19, 23			0.8	V
2-2	Digital input “High” input voltage	V_{IH}																			2.0			V
2-3	Digital input “Low” input current	I_{IL}	a	a	a	a	a	a	a	a	e	b	a	a	b	a	a	b	a	“High” applied voltage : 5 V “Low” applied voltage : 0 V Test point : I_6, I_7, I_8, I_9	–100			µA
2-4	Digital input “High” input current	I_{IH}	a	a	a	a	a	a	a	a	e	b	a	a	b	b	b	b	b				100	µA
2-5	Write data input “Low” input voltage	V_{WDL}																			V_{WDH} –2.0		V_{WDH} –0.25	V
2-6	Write data input “High” input voltage	V_{WDH}																			V_{CC} –1.1		V_{CC} –0.4	V
2-7	Write data input current	I_{WD}	b	b	b	b	a	a	a	a	e	b	a	a	b	a	a	a	a	Input voltage : 4 V			50	µA
3-1	Write unsafe output saturation voltage	V_{WUS}	b	b	b	b	b	a	a	a	b	b	a	c	c	a	a	b	a	Output current : 1 mA Test point : V_1			0.5	V
3-2	Write unsafe output leak current	I_{WUS}	b	b	b	b	a	a	a	a	e	b	a	a	b	a	a	b	a	Test point : I_3			50	µA
4	Supply power ON/OFF detector threshold voltage	V_{TH}	b	b	b	b	b	a	a	a	a	b	a	a	b	a	a	b	a	When V_{CC} is lowered from 5 V in Write mode and I_W does not flow anymore, V_{CC} voltage is set to V_{THOFF}. When V_{CC} is raised from 3 V and I_W starts to flow, V_{CC} voltage is set to V_{THON}.	3.4	3.9	4.3	V

No.	Item	Symbol	SW conditions																	Measurement conditions	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17					
5-1	Write current setting range	I_W																			10		22	mA_{o-p}
5-2	Write current voltage	V_{WC}	b	b	b	b	a	a	a	a	e	b	a	a	b	a	a	a	a		2.25	2.5	2.75	V
5-3	Write current gain	A_W																		$I_W=A_W \bullet V_{WC}/R_{WC}$	18	20	22	mA/mA
5-4	Write current setting constant	K_W	b	b	b	b	b	a	a	a	a	b	a	a	b	a	a	b	a	$I_W=K_W/R_{WC}$	45	50	55	
6-1	WUS/SE voltage	V_{SEH}	b	b	b	b	b	a	a	a	a	b	b	a	a	a	a	b	a	Servo write enabled	V_{CC} +1.5		V_{CC} +1.6	V
6-2	WUS/SE sink current	I_{SEH}	b	b	b	b	b	a	a	a	a	b	b	a	a	a	a	b	a	Servo write enabled	5		14	mA
7	Read amplifier differential voltage gain	A_V	a	a	a	a	b	a	a	a	c	b	a	a	b	a	a	b	b	Input voltage SG1 : 1 mVp-p, 300 kHz Load resistance (RDX, RDY) : 1 kΩ Test point : V4 [Vp-p] $AV = \frac{V4}{SG1}$	355	420	485	V/V
8	Frequency band width (–3 dB)	BW	a	a	a	a	b	a	a	a	c	b	a	a	b	a	a	b	b	Frequency at which A_V lowers by 3 dB	100	140		MHz
9	Input referred noise	E_N	a	a	a	a	a	a	a	a	e	b	a	a	b	a	a	b	b	Head impedance : 0 Ω, when the read amplifier output voltage is amplified 100 times and voltage passed though a LPF (low pass filter of cutoff frequency 15 MHz) is V_N [Vrms], $EN = \frac{V_N}{100 \bullet AV\sqrt{15 \times 10^6}}$ Test point : V_5		0.46	0.65	$\frac{nV}{\sqrt{Hz}}$

No.	Item	Symbol	SW conditions																	Measurement conditions	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17					
10	Common mode rejection ration	CMRR	a	a	a	a	b	a	a	a	d	b	a	a	b	a	a	b	b	In-phase input voltage SG2 : 100 mVp-p, 20 MHz When the Read amplifier output is V_{CM} [mVp-p], $CMRR = 20 \log \frac{100}{V_{CM}} + 20 \log A_V$ Test point : V_4	50			dB
11	Power supply rejection ratio	PSRR	a	a	a	a	a	a	a	a	e	a	a	a	b	a	a	b	b	Ripple voltage SG3 : 100 mVp-p, 20 MHz When the Read amplifier output is V_P [mVp-p], $PSRR = 20 \log \frac{100}{V_P} + 20 \log A_V$ Test point : V_4	50			dB
12	Channel separation	CS	a	a	a	a	a	b	a	a	c	b	a	a	b	a	a	b	b	Selected head input voltage : 0 mVp-p Unselected head input voltage SG1 : 100 mVp-p, 20 MHz When the Read amplifier output is V_{CS} [mVp-p], $CS = 20 \log \frac{100}{V_{CS}} + 20 \log A_V$ Test point : V_4	50			dB
13	Read data output offset voltage for Read	V_{OFFR}	a	a	a	a	a	a	a	a	e	b	a	a	b	a	a	a	b	$V_{OFFR} = V_2 - V_3$ Test point : V_2, V_3	–300		300	mV

No.	Item	Symbol	SW conditions																	Measurement conditions	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17					
14	RDX, RDY common mode output voltage difference between modes	Vdiff	a	a	a	a	a	a	a	a	e	b	a	a	b	a	a	a	c	Test point : Pin 20, 21	–300		300	mV
15	RDX, RDY common mode output voltage for Read	V_{RD}	a	a	a	a	a	a	a	a	e	b	a	a	b	a	a	a	b	Test Point : V_2, V_3	V_{CC} –2.6	V_{CC} –2.3	V_{CC} –2.0	V

Unless otherwise specified, V_{CC}=5 V, Ta=25 °C, f_{WD} (Write data frequency) =5 MHz, I_W=20 mA, L_H (Head inductance) =1 µH, R_H (Head DC resistance value) =12 Ω

Refer to Fig. 2 to Fig. 4

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
14	Head differential voltage amplitude	V_{SW}	Differential voltage between HX pin and HY pin at switching of Write current		9		Vp-p
15-1	Mode switching time Read to Write	T_{RW}	T_{RW} is the time required for Write current to turn to 90 % after Pin 23 changes from “High” to “Low”.		130	150	ns
15-2	Mode switching time Write to Read	T_{WR1}	T_{WR1} is the time required for the Read amplifier output* to turn to 90 % after Pin 23 changes from “Low” to “High”.		180	220	ns
		T_{WR2}	T_{WR2} is the time required for Write current to decreases to 10 % after Pin 23 changes from “Low” to “High”.		100	200	ns
16-1	Mode switching time safe to unsafe	T_{SA1}	T_{SA1} is the time required for Pin 14 to turn “High” after the last transition of Write data when Write data is stopped in Write mode.	1.0	2.3	3	µs
16-2	Mode switching time unsafe to safe	T_{SA2}	T_{SA2} is the time required for Pin 14 to turn “Low” after the first transition of Write data in Write mode.			0.6	µs
17	Head switching time	T_H	T_H is the time required for the Read amplifier output* to reach 90 % when the selected head switched in Read mode.			0.6	µs
18	Write current propagation delay time	T_{PD}	T_{PD} is the time required for Write current to reach 90 % after the Write data falling edge. L_H=0 µH, R_H=0 Ω		2	7	ns
19	Write current rise/fall time	T_R/T_F	T_R is the time required for Write current to reach 90 % from 10 %; T_F is the same time required to reach 10 % from 90 %. L_H=0 µH, R_H=0 Ω		1	3	ns

*Read amplifier output 100 mVp-p 10 MHz

Test Circuit 1

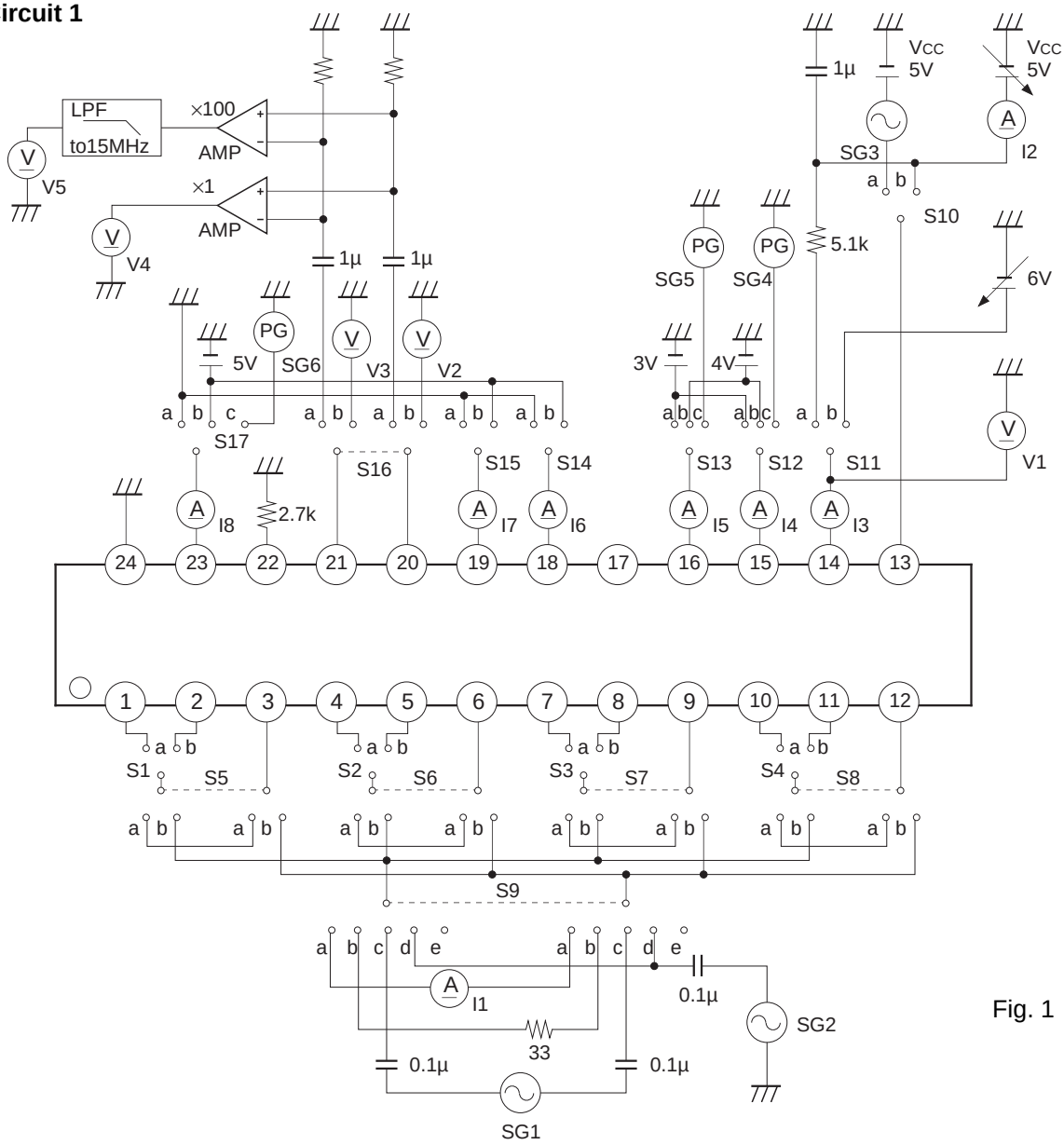


Fig. 1

Test Circuit 2

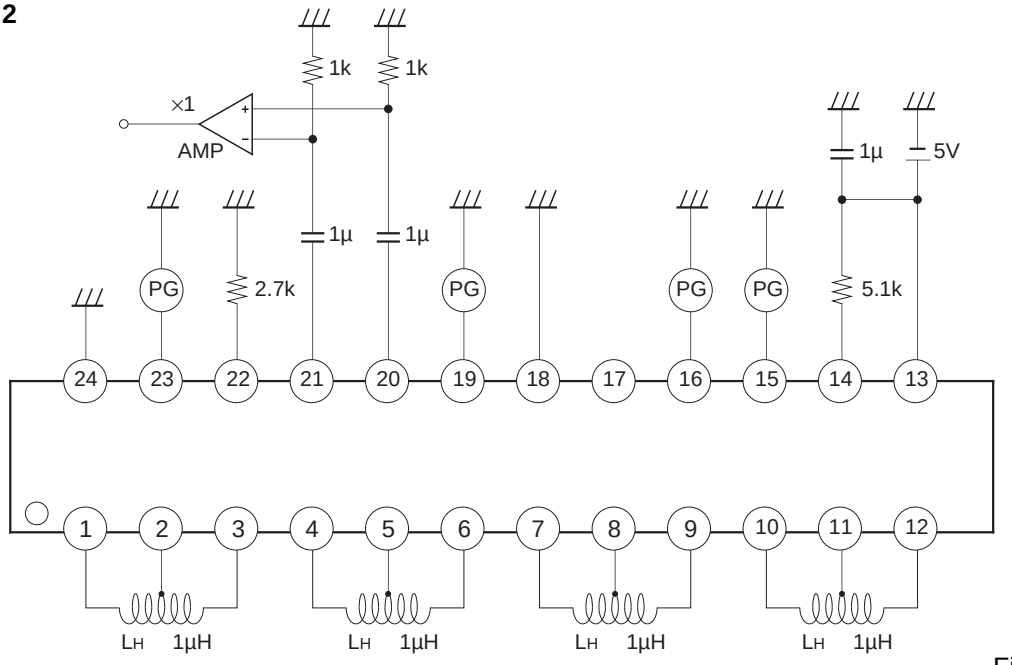


Fig. 2

Timing Chart 1

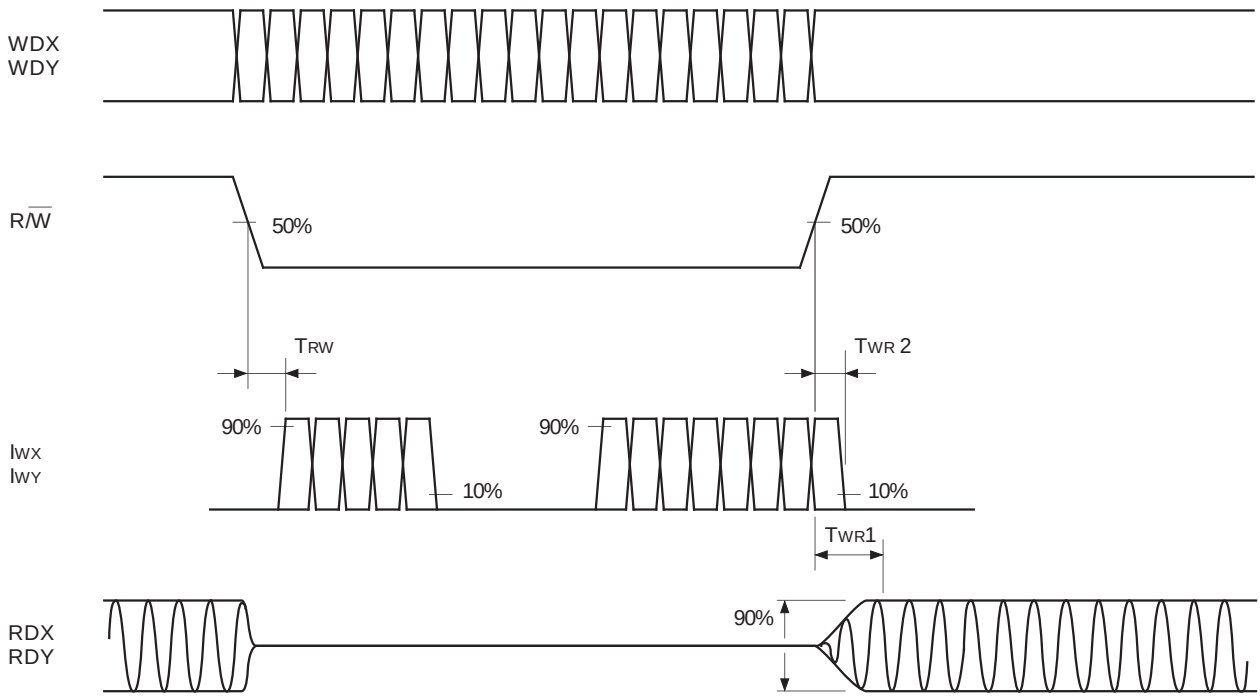


Fig. 3

Timing Chart 2

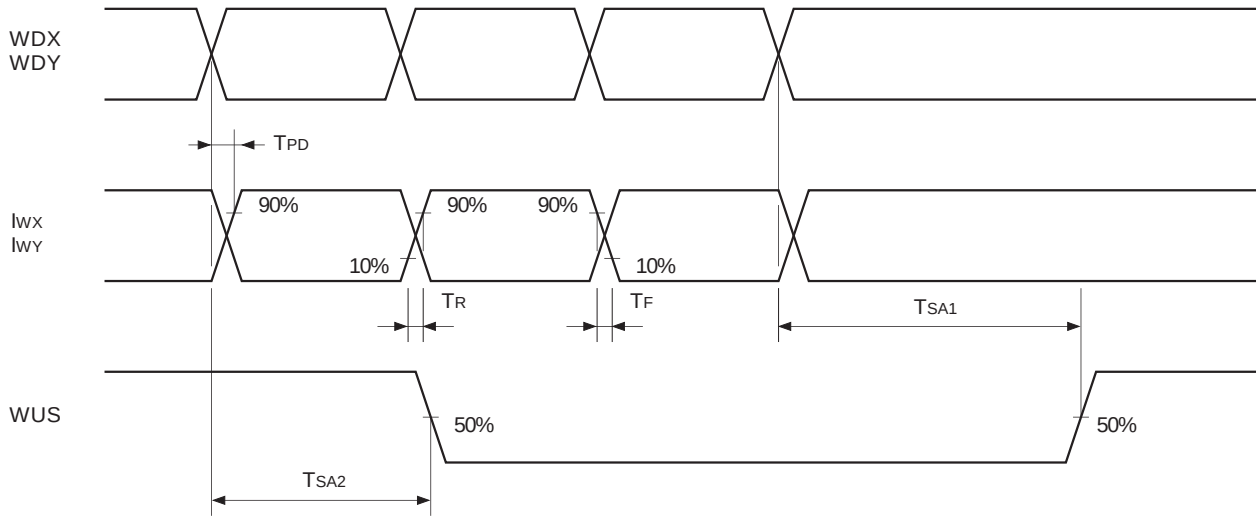


Fig. 4

Description Functions

Read amplifier

This is a low noise amplifier for amplifying the signals from the heads with an emitter follower output.

The RDX and RDY are the outputs of the differential amplifier whose polarity between the RDX and X side of the head input is same.

Write circuit

The Write data input to WDX pin and WDY pin passes through the buffer amp. It drives the Write switch circuit which supplies the Write current to the heads.

The Write current flows into the X side when WDX is “Low” and WDY is “High”.

Mode control

The mode are set as shown Table 1 by R/$\overline{W}$ and WUS/SE.

R/$\overline{W}$	WUS/SE	HS0	HS1	Mode
L	X	See Table 2		Write
H	X			Read
L	**	See Table 3		Servo Write

Table 1. Mode selection

Head selection

The heads are selected as shown in Table 2 by the HS0, HS1 and HS2 pins.

HS0	HS1	Head
L	L	0
H	L	1
L	H	2
H	H	3

Table 2. Head selection

Servo write mode **

This mode allows for writing to multiple channels at once.

To enable servo write mode follow these steps:

(1) Place the device in the Read mode.
(2) Set HS0 and HS1 following Table 3.
(3) Set WUS/SE to V_{SEH}, or input I_{SEH} to WUS/SE.
(4) While maintaing step (2) and (3) above make R/W low, placing the device in servo write mode.

Write unsafe detection circuit

This circuit detects write errors.

In normal Write mode, the WUS output is low; in the conditions listed below, it is high.

- Head inputs is open (under the condition which. RH=∞ and Write data frequency is ≤ 10 MHz)
- Head input is shorted to GND or VCC.
- Write data frequency is abnormally low.
- No write current.
- In read mode.
- Supply voltage is abnormal (see power supply ON/OFF detection).

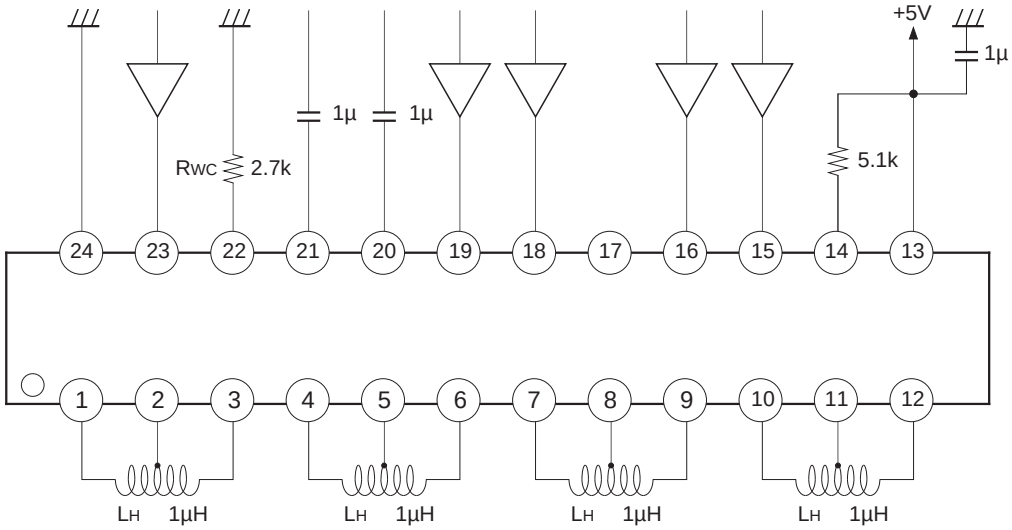
Power supply ON/OFF detection

This circuit monitors V_{CC} to detect erroneous Writes. The error status is established when V_{CC} falls below the threshold voltage (V_{TH}) of the power supply ON/OFF detector, in which case the recording and playback functions are prohibited. When V_{CC} rises above V_{TH}, the prohibition of these functions is released.

HS0	HS1	Head
L	L	0, 1
H	L	0, 1, 2, 3
L	H	2, 3
H	H	0, 1, 2, 3

Table 3. Head selection in Servo Write mode

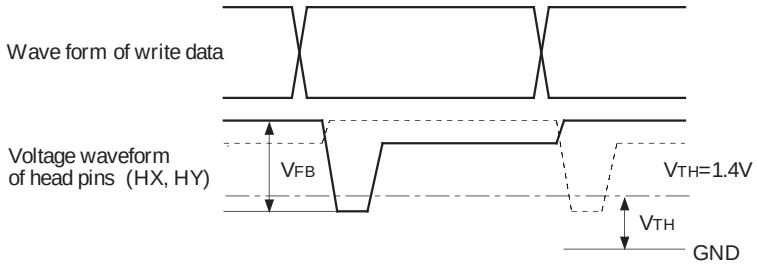
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on operation

- This device handles high frequency and high gain signals. Please note the following;
  - ♦ Connect V_{CC} decoupling capacitor of approximately 1000 pF near the device.
  - ♦ Make the GND area as large as possible.
- When using as 2-channel, short-circuit the X and Y sides of unused head pins or leave them open.
- The WC pin is a constant voltage pin. When noise affects this pin, it creates noise in Write c current. Therefore, locate R_{WC} as close to the device as possible.
- Write unsafe detection circuit
  This circuit uses the voltage waveforms of the head pins for detection.



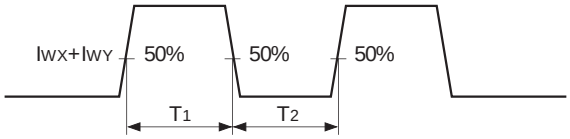
  - ♦ VFB must be more than 2 V. When V_{FB} < 2 V, it is possible that Write unsafe detection maximum frequency becomes more than 1 MHz.
  - ♦ The normal operating area of write unsafe detection circuit is changed by head inductance, head DC resistance, write current and other.

Application Notes

Use the following characteristics for reference. V_{CC}=5V, Ta=25 °C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Write mode	Differential output capacitance	C_O	Between head input pins		4.5	6	pF
	Differential output resistance	R_O		300	420	545	Ω
Read mode	Differential input capacitance	C_I	Between head input pins		6.7	10	pF
	Differential input resistance	R_I	f=5 MHz	520	1200	2400	Ω
	Output resistance	R_{RD}	RDX or RDY, f=5 MHz			50	Ω
Unselected head differential current in Write mode		I_{US}	L_H=1 µH, R_H=12 Ω I_W=20 mA			0.2	mAp-p
Write current symmetry		T_{AS}*	L_H=0 µH, R_H=0 Ω I_W=20 mA	–0.5		0.5	ns

*TAS=T_1–T_2



Setting of Write current

Write current can be set with resistor R_{WC} (kΩ) at Pin 22.

I_W=K/R_{WC} (mA) Refer to Fig. 5.

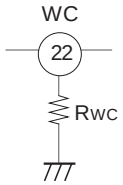
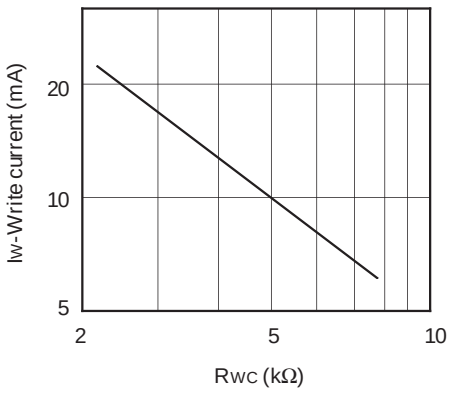
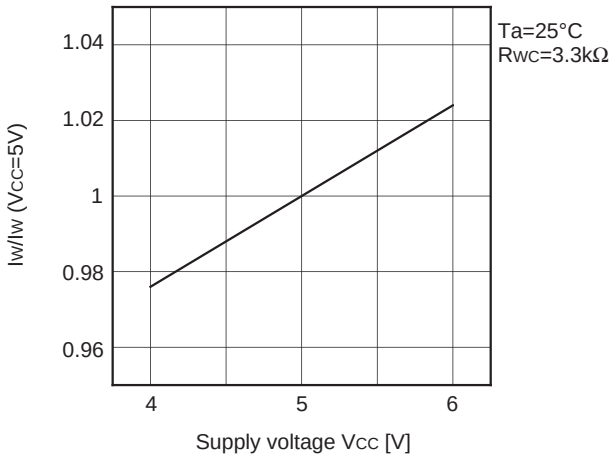


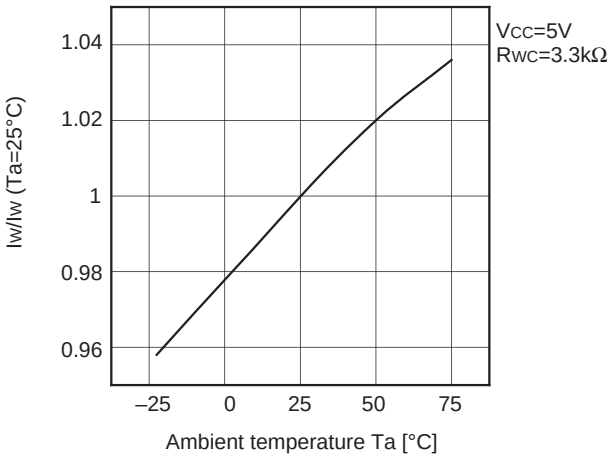
Fig.5 Write current vs. R_{WC}



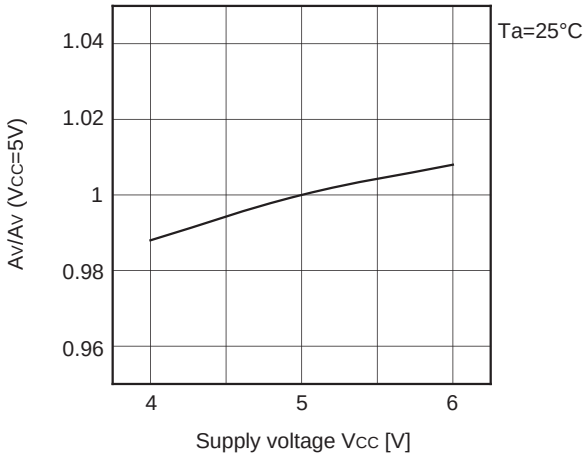
Normalized write current
vs. Supply voltage



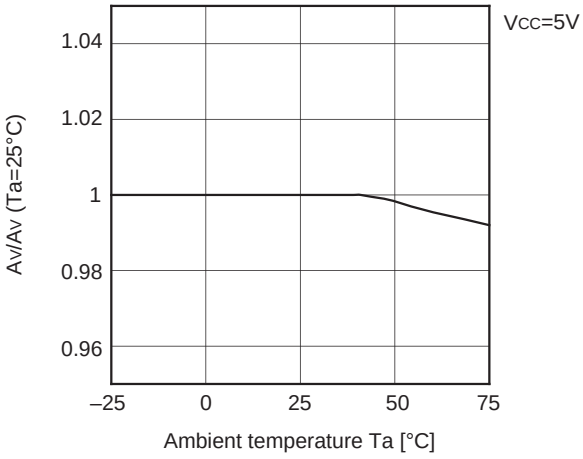
Normalized write current
vs. Ambient temperature



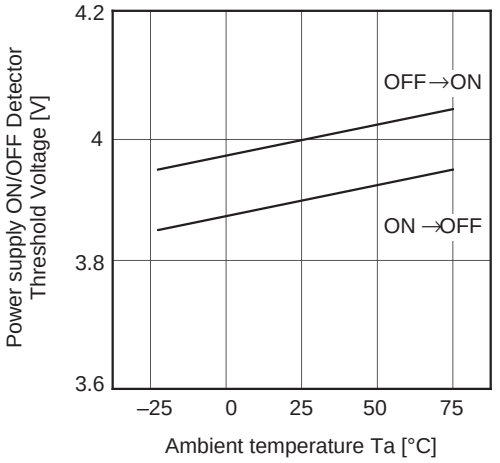
Normalized read amplifier voltage tgain
vs. Supply voltage



Normalized read amplifier voltage gain
vs. Ambient temperature

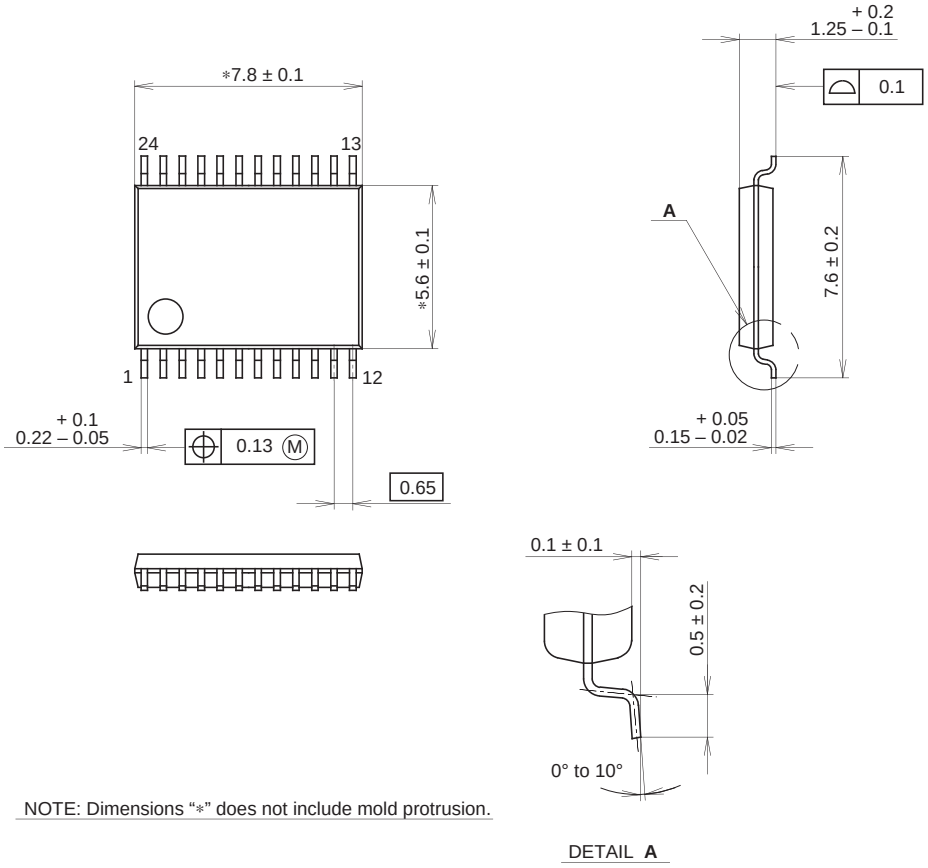


Power supply ON/OFF detector threshold
voltage vs. Ambient temperature



Package Outline Unit : mm

24PIN SSOP(PLASTIC)



NOTE: Dimensions "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).