19-3153; Rev 0; 1/04

1.8Msps, Single-Supply, Low-Power, True-Differential, 10-Bit ADCs

General Description

The MAX1072/MAX1075 low-power, high-speed, serial-output, 10-bit, analog-to-digital converters (ADCs) operate at up to 1.8Msps. These devices feature true-differential inputs, offering better noise immunity, distortion improvements, and a wider dynamic range over single-ended inputs. A standard SPI™/QSPI™/MICROWIRE™ interface provides the clock necessary for conversion. These devices easily interface with standard digital signal processor (DSP) synchronous serial interfaces.

The MAX1072/MAX1075 operate from a single +4.75V to +5.25V supply voltage and require an external reference. The MAX1072 has a unipolar analog input, while the MAX1075 has a bipolar analog input. These devices feature a partial power-down mode and a full power-down mode for use between conversions, which lower the supply current to 1mA (typ) and 1µA (max), respectively. Also featured is a separate power-supply input (V_L), which allows direct interfacing to +1.8V to V_{DD} digital logic. The fast conversion speed, low-power dissipation, excellent AC performance, and DC accuracy (±0.5 LSB INL) make the MAX1072/MAX1075 ideal for industrial process control, motor control, and base-station applications.

The MAX1072/MAX1075 come in a 12-pin TQFN package, and are available in the commercial (0°C to +70°C) and extended (-40°C to +85°C) temperature ranges.

Applications

Data Acquisition

Bill Validation

Motor Control

Communications

Portable Instruments

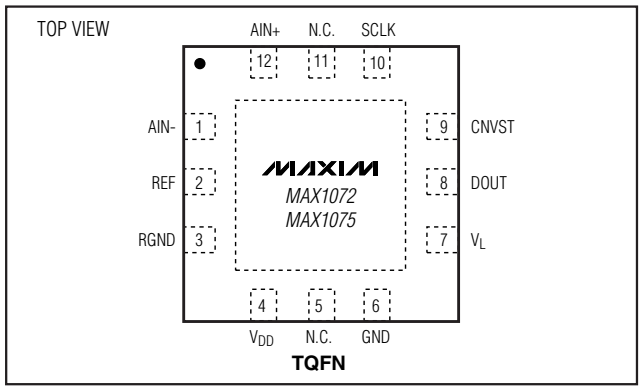
Features

- **1.8Msps Sampling Rate**
- **Only 45mW (typ) Power Dissipation**
- **Only 1µA (max) Shutdown Current**
- **High-Speed, SPI-Compatible, 3-Wire Serial Interface**
- **61dB S/(N + D) at 525kHz Input Frequency**
- **Internal True-Differential Track/Hold (T/H)**
- **External Reference**
- **No Pipeline Delays**
- **Small 12-Pin TQFN Package**

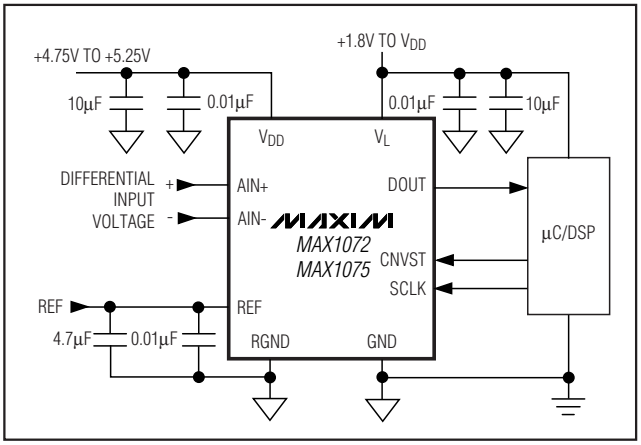
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INPUT
MAX1072CTC-T	0°C to +70°C	12 TQFN-12	Unipolar
MAX1072ETC-T	-40°C to +85°C	12 TQFN-12	Unipolar
MAX1075CTC-T	0°C to +70°C	12 TQFN-12	Bipolar
MAX1075ETC-T	-40°C to +85°C	12 TQFN-12	Bipolar

Pin Configuration



Typical Operating Circuit



SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

1.8Msps, Single-Supply, Low-Power, True-Differential, 10-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
V_L to GND .....-0.3V to the lower of (V_{DD} + 0.3V) or +6V
Digital Inputs
to GND .....-0.3V to the lower of (V_{DD} + 0.3V) or +6V
Digital Output
to GND .....-0.3V to the lower of (V_L + 0.3V) or +6V
Analog Inputs and
REF to GND.....-0.3V to the lower of (V_{DD} + 0.3V) or +6V
RGND to GND .....-0.3V to +0.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
12-Pin TQFN (derate 16.9mW/°C above +70°C) 1349mW
Operating Temperature Ranges
MAX107_ CTC .....0°C to +70°C
MAX107_ ETC.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_L = V_{DD}, V_{REF} = 4.096V, f_{SCLK} = 28.8MHz, 50% duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			10			Bits
Relative Accuracy	INL	(Note 1)			±0.5	LSB
Differential Nonlinearity	DNL	(Note 2)			±0.5	LSB
Offset Error					±2	LSB
Offset-Error Temperature Coefficient				±1		ppm/°C
Gain Error		Offset nulled			±2	LSB
Gain Temperature Coefficient				±2		ppm/°C
DYNAMIC SPECIFICATIONS (f_{IN} = 525kHz sine wave, V_{IN} = V_{REF}, unless otherwise noted.)						
Signal-to-Noise Plus Distortion	SINAD		60	61		dB
Total Harmonic Distortion	THD			-80	-74	dB
Spurious-Free Dynamic Range	SFDR			-80	-74	dB
Intermodulation Distortion	IMD	f_{IN1} = 250kHz, f_{IN2} = 300kHz		-78		dB
Full-Power Bandwidth		-3dB point, small-signal method		20		MHz
Full-Linear Bandwidth		S/(N + D) Σ 56dB, single ended		2		MHz
CONVERSION RATE						
Minimum Conversion Time	t_{CONV}	(Note 3)			0.556	µs
Maximum Throughput Rate			1.8			Msps
Minimum Throughput Rate		(Note 4)	10			ksps
Track-and-Hold Acquisition Time	t_{ACQ}	(Note 5)		104		ns
Aperture Delay				5		ns
Aperture Jitter		(Note 6)		30		ps
External Clock Frequency	f_{SCLK}				28.8	MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_L = V_{DD}, V_{REF} = 4.096V, f_{SCLK} = 28.8MHz, 50% duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS (AIN+, AIN-)						
Differential Input Voltage Range	V_{IN}	AIN+ - AIN-, MAX1072	0		V_{REF}	V
		AIN+ - AIN-, MAX1075	-V_{REF} / 2		+V_{REF} / 2	
Absolute Input Voltage Range			0		V_{DD}	V
DC Leakage Current					±1	µA
Input Capacitance		Per input pin		20		pF
Input Current (Average)		Time averaged at maximum throughput rate		75		µA
REFERENCE INPUT (REF)						
REF Input Voltage Range	V_{REF}		1.0		V_{DD} + 50mV	V
Input Capacitance				20		pF
DC Leakage Current					±1	µA
Input Current (Average)		Time averaged at maximum throughput rate		400		µA
DIGITAL INPUTS (SCLK, CNVST)						
Input Voltage Low	VIL				0.3 x V_L	V
Input Voltage High	VIH		0.7 x V_L			V
Input Leakage Current	I_{IL}			0.05	±10	µA
DIGITAL OUTPUT (DOUT)						
Output Load Capacitance	C_{OUT}	For stated timing performance			30	pF
Output Voltage Low	V_{OL}	I_{SINK} = 5mA, V_L ≥ 1.8V			0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA, V_L ≥ 1.8V	V_L - 0.5V			V
Output Leakage Current	I_{OL}	Output high impedance		±0.2	±10	µA
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		4.75		5.25	V
Digital Supply Voltage	V_L		1.8		V_{DD}	V
Analog Supply Current, Normal Mode	I_{DD}	Static, f_{SCLK} = 28.8MHz		7	9	mA
		Static, no SCLK		4	5	
		Operational, 1.8Msps		9	11	
Analog Supply Current, Partial Power-Down Mode	I_{DD}	f_{SCLK} = 28.8MHz		1		mA
		No SCLK		1		
Analog Supply Current, Full Power-Down Mode	I_{DD}	f_{SCLK} = 28.8MHz		1		µA
		No SCLK			1	
Digital Supply Current (Note 7)		Operational, full-scale input at 1.8Msps		1	2.5	mA
		Static, f_{SCLK} = 28.8MHz		0.4	1	
		Partial/full power-down mode, f_{SCLK} = 28.8MHz		0.2	0.5	
		Static, no SCLK (all modes)		0.1	1	µA
Positive-Supply Rejection	PSR	V_{DD} = 5V ±5%, full-scale input		±0.2	±3.0	mV

1.8Msps, Single-Supply, Low-Power, True-Differential, 10-Bit ADCs

TIMING CHARACTERISTICS

(V_{DD} = +5V ±5%, V_L = V_{DD}, V_{REF} = 4.096V, f_{SCLK} = 28.8MHz, 50% duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse-Width High	t_{CH}	V_L = 1.8V to V_{DD}	15.6			ns
SCLK Pulse-Width Low	t_{CL}	V_L = 1.8V to V_{DD}	15.6			ns
SCLK Rise to DOUT Transition	t_{DOUT}	C_L = 30pF, V_L = 4.75V to V_{DD}			14	ns
		C_L = 30pF, V_L = 2.7V to V_{DD}			17	
		C_L = 30pF, V_L = 1.8V to V_{DD}			24	
DOUT Remains Valid After SCLK	t_{DHOLD}	V_L = 1.8V to V_{DD}	4			ns
CNVST Fall to SCLK Fall	t_{SETUP}	V_L = 1.8V to V_{DD}	10			ns
CNVST Pulse Width	t_{CSW}	V_L = 1.8V to V_{DD}	20			ns
Power-Up Time; Full Power-Down	T_{PWR-UP}			2		ms
Restart Time; Partial Power-Down	t_{RCV}			16		Cycles

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and the offset error have been nulled.

Note 2: No missing codes over temperature.

Note 3: Conversion time is defined as the number of clock cycles (16) multiplied by the clock period.

Note 4: At sample rates below 10ksps, the input full-linear bandwidth is reduced to 5kHz.

Note 5: The listed value of three SCLK cycles is given for full-speed continuous conversions. Acquisition time begins on the 14th rising edge of SCLK and terminates on the next falling edge of CNST. The IC idles in acquisition mode between conversions.

Note 6: Undersampling at the maximum signal bandwidth requires the minimum jitter spec for SINAD performance.

Note 7: Digital supply current is measured with the V_{IH} level equal to V_L, and the V_{IL} level equal to GND.

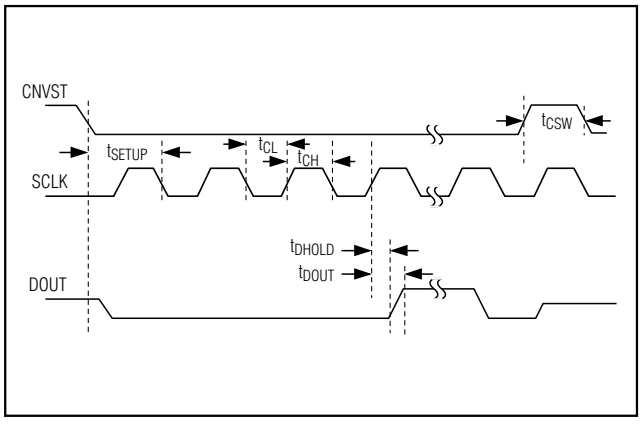


Figure 1. Detailed Serial-Interface Timing

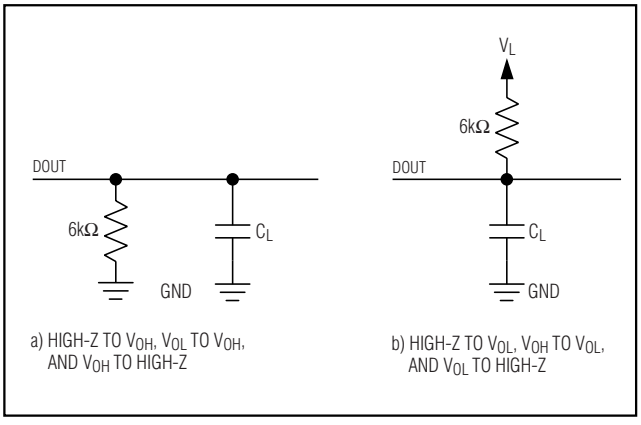
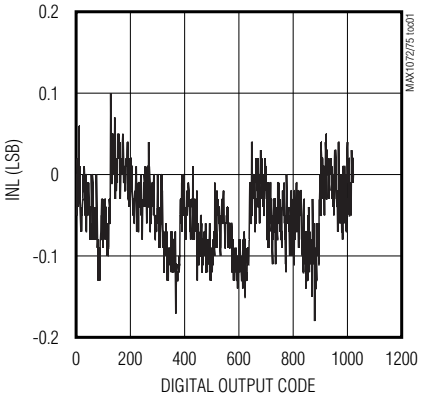


Figure 2. Load Circuits for Enable/Disable Times

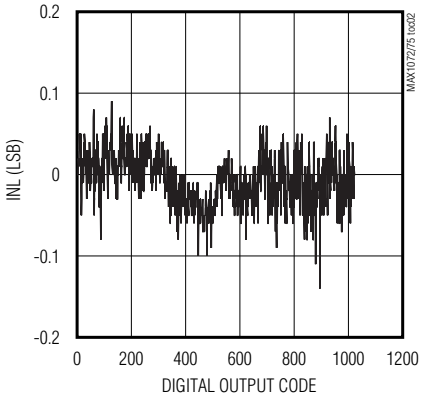
Typical Operating Characteristics

(V_{DD} = +5V, V_L = V_{DD}, V_{REF} = 4.096V, f_{SCLK} = 28.8MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

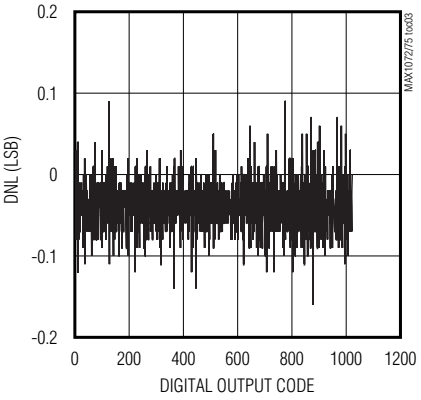
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (MAX1072)



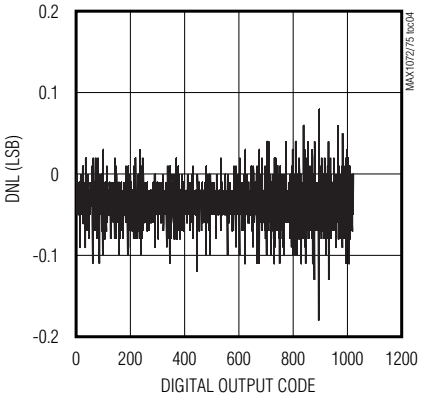
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (MAX1075)



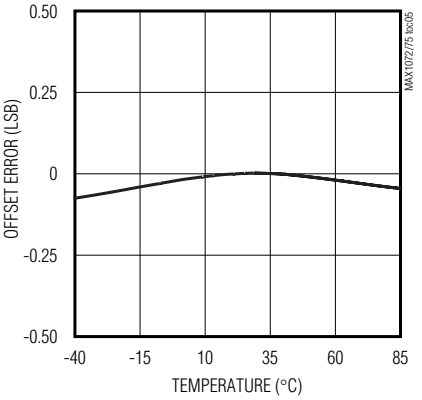
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE (MAX1072)



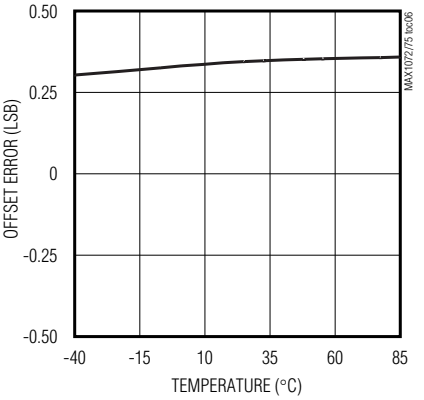
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE (MAX1075)



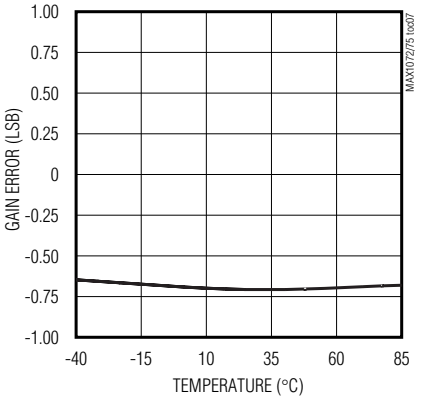
OFFSET ERROR vs. TEMPERATURE (MAX1072)



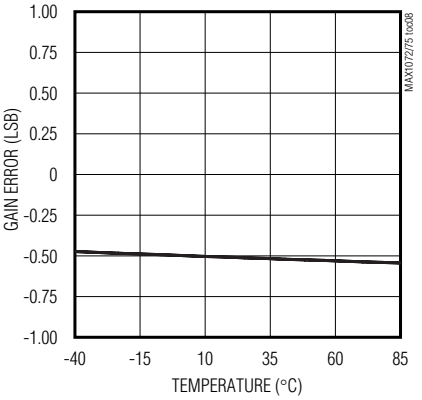
OFFSET ERROR vs. TEMPERATURE (MAX1075)



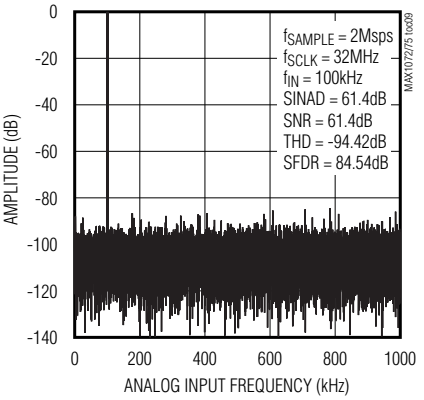
GAIN ERROR vs. TEMPERATURE (MAX1072)



GAIN ERROR vs. TEMPERATURE (MAX1075)



FFT PLOT (MAX1072)

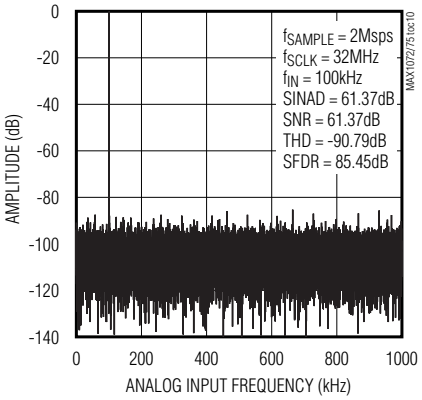


1.8Msps, Single-Supply, Low-Power, True-Differential, 10-Bit ADCs

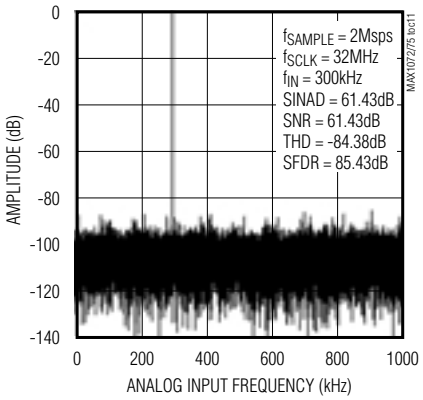
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_L = V_{DD}, V_{REF} = 4.096V, f_{SCLK} = 28.8MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

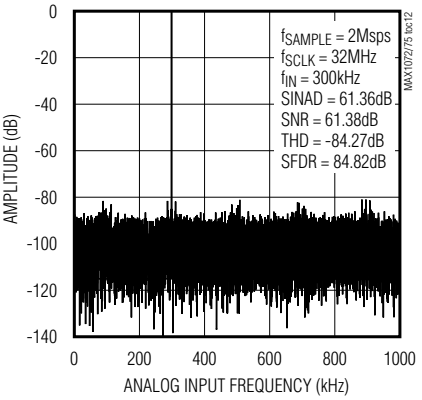
FFT PLOT (MAX1075)



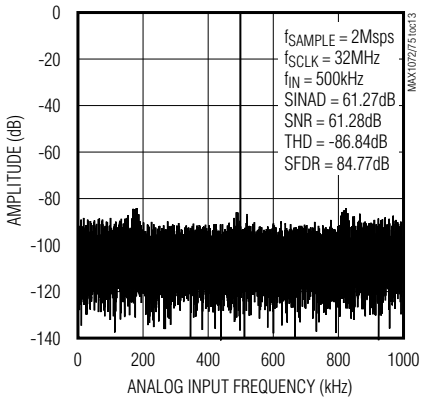
FFT PLOT (MAX1072)



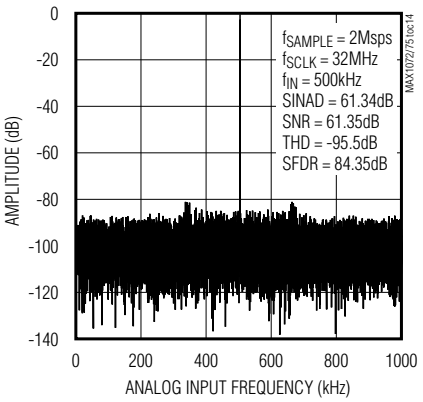
FFT PLOT (MAX1075)



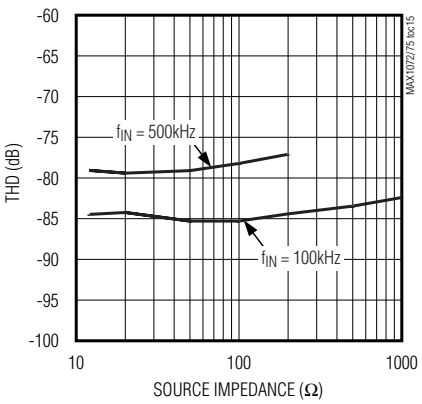
FFT PLOT (MAX1072)



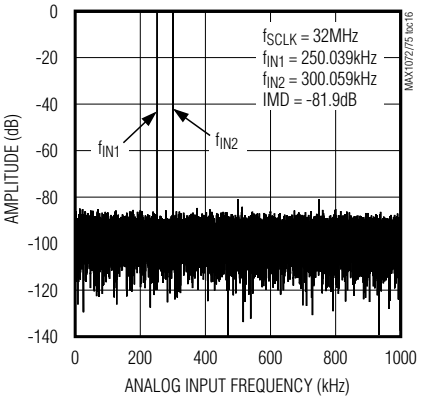
FFT PLOT (MAX1075)



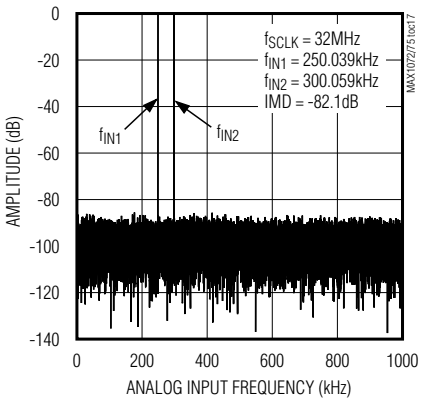
TOTAL HARMONIC DISTORTION vs. SOURCE IMPEDANCE



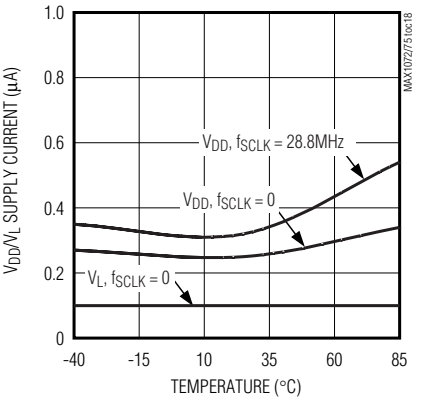
TWO-TONE IMD PLOT (MAX1072)



TWO-TONE IMD PLOT (MAX1075)



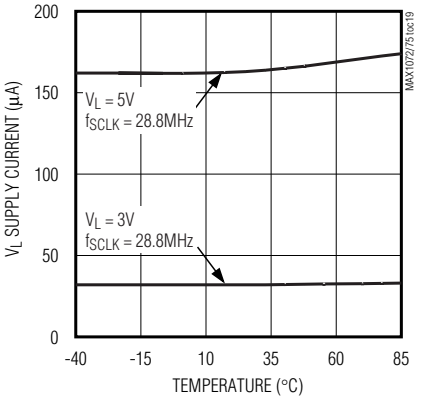
V_{DD}/V_L FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



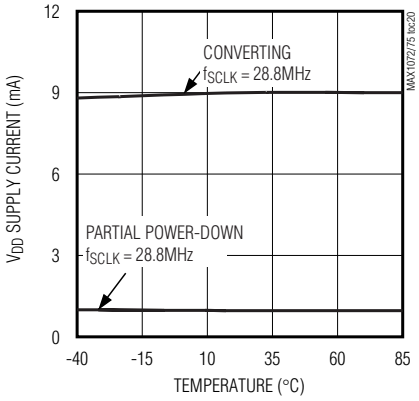
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_L = V_{DD}, V_{REF} = 4.096V, f_{SCLK} = 28.8MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

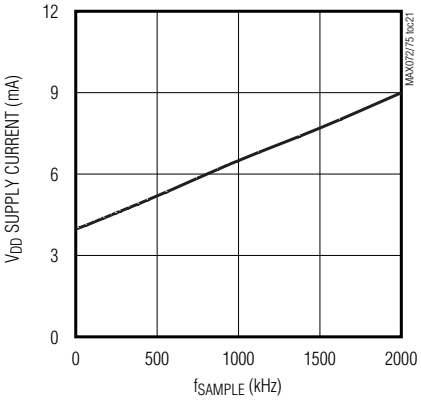
V_L PARTIAL/FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



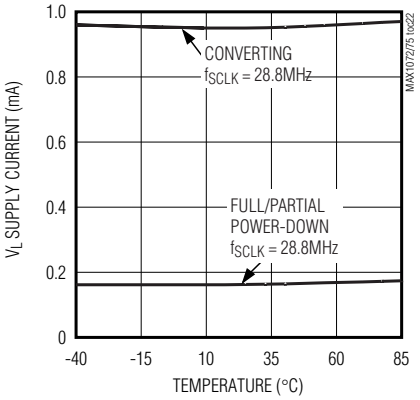
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



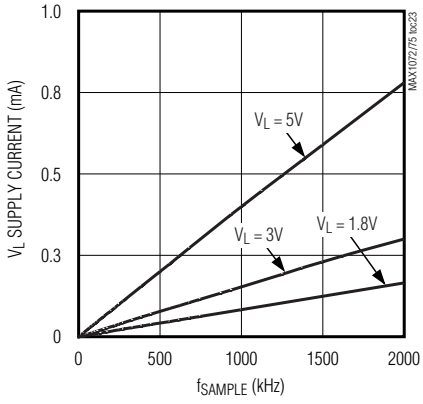
V_{DD} SUPPLY CURRENT vs. CONVERSION RATE



V_L SUPPLY CURRENT vs. TEMPERATURE



V_L SUPPLY CURRENT vs. CONVERSION RATE



1.8Msps, Single-Supply, Low-Power, True-Differential, 10-Bit ADCs

Pin Description

PIN	NAME	FUNCTION
1	AIN-	Negative Analog Input
2	REF	External Reference Voltage Input. V_{REF} sets the analog input range. Bypass REF with a 0.01µF capacitor and a 4.7µF capacitor to RGND.
3	RGND	Reference Ground. Connect RGND to GND.
4	V_{DD}	Positive Analog Supply Voltage (+4.75V to +5.25V). Bypass V_{DD} with a 0.01µF capacitor and a 10µF capacitor to GND.
5, 11	N.C.	No Connection
6	GND	Ground. GND is internally connected to EP.
7	V_L	Positive Logic Supply Voltage (1.8V to V_{DD}). Bypass V_L with a 0.01µF capacitor and a 10µF capacitor to GND.
8	DOUT	Serial Data Output. Data is clocked out on the rising edge of SCLK.
9	CNVST	Convert Start. Forcing CNVST high prepares the part for a conversion. Conversion begins on the falling edge of CNVST. The sampling instant is defined by the falling edge of CNVST.
10	SCLK	Serial Clock Input. Clocks data out of the serial interface. SCLK also sets the conversion speed.
12	AIN+	Positive Analog Input
—	EP	Exposed Paddle. EP is internally connected to GND.

Detailed Description

The MAX1072/MAX1075 use an input T/H and successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 10-bit output. The serial interface requires only three digital lines (SCLK, CNVST, and DOUT) and provides easy interfacing to microprocessors (µPs) and DSPs. Figure 3 shows the simplified internal structure for the MAX1072/MAX1075.

True-Differential Analog Input T/H

The equivalent circuit of Figure 4 shows the input architecture of the MAX1072/MAX1075, which is composed of a T/H, a comparator, and a switched-capacitor digital-to-analog converter (DAC). The T/H enters its tracking mode on the 14th SCLK rising edge of the previous conversion. Upon power-up, the T/H enters its tracking mode immediately. The positive input capacitor is connected to AIN+. The negative input capacitor is connected to AIN-. The T/H enters its hold mode on the falling edge of CNVST and the difference between the sampled positive and negative input voltages is converted. The time required for the T/H to acquire an input signal is determined by how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} \geq 8 \times (RS + R_{IN}) \times 16pF$$

where $R_{IN} = 200\Omega$, and RS is the source impedance of the input signal.

Note: t_{ACQ} is never less than 104ns and any source impedance below 12Ω does not significantly affect the ADC's AC performance.

Input Bandwidth

The ADC's input-tracking circuitry has a 20MHz small-signal bandwidth, making it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes that clamp the analog input to V_{DD} and GND allow the analog input pins to swing from GND - 0.3V to V_{DD} + 0.3V without damage. Both inputs must not exceed V_{DD} or be lower than GND for accurate conversions.

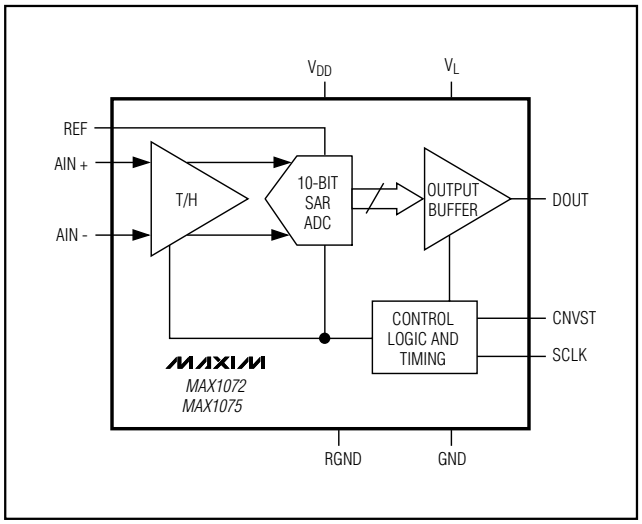


Figure 3. Functional Diagram

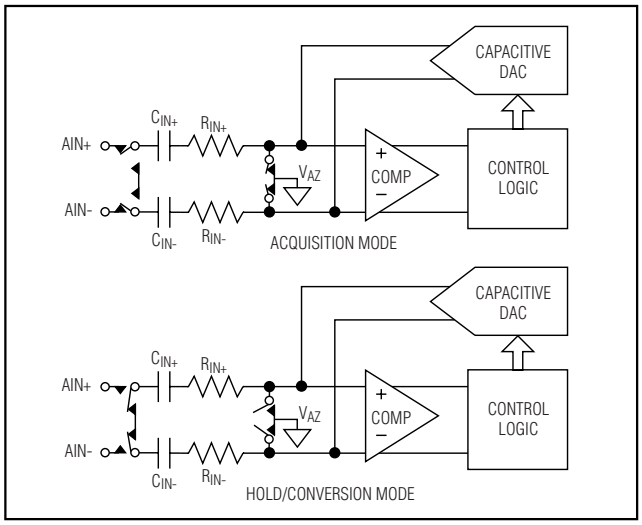


Figure 4. Equivalent Input Circuit

Serial Interface

Initialization After Power-Up and Starting a Conversion

Upon initial power-up, the MAX1072/MAX1075 require a complete conversion cycle to initialize the internal calibration. Following this initial conversion, the part is ready for normal operation. This initialization is only required after a hardware power-up sequence and is not required after exiting partial or full power-down mode.

To start a conversion, pull CNVST low. At CNVST's falling edge, the T/H enters its hold mode and a conversion is initiated. SCLK runs the conversion and the data can then be shifted out serially on DOUT.

Timing and Control

Conversion-start and data-read operations are controlled by the CNVST and SCLK digital inputs. Figures 1 and 5 show timing diagrams, which outline the serial-interface operation.

A CNVST falling edge initiates a conversion sequence; the T/H stage holds the input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK is used to drive the conversion process, and it shifts data out as each bit of the conversion is determined.

SCLK begins shifting out the data after the 4th rising edge of SCLK. DOUT transitions t_{DOUT} after each SCLK's rising edge and remains valid 4ns (t_{DHOLD}) after the next rising edge. The 4th rising clock edge produces the MSB of the conversion at DOUT, and the MSB remains valid 4ns after the 5th rising edge. Since there are 10 data bits, 2 sub-bits (S1 and S0), and 3 leading zeros, at least 16 rising clock edges are needed to shift out these bits. For continuous operation, pull CNVST high between the 14th and the 16th SCLK rising edges. If CNVST stays low after the falling edge of the 16th SCLK cycle, the DOUT line goes to a high-impedance state on either CNVST's rising edge or the next SCLK's rising edge.

Partial Power-Down and Full Power-Down Modes

Power consumption can be reduced significantly by placing the MAX1072/MAX1075 in either partial power-down mode or full power-down mode. Partial power-down mode is ideal for infrequent data sampling and fast wake-up time applications. Pull CNVST high after the 3rd SCLK rising edge and before the 14th SCLK rising edge to enter and stay in partial power-down mode (see Figure 6). This reduces the supply current to 1mA. Drive CNVST low and allow at least 14 SCLK cycles to elapse before driving CNVST high to exit partial power-down mode.

Full power-down mode is ideal for infrequent data sampling and very low supply current applications. The MAX1072/MAX1075 have to be in partial power-down mode in order to enter full power-down mode. Perform the SCLK/CNVST sequence described above to enter partial

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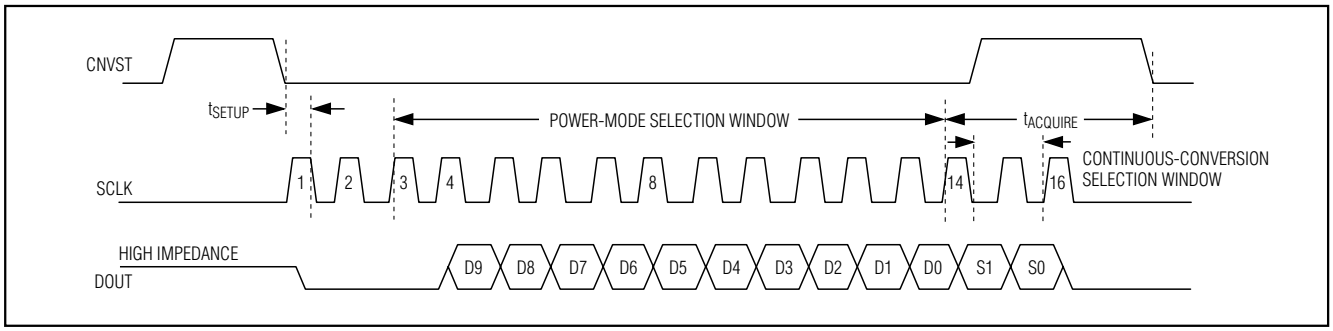

Figure 5. Interface-Timing Sequence

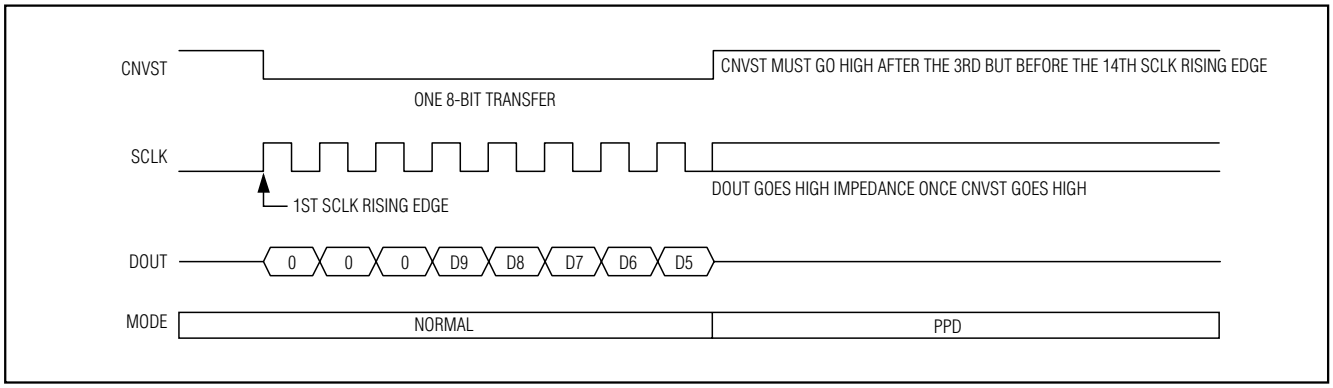

Figure 6. SPI Interface—Partial Power-Down Mode

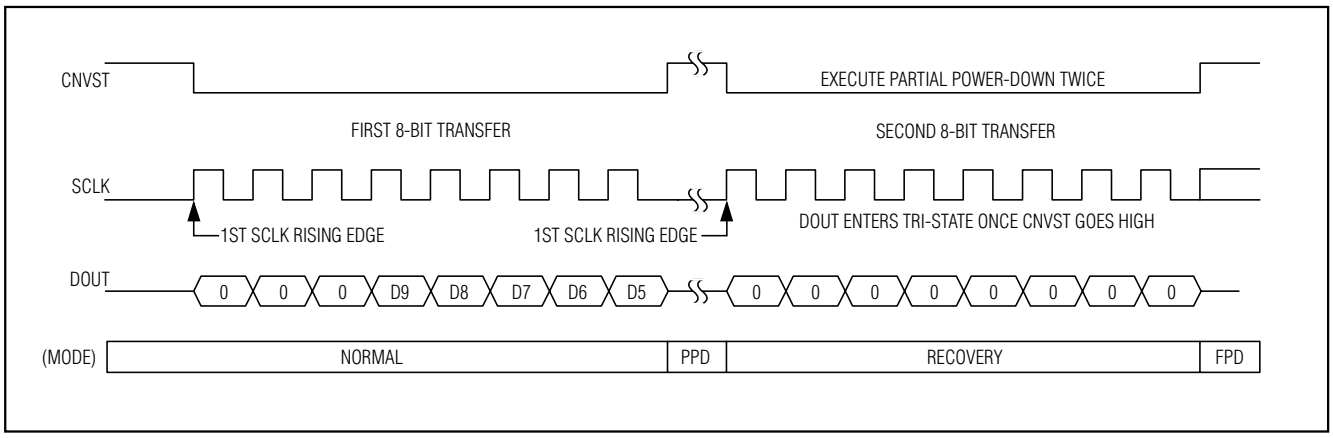

Figure 7. SPI Interface—Full Power-Down Mode

power-down mode. Then repeat the same sequence to enter full power-down mode (see Figure 7). Drive CNVST low, and allow at least 14 SCLK cycles to elapse before driving CNVST high to exit full power-down mode. In partial/full power-down mode, maintain a logic low or a logic high on SCLK to minimize power consumption.

Transfer Function

Figure 8 shows the unipolar transfer function for the MAX1072. Figure 9 shows the bipolar transfer function for the MAX1075. The MAX1072 output is straight binary, while the MAX1075 output is two's complement.

Applications Information

External Reference

An external reference is required for the MAX1072/MAX1075. Use a 4.7µF and 0.01µF bypass capacitor on the REF pin for best performance. The reference input structure allows a voltage range of +1V to V_{DD}.

How to Start a Conversion

An analog-to-digital conversion is initiated by CNVST, clocked by SCLK, and the resulting data is clocked out on DOUT by SCLK. With SCLK idling high or low, a falling edge on CNVST begins a conversion. This causes the analog input stage to transition from track to hold mode, and DOUT to transition from high impedance to being actively driven low. A total of 16 SCLK cycles are required to complete a normal conversion. If CNVST is low during the 16th falling SCLK edge, DOUT returns to high impedance on the next rising edge of CNVST or SCLK, enabling the serial interface to be shared by multiple devices. If CNVST returns high after the 14th, but before the 16th SCLK rising edge, DOUT remains active so continuous conversions can be sustained. The highest throughput is achieved when performing continuous conversions. Figure 10 illustrates a conversion using a typical serial interface.

Connection to Standard Interfaces

The MAX1072/MAX1075 serial interface is fully compatible with SPI/QSPI and MICROWIRE (see Figure 11). If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 28.8MHz.

SPI and MICROWIRE

When using SPI or MICROWIRE, the MAX1072/MAX1075 are compatible with all four modes programmed with the CPHA and CPOL bits in the SPI or MICROWIRE control register. Conversion begins with a CNVST falling edge. DOUT goes low, indicating a conversion is in progress. Two consecutive 1-byte reads are required to get the full 10 bits from the ADC. DOUT transitions on SCLK rising edges. DOUT is guaranteed to be valid t_{DOUT} later and remains valid until t_{DHOLD} after the following SCLK rising edge. When using CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1, the data is clocked into the µP on the following rising edge. When using CPOL = 0 and CPHA = 1 or CPOL = 1 and CPHA = 0, the data is clocked into the µP on the next falling edge. See Figure 11 for connections and Figures 12 and 13 for timing. See the *Timing Characteristics* section to determine the best mode to use.

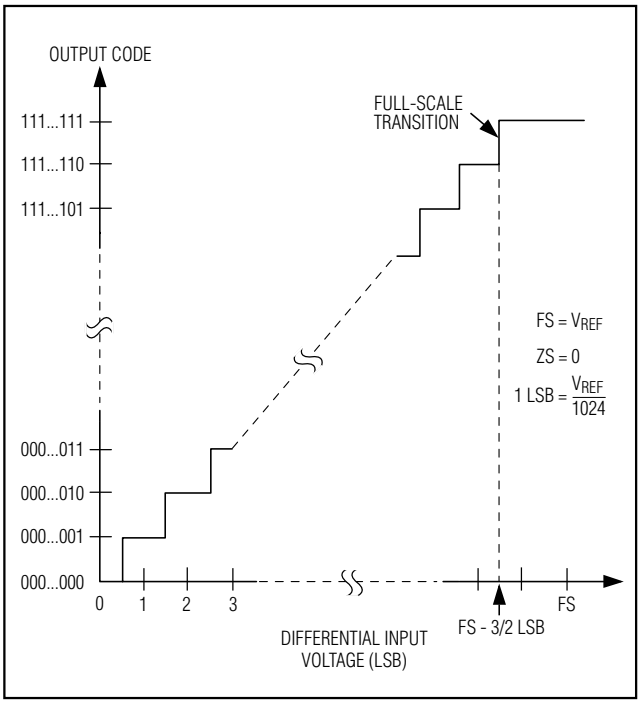

Figure 8. Unipolar Transfer Function (MAX1072 Only)

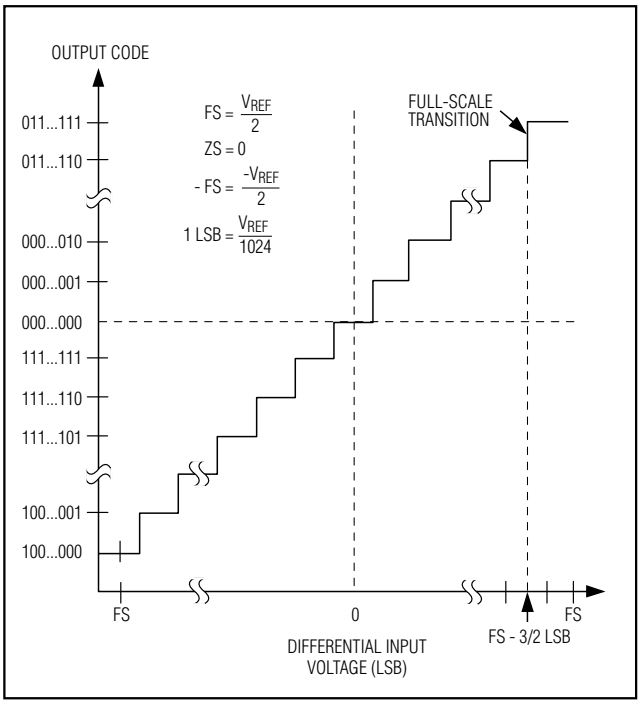

Figure 9. Bipolar Transfer Function (MAX1075 Only)

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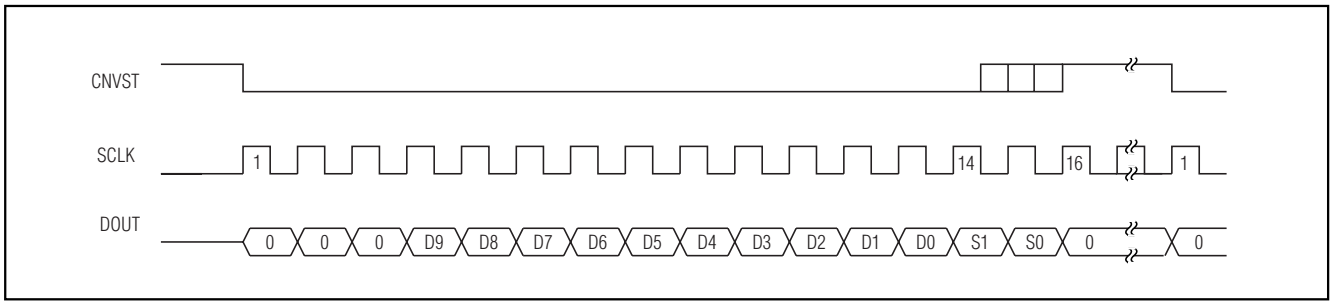

Figure 10. Continuous Conversion with Burst/Continuous Clock

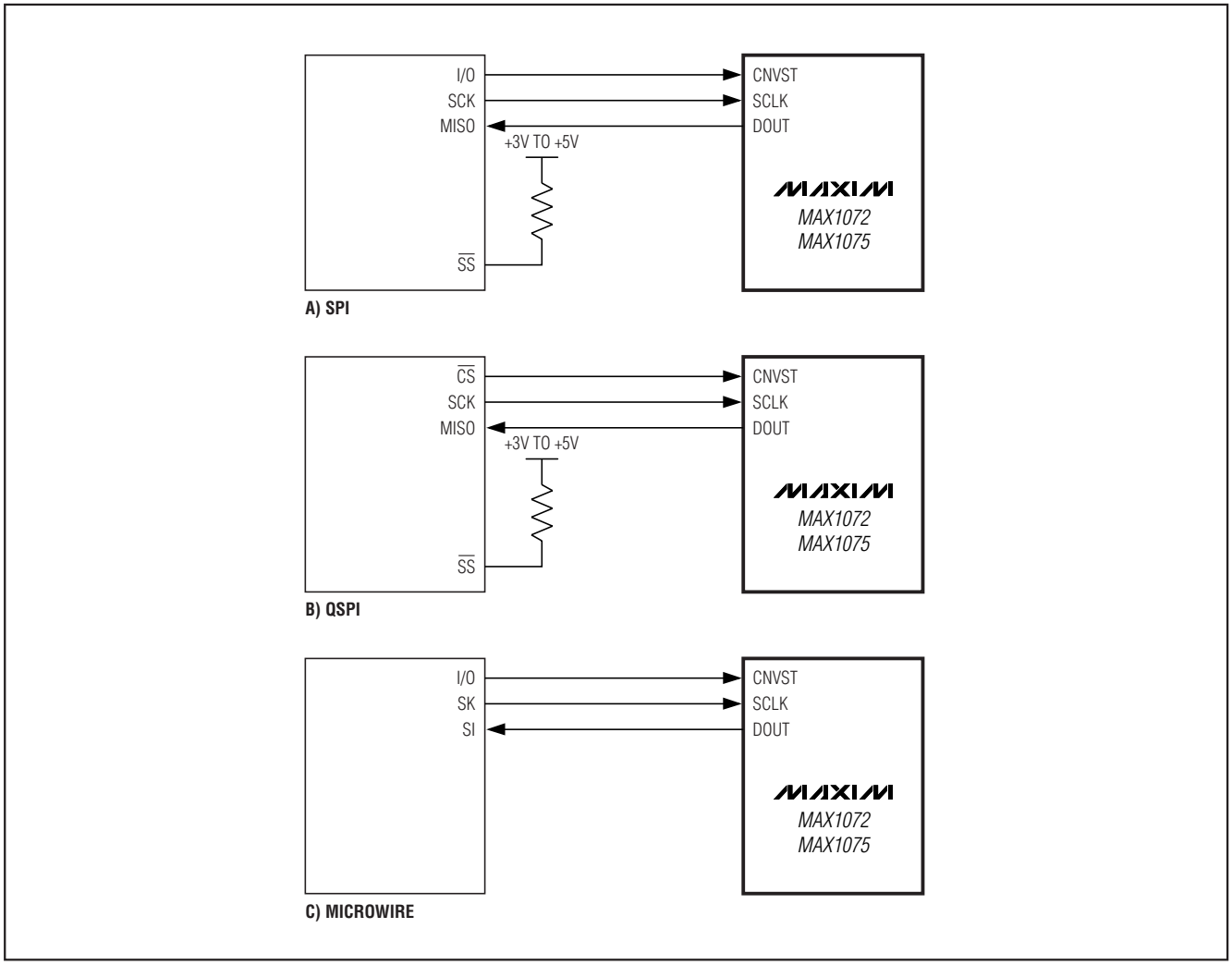

Figure 11. Common Serial-Interface Connections to the MAX1072/MAX1075

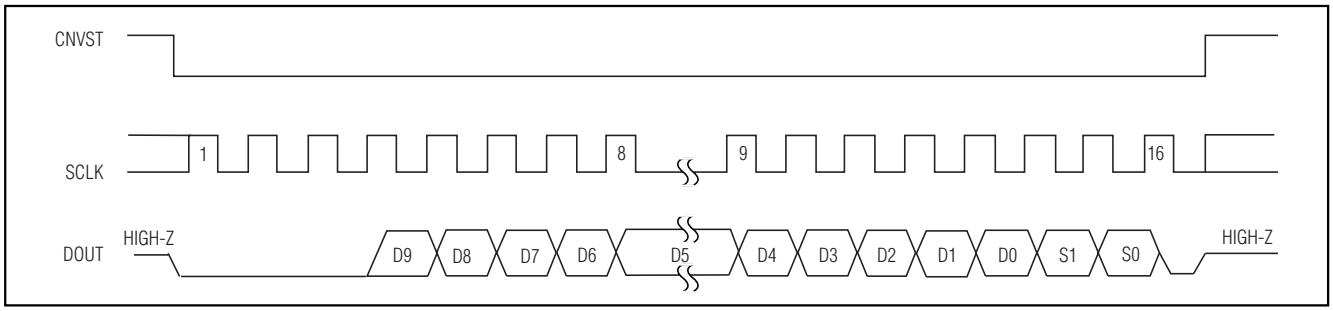

Figure 12. SPI/MICROWIRE Serial-Interface Timing—Single Conversion (CPOL = CPHA = 0), (CPOL = CPHA = 1)

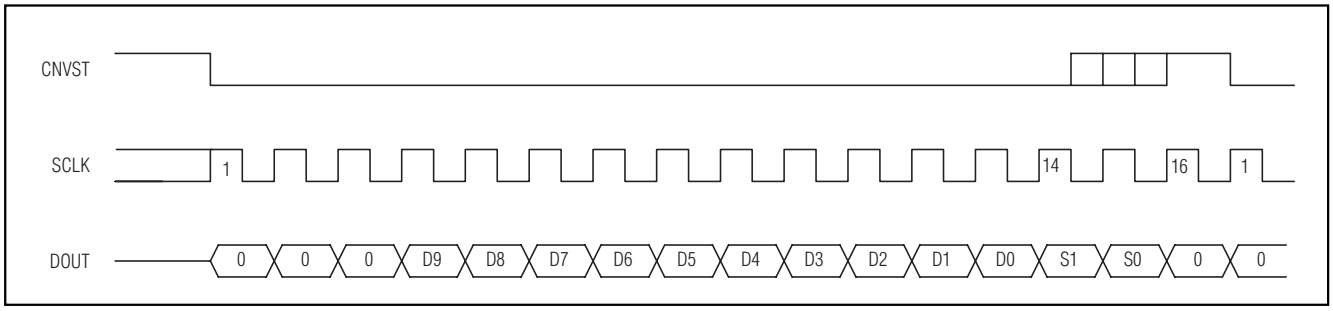

Figure 13. SPI/MICROWIRE Serial-Interface Timing—Continuous Conversion (CPOL = CPHA = 0), (CPOL = CPHA = 1)

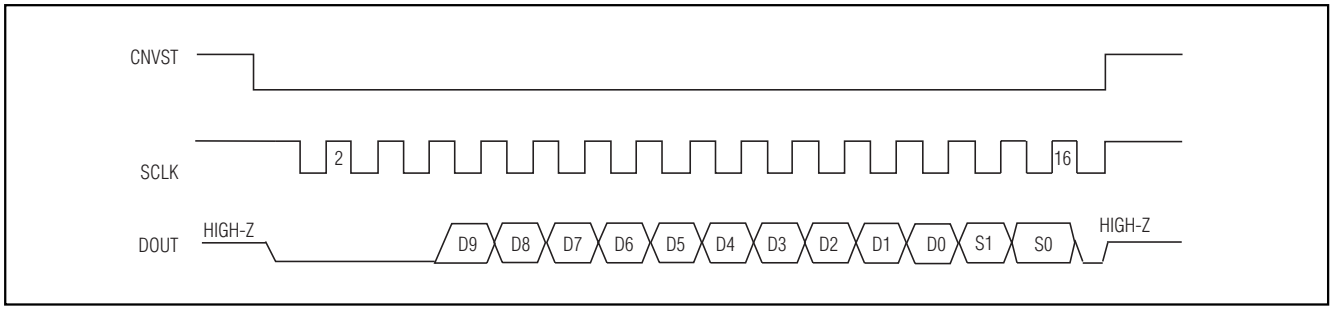

Figure 14. QSPI Serial-Interface Timing—Single Conversion (CPOL = 1, CPHA = 1)

QSPI

Unlike SPI, which requires two 1-byte reads to acquire the 10 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1072/MAX1075 require 16 clock cycles from the µP to clock out the 10 bits of data. Figure 14 shows a transfer using CPOL = 1 and CPHA = 1. The conversion result contains three zeros, followed by the 10 data bits, 2 sub-bits, and a trailing zero with the data in MSB-first format.

DSP Interface to the TMS320C54_

The MAX1072/MAX1075 can be directly connected to the TMS320C54_ family of DSPs from Texas Instruments, Inc. Set the DSP to generate its own clocks or use external clock signals. Use either the standard or buffered serial port. Figure 15 shows the simplest interface between the MAX1072/MAX1075 and the TMS320C54_, where the transmit serial clock (CLKX) drives the receive serial clock (CLKR) and SCLK, and the transmit frame sync (FSX) drives the receive frame sync (FSR) and CNVST.

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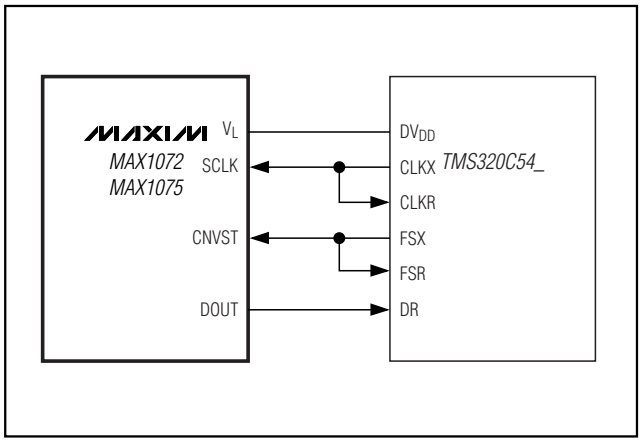

Figure 15. Interfacing to the TMS320C54_ Internal Clocks

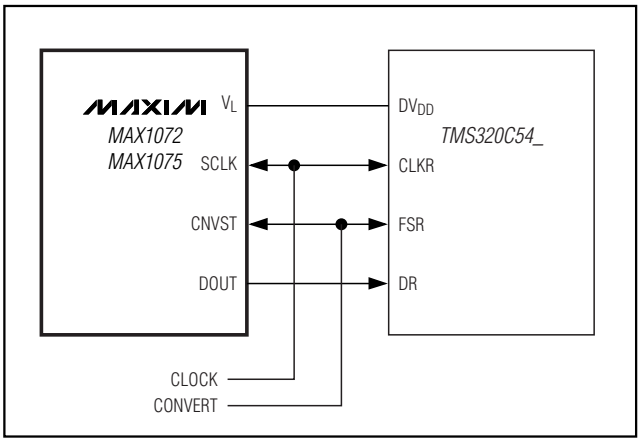

Figure 16. Interfacing to the TMS320C54_ External Clocks

For continuous conversion, set the serial port to transmit a clock, and pulse the frame sync signal for a clock period before data transmission. The serial-port configuration (SPC) register should be set up with internal frame sync (TXM = 1), CLKX driven by an on-chip clock source (MCM = 1), burst mode (FSM = 1), and 16-bit word length (FO = 0).

This setup allows continuous conversions provided that the data transmit register (DXR) and the data-receive register (DRR) are serviced before the next conversion. Alternatively, autobuffering can be enabled when using the buffered serial port to execute conversions and read the data without CPU intervention. Connect the V_L pin to the TMS320C54_ supply voltage when the MAX1072/MAX1075 are operating with an analog supply voltage higher than the DSP supply voltage. The word length can be set to 8 bits with FO = 1 to implement the power-down modes. The CNVST pin must idle high to remain in either power-down state.

Another method of connecting the MAX1072/MAX1075 to the TMS320C54_ is to generate the clock signals external to either device. This connection is shown in Figure 16 where serial clock (CLOCK) drives the CLKR and SCLK and the convert signal (CONVERT) drives the FSR and CNVST.

The serial port must be set up to accept an external receive-clock and external receive-frame sync.

The SPC register should be written as follows:

TXM = 0, external frame sync

MCM = 0, CLKX is taken from the CLKX pin

FSM = 1, burst mode

FO = 0, data transmitted/received as 16-bit words

This setup allows continuous conversion, provided that the DRR is serviced before the next conversion. Alternatively, autobuffering can be enabled when using the buffered serial port to read the data without CPU intervention. Connect the V_L pin to the TMS320C54_ supply voltage when the MAX1072/MAX1075 are operating with an analog supply voltage higher than the DSP supply voltage.

The MAX1072/MAX1075 can also be connected to the TMS320C54_ by using the data transmit (DX) pin to drive CNVST and the CLKX generated internally to drive SCLK. A pullup resistor is required on the CNVST signal to keep it high when DX goes high impedance and 0001hex should be written to the DXR continuously for continuous conversions. The power-down modes may be entered by writing 00FFhex to the DXR (see Figures 17 and 18).

DSP Interface to the ADSP21_ _ _

The MAX1072/MAX1075 can be directly connected to the ADSP21_ _ _ family of DSPs from Analog Devices, Inc. Figure 19 shows the direct connection of the MAX1072/MAX1075 to the ADSP21_ _ _. There are two modes of operation that can be programmed to interface with the MAX1072/MAX1075. For continuous conversions, idle CNVST low and pulse it high for one clock cycle during the LSB of the previous transmitted word. The ADSP21_ _ _ STCTL and SRCTL registers should be configured for early framing (LAFR = 0) and for an active-high frame (LTFS = 0, LRFS = 0) signal. In this mode, the data-independent frame-sync bit (DITFS = 1) can be selected to eliminate the need for writing to the transmit-data register more than once. For single conversions, idle CNVST high and pulse it low for the entire conversion. The ADSP21_ _ _ STCTL and SRCTL regis-

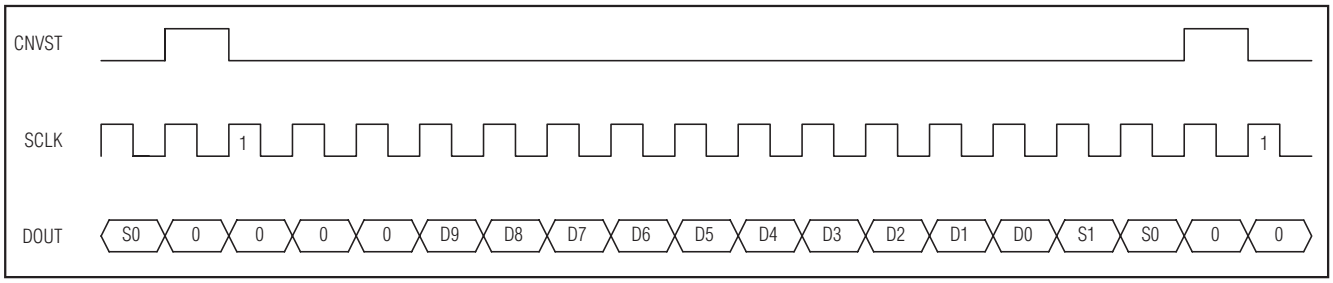

Figure 17. DSP Interface—Continuous Conversion

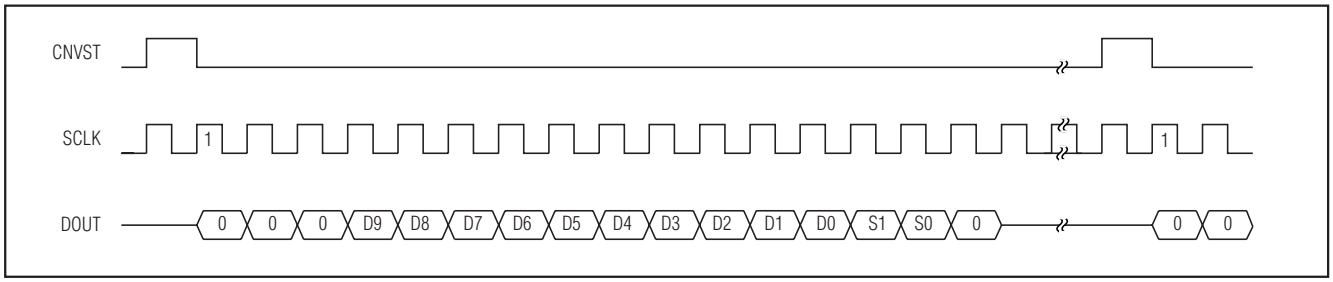

Figure 18. DSP Interface—Single-Conversion, Continuous/Burst Clock

ters should be configured for late framing (LAFR = 1) and for an active-low frame (LTFS = 1, LRFS = 1) signal. This is also the best way to enter the power-down modes by setting the word length to 8 bits (SLEN = 1001). Connect the V_L pin to the ADSP21_ _ _ supply voltage when the MAX1072/MAX1075 are operating with a supply voltage higher than the DSP supply voltage (see Figures 17 and 18).

Layout, Grounding, and Bypassing

For best performance, use PC boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 20 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at GND, separate from the logic ground. Connect all other analog grounds and DGND to this star ground point for further noise reduction. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply can affect the ADC's high-speed comparator. Bypass this supply to the single-point analog ground with 0.01µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1072/MAX1075 are measured using the end-points method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of 1 LSB or less guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of CNVST and the instant when an actual sample is taken.

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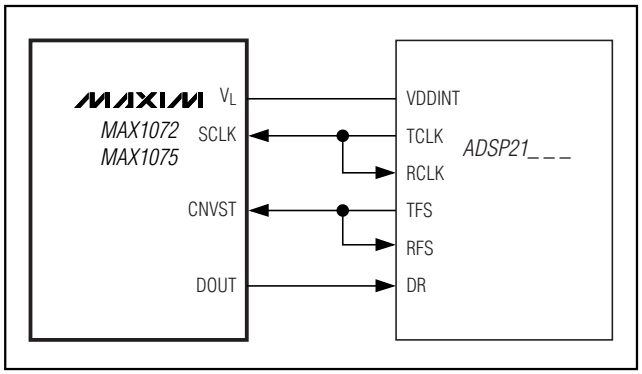


Figure 19. Interfacing to the ADSP21_ _ _

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals:

$$SINAD(dB) = 20 \times \log (Signal_{RMS} / Noise_{RMS})$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

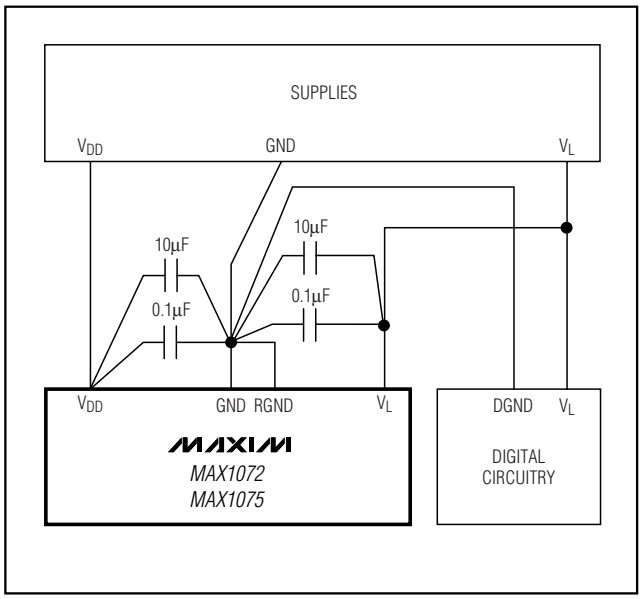


Figure 20. Power-Supply Grounding Condition

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest distortion component.

Full-Power Bandwidth

Full-power bandwidth is the frequency at which the input signal amplitude attenuates by 3dB for a full-scale input.

Full-Linear Bandwidth

Full-linear bandwidth is the frequency at which the signal to noise plus distortion (SINAD) is equal to 56dB.

Intermodulation Distortion

Any device with nonlinearities creates distortion products when two sine waves at two different frequencies (f1 and f2) are input into the device. Intermodulation distortion (IMD) is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones, f1 and f2. The individual input tone levels are at -7dBFS.

The intermodulation products are as follows:

- 2nd-order intermodulation products (IM2): $f_1 + f_2$, $f_2 - f_1$
- 3rd-order intermodulation products (IM3): $2f_1 - f_2$, $2f_2 - f_1$, $2f_1 + f_2$, $2f_2 + f_1$
- 4th-order intermodulation products (IM4): $3f_1 - f_2$, $3f_2 - f_1$, $3f_1 + f_2$, $3f_2 + f_1$
- 5th-order intermodulation products (IM5): $3f_1 - 2f_2$, $3f_2 - 2f_1$, $3f_1 + 2f_2$, $3f_2 + 2f_1$

Chip Information

TRANSISTOR COUNT: 13,016

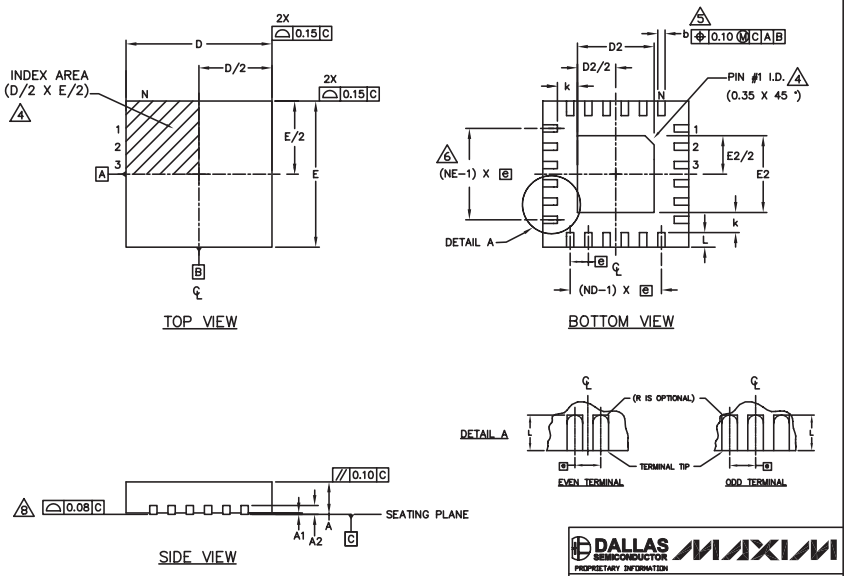
PROCESS: BiCMOS

1.8Msps, Single-Supply, Low-Power, True-Differential, 10-Bit ADCs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. B | 1/2

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. B | 2/2