MAC15M, MAC15N

Preferred Device

Triacs

Silicon Bidirectional Thyristors

Designed for high performance full-wave ac control applications where high noise immunity and high commutating di/dt are required.

- Blocking Voltage to 800 Volts
- On-State Current Rating of 15 Amperes RMS at 80°C
- Uniform Gate Trigger Currents in Three Modes
- High Immunity to dv/dt — 250 V/μs minimum at 125°C
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220AB Package
- High Commutating di/dt — 9.0 A/ms minimum at 125°C
- Operational in Three Quadrants, Q1, Q2, and Q3
- Device Marking: Logo, Device Type, e.g., MAC15M, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

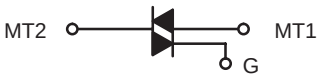
Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage(1) (–40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) MAC15M MAC15N	V_{DRM}, V_{RRM}	600 800	Volts
On–State RMS Current (Full Cycle Sine Wave, 60 Hz, T_C = 80°C)	$I_{T(RMS)}$	15	A
Peak Non-repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	150	A
Circuit Fusing Consideration (t = 8.3 ms)	I^2t	93	A^2s
Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 80°C)	P_{GM}	20	Watts
Average Gate Power (t = 8.3 ms, T_C = 80°C)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

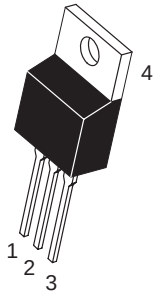
(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

ON Semiconductor

http://onsemi.com

TRIACS
15 AMPERES RMS
600 thru 800 VOLTS





TO–220AB
CASE 221A
STYLE 4

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
MAC15M	TO220AB	50 Units/Rail
MAC15N	TO220AB	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
$R_{\theta JC}$ $R_{\theta JA}$	Thermal Resistance — Junction to Case — Junction to Ambient	2.0 62.5	°C/W
T_L	Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	260	°C

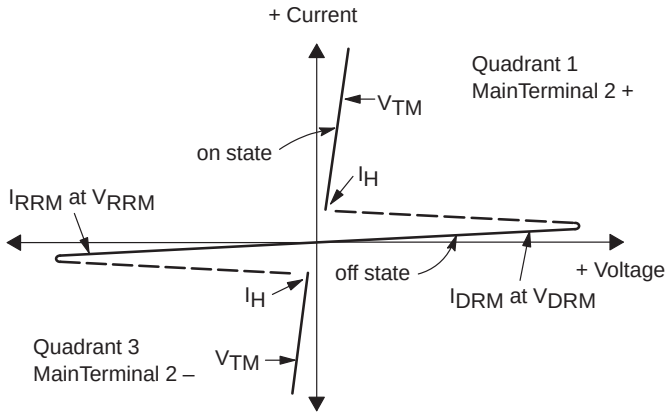
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Symbol	Characteristic		Min	Typ	Max	Unit
OFF CHARACTERISTICS						
I_{DRM}, I_{RRM}	Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open)	T_J = 25°C T_J = 125°C	— —	— —	0.01 2.0	mA
ON CHARACTERISTICS						
V_{TM}	Peak On-State Voltage(1) (I_{TM} = ±21 A Peak)		—	1.2	1.6	Volts
I_{GT}	Gate Trigger Current (Continuous DC) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)		 5.0 5.0 5.0	 13 16 18	 35 35 35	mA
I_H	Hold Current (V_D = 12 Vdc, Gate Open, Initiating Current = ±150 mA)		—	20	40	mA
I_L	Latching Current (V_D = 24 V, I_G = 35 mA) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)		 — — —	 33 36 33	 50 80 50	mA
V_{GT}	Gate Trigger Voltage (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)		 0.5 0.5 0.5	 0.75 0.72 0.82	 1.5 1.5 1.5	Volts
DYNAMIC CHARACTERISTICS						
$(di/dt)_c$	Rate of Change of Commutating Current; See Figure 10. (V_D = 400 V, I_{TM} = 6.0 A, Commutating dv/dt = 24 V/μs, Gate Open, T_J = 125°C, f = 250 Hz, No Snubber)	C_L = 10 μF L_L = 40 mH	9.0	—	—	A/ms
dv/dt	Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)		250	—	—	V/μs

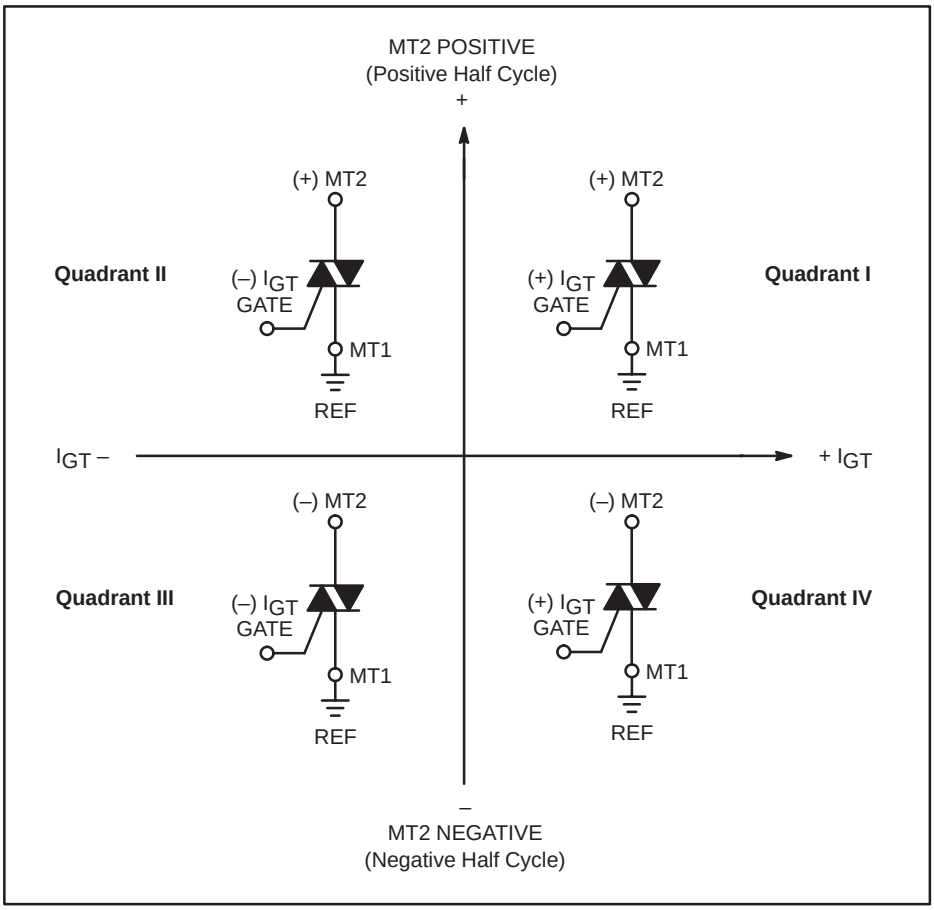
(1) Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in–phase signals (using standard AC lines) quadrants I and III are used.

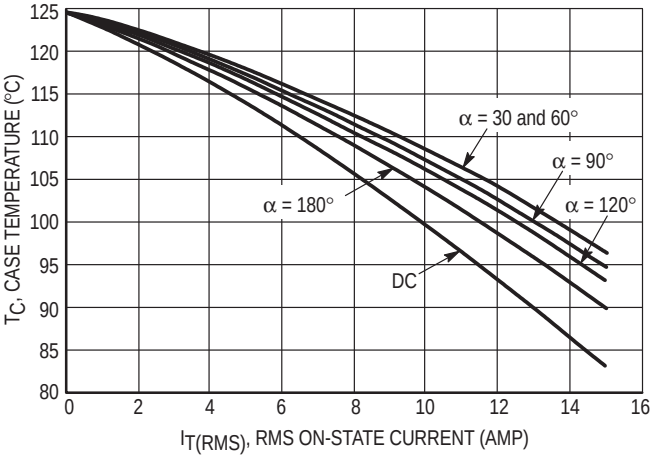


Figure 1. RMS Current Derating

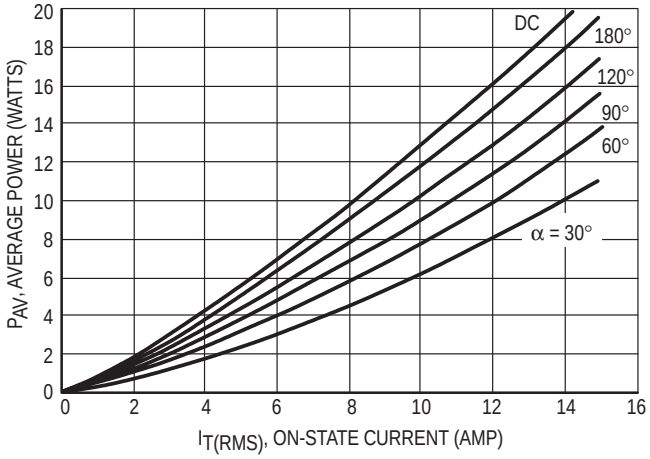


Figure 2. On–State Power Dissipation

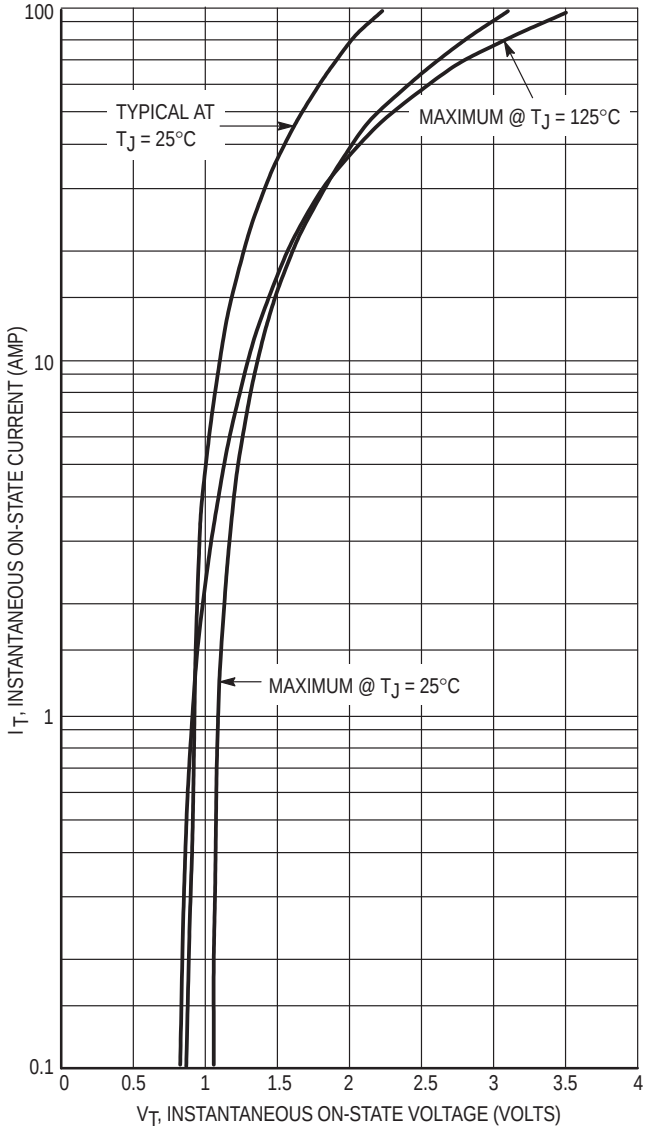


Figure 3. On–State Characteristics

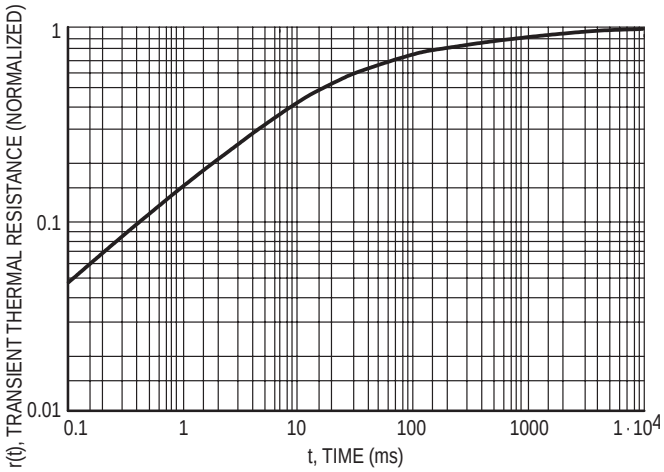


Figure 4. Transient Thermal Response

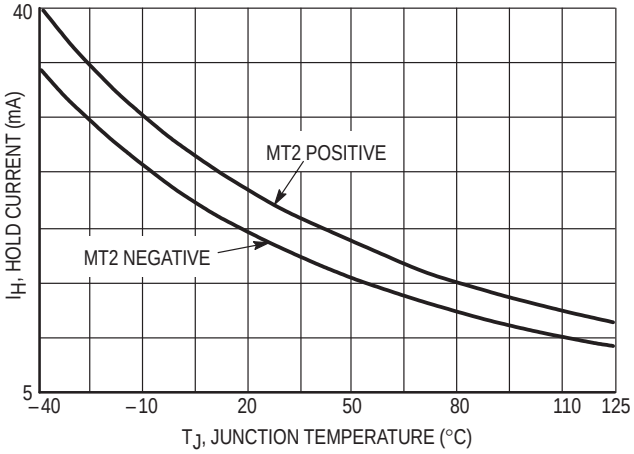


Figure 5. Hold Current Variation

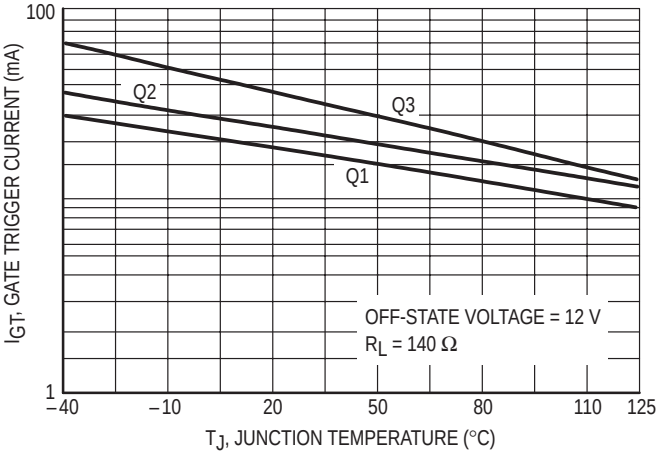


Figure 6. Typical Holding Current versus Junction Temperature

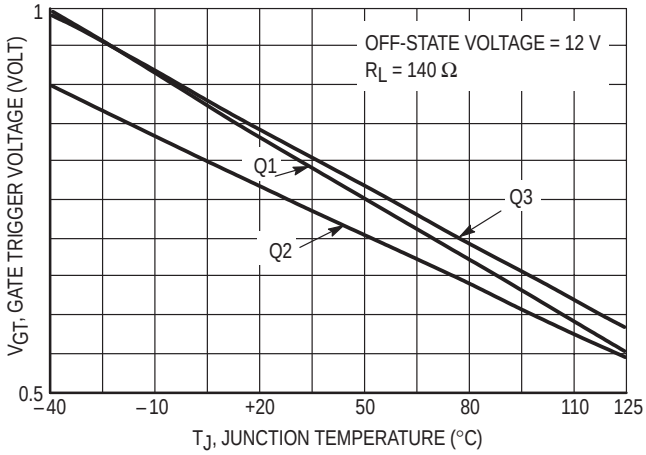


Figure 7. Gate Trigger Voltage versus Junction Temperature

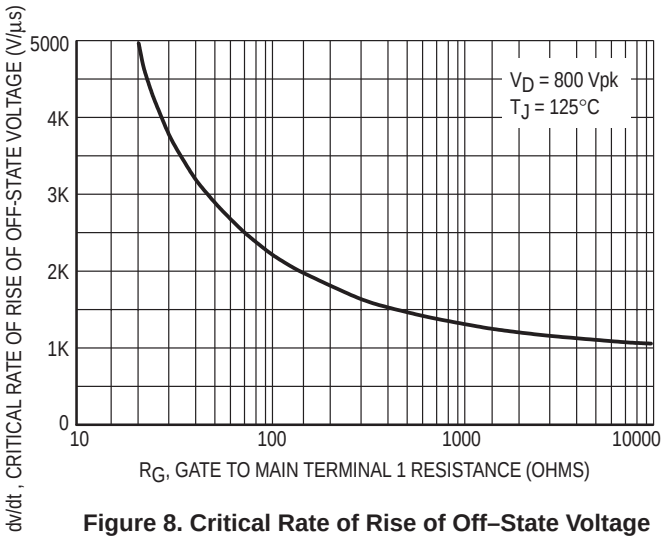


Figure 8. Critical Rate of Rise of Off–State Voltage (Exponential)

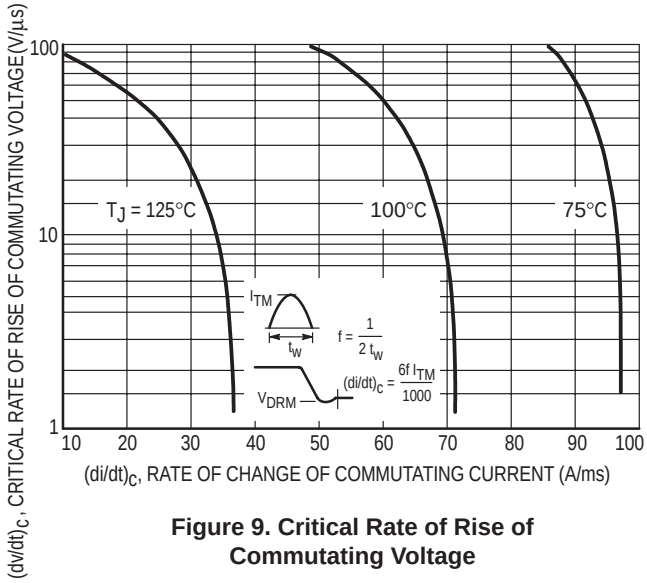
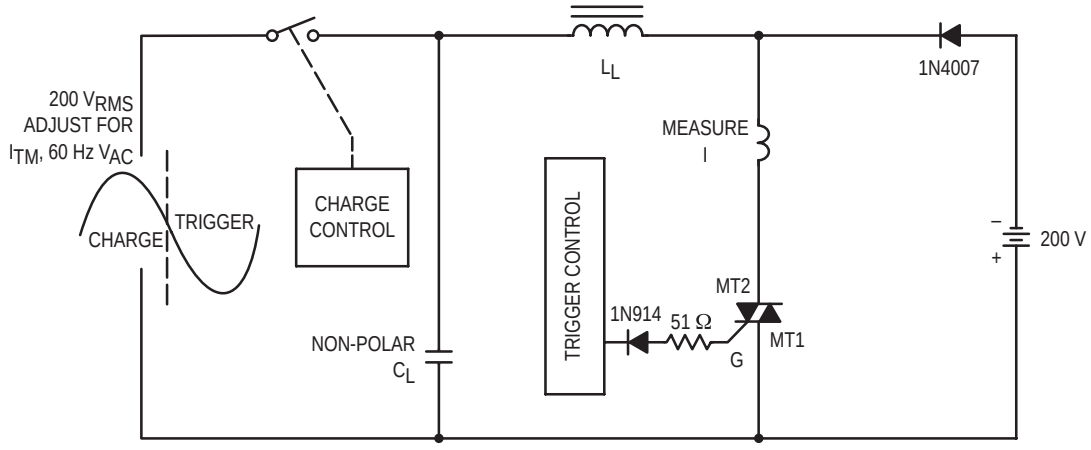


Figure 9. Critical Rate of Rise of Commutating Voltage

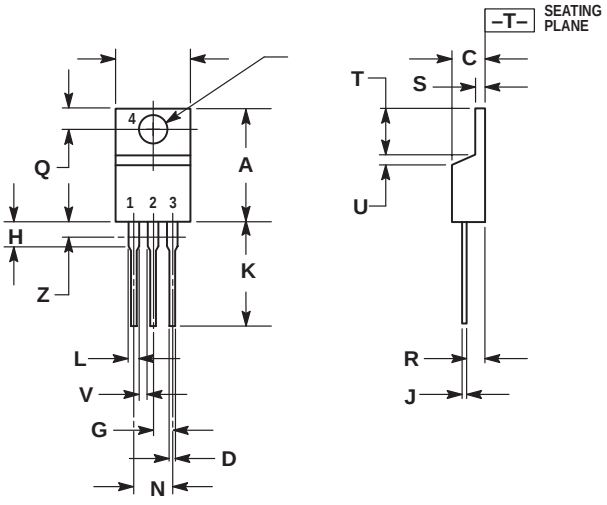


Note: Component values are for verification of rated $(di/dt)_C$. See AN1048 for additional information.

Figure 10. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_C$

PACKAGE DIMENSIONS

TO–220AB
CASE 221A–09
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

Notes

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