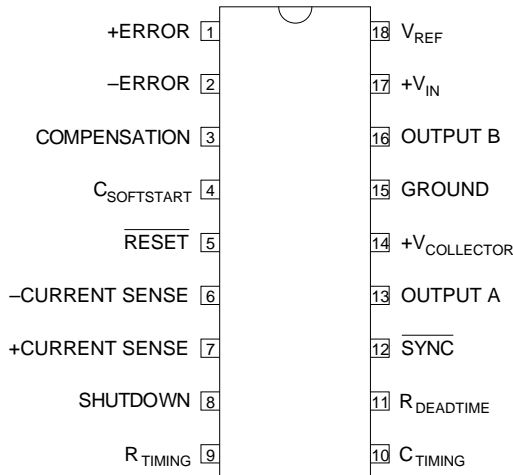


TOP VIEW



J Package – 18 Pin Ceramic DIP  
 N Package – 18 Pin Plastic DIP  
 DW Package – 18 Pin Plastic (300) SOIC

Order Information

Part Number	J-Pack 18 Pin	N-Pack 18 Pin	D-18 18 Pin	Temp. Range
IP1526	✓			-55 to +125°C
IP3526	✓	✓	✓	0 to +70°C

Note:

To order, add the package identifier to the part number.  
 eg. IP1526J  
 IP3526DW-18

## REGULATING PULSE WIDTH MODULATOR

### FEATURES

- 8 to 35V operation
- 5V reference trimmed to ±1%
- 1Hz to 400kHz oscillator range
- Dual 100mA source/sink outputs
- Digital current limiting
- Double pulse suppression
- Programmable deadtime
- Undervoltage lockout
- Single Pulse metering
- Programmable soft start
- Wide current limit common mode range
- TTL/CMOS compatible logic ports
- Symmetry correction capability
- Guaranteed 6 unit synchronisation

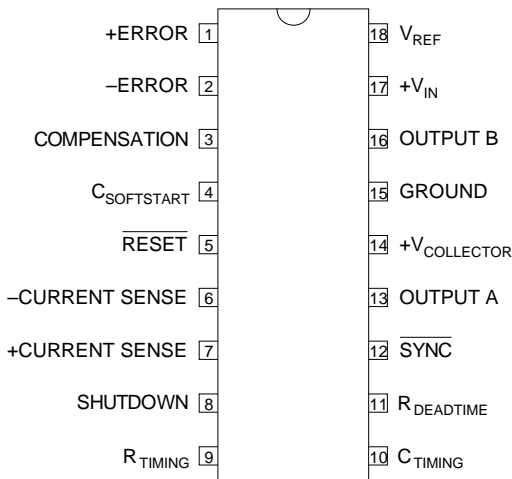
### ABSOLUTE MAXIMUM RATINGS (T<sub>case</sub> = 25°C unless otherwise stated)

+V <sub>IN</sub>	Input Voltage		+40V
	Collector Supply Voltage		+40V
	Logic Inputs		-0.3 to +5.5V
	Analogue Inputs		-0.3 to +V <sub>IN</sub>
	Source / Sink Load Current		200mA
	Reference Load Current		Internally Limited
	Logic Sink Current		15mA
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25°C	1W
		Derate @ T <sub>A</sub> > 50°C	10mW/°C
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	3W
		Derate @ T <sub>C</sub> > 25°C	24mW/°C
T <sub>J</sub>	Operating Junction Temperature		See Ordering Information
T <sub>STG</sub>	Storage Temperature Range		-65 to +150°C
T <sub>L</sub>	Lead Temperature	(soldering, 10 seconds)	+300°C

**DESCRIPTION**

The IP1526 and IP3526 high performance monolithic pulse width modulator circuits are designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled.

**BLOCK DIAGRAM**



**RECOMMENDED OPERATING CONDITIONS**

$V_{IN}$	Input Voltage	+8 to +35V
	Collector Voltage	+4.5 to +35V
	Sink/Source Load Current (Each Output)	0 to 100mA
	Reference Load Current	0 to 20mA
	Oscillator Frequency Range	1Hz to 400kHz
$R_T$	Oscillator Timing Resistor	2k $\Omega$ to 150k $\Omega$
$C_T$	Oscillator Timing Capacitor	470pF to 20 $\mu$ F
	Available Deadtime Range @ 40kHz	3% to 50%
	Operating Ambient Temperature Range	IP1526: -55 to +125 $^{\circ}$ C IP3526: 0 to +70 $^{\circ}$ C

**ELECTRICAL CHARACTERISTICS** ( $T_J$  = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1526			IP3526			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>REFERENCE SECTION</b>								
Output Voltage	$T_J = 25^\circ\text{C}$	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	$V_{IN} = 8$ to 35V		2	20		2	30	mV
Load Regulation	$I_L = 0$ to 20mA		5	30		5	50	
Temperature Stability			15	50		15	50	mV
Total Output Voltage Range		4.9	5.0	5.1	4.85	5.0	5.15	V
Short Circuit Current	$V_{REF} = 0$	25	80	140	25	80	140	mA
<b>UNDERVOLTAGE LOCKOUT</b>								
$\overline{\text{RESET}}$ Output Voltage	$V_{REF} = 3.8\text{V}$		0.2	0.4		0.2	0.4	V
	$V_{REF} = 4.8\text{V}$	2.4	4.8		2.4	4.8		
<b>OSCILLATOR SECTION <sup>2</sup></b>								
Initial Accuracy	$T_J = 25^\circ\text{C}$		$\pm 3$	$\pm 8$		$\pm 3$	$\pm 8$	%
Voltage Stability	$V_{IN} = 8$ to 35V		0.5	1		0.5	1	
Temperature Stability			3	10		7	10	
Minimum Frequency	$R_T = 150\text{k}\Omega$ $C_T = 0.2\mu\text{F}$			100			100	Hz
Maximum Frequency	$R_T = 2\text{k}\Omega$ $C_T = 470\text{pF}$	400			400			kHz
Sawtooth Peak Voltage	$V_{IN} = 35\text{V}$		3	3.5		3	3.5	V
Sawtooth Valley Voltage	$V_{IN} = 8\text{V}$ $T_J = 25^\circ\text{C}$	0.5	1			1		
<b>ERROR AMPLIFIER SECTION <sup>3</sup></b>								
Input Offset Voltage	$R_S \leq 2\text{k}\Omega$		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	
DC Open Loop Gain	$R_L \geq 10\text{M}\Omega$	64	72		60	72		dB
High Output Voltage	$V_{PIN1} - V_{PIN2} \geq 150\text{mV}$ $I_{SOURCE} = 100\mu\text{A}$	3.6	4.2		3.6	4.2		V
Low Output Voltage	$V_{PIN1} - V_{PIN2} \geq 150\text{mV}$ $I_{SINK} = 100\mu\text{A}$		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$R_S \leq 2\text{k}\Omega$	70	94		70	94		dB
Supply Voltage Rejection	$V_{IN} = 12\text{V}$ to 18V	66	80		66	80		

**NOTES**

1. Test Conditions unless otherwise stated:

$$V_{IN} = 15\text{V}$$

$$T_J = -55 \text{ to } +125^\circ\text{C} \quad \text{for IP1526}$$

$$T_J = 0 \text{ to } +70^\circ\text{C} \quad \text{for IP3526}$$

2. Oscillator / PWM Section Test Conditions:

$$f_{OSC} = 40\text{kHz}$$

$$(R_T = 4.12\text{k}\Omega, C_T = 0.01\mu\text{F} \pm 1\%, R_D = 0)$$

3. Error Amplifier Section Test Condition:

$$V_{CM} = 0 \text{ to } 5.2\text{V}$$

**ELECTRICAL CHARACTERISTICS** ( $T_J$  = Over Operating Temperature Range unless otherwise stated)

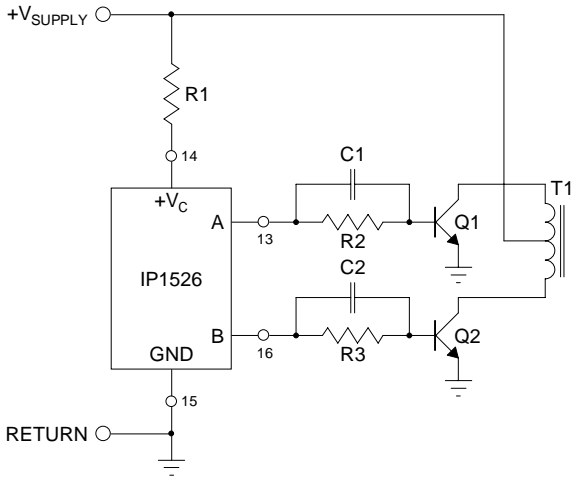
Parameter	Test Conditions	IP1526			IP3526			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>PWM COMPARATOR <sup>2</sup></b>								
Minimum Duty Cycle	$V_{PIN2} - V_{PIN1} \geq 150\text{mV}$			0			0	%
Maximum Duty Cycle	$V_{PIN1} - V_{PIN2} \geq 150\text{mV}$	45	49		45	49		
<b>DIGITAL PORTS (SYNC, SHUTDOWN &amp; RESET)</b>								
HIGH Output Voltage	$I_{SOURCE} = 40\mu\text{A}$	2.4	4.0		2.4	4.0		V
LOW Output Voltage	$I_{SINK} = 3.6\text{mA}$		0.2	0.4		0.2	0.4	
HIGH Input Current	$V_{IH} = 2.4\text{V}$		-125	-200		-125	-300	$\mu\text{A}$
LOW Input Current	$V_{IL} = 0.4\text{V}$		-225	-360		-225	-500	
<b>CURRENT LIMIT COMPARATOR <sup>4</sup></b>								
Sense Voltage	$R_S \leq 50\Omega$	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	$\mu\text{A}$
<b>SOFT-START SECTION</b>								
Error Clamp Voltage	$\overline{\text{RESET}} = 0.4\text{V}$		0.1	0.4		0.1	0.4	V
$C_S$ Charging Current	$\overline{\text{RESET}} = 2.4\text{V}$	50	100	150	50	100	150	$\mu\text{A}$
<b>OUTPUT DRIVERS (each output) <sup>5</sup></b>								
HIGH Output Voltage	$I_{SOURCE} = 20\text{mA}$	12.5	13.5		12.5	13.5		V
	$I_{SOURCE} = 100\text{mA}$	12	13		12	13		
LOW Output Voltage	$I_{SINK} = 20\text{mA}$		0.2	0.3		0.2	0.3	V
	$I_{SINK} = 100\text{mA}$		1.2	2.0		1.2	2.0	
Collector Leakage	$V_C = 40\text{V}$		50	150		50	150	$\mu\text{A}$
Rise Time	$C_L = 1000\text{pF}$		0.3	0.6		0.3	0.6	$\mu\text{s}$
Fall Time	$C_L = 1000\text{pF}$		0.1	0.2		0.1	0.2	
<b>POWER CONSUMPTION</b>								
Standby Current	$V_{IN} = 35\text{V}$ $R_T = 4.12\text{k}\Omega$ $\text{SHUTDOWN} = 0.4\text{V}$		18	30		18	30	mA

**NOTES**

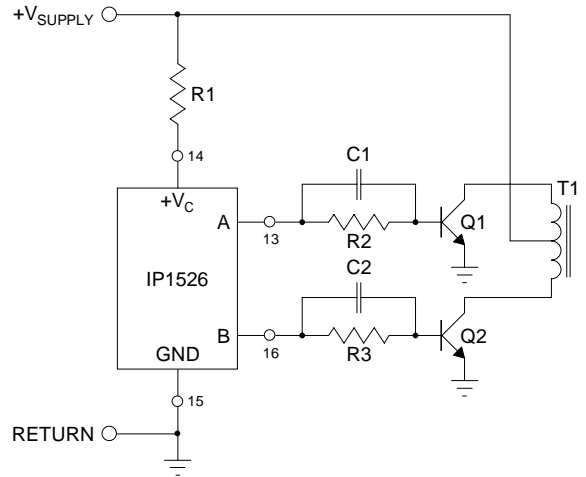
- Test Conditions unless otherwise stated:  
 $V_{IN} = 15\text{V}$   
 $T_J = -55$  to  $+125^\circ\text{C}$  for IP1526  
 $T_J = 0$  to  $+70^\circ\text{C}$  for IP3526
- Oscillator / PWM Section Test Conditions:  
 $f_{OSC} = 40\text{kHz}$   
 $(R_T = 4.12\text{k}\Omega, C_T = 0.01\mu\text{F} \pm 1\%, R_D = 0)$
- Error Amplifier Section Test Conditions:  
 $V_{CM} = 0$  to  $5.2\text{V}$
- Current Limit Comparator Section Test Conditions:  
 $V_{CM} = 0$  to  $12\text{V}$
- Output Driver Section Test Conditions:  
 $V_C = 15\text{V}$

APPLICATIONS INFORMATION

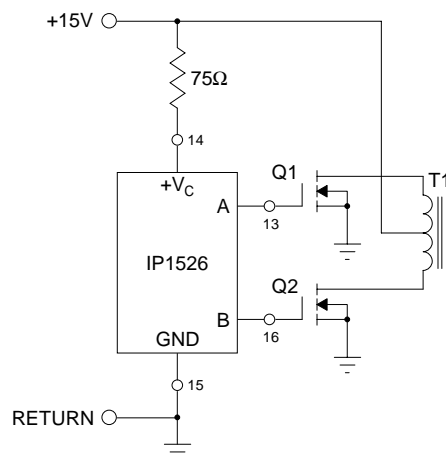
Push-Pull Configuration



Single-Ended Configuration

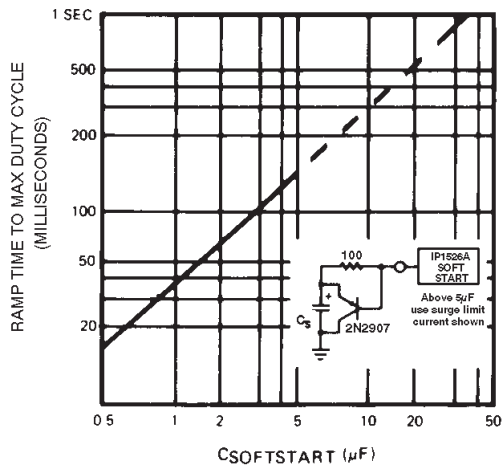


Driving N-Channel Power MOSFETs

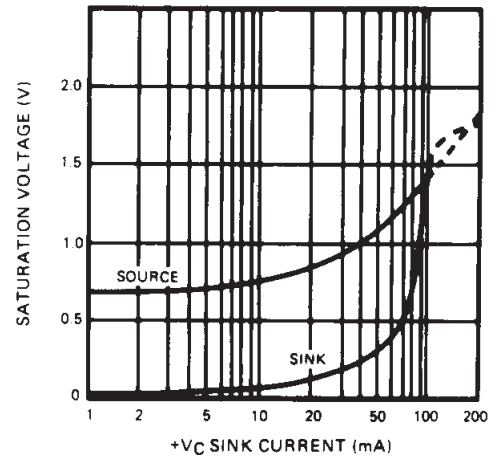


TYPICAL PERFORMANCE CHARACTERISTICS

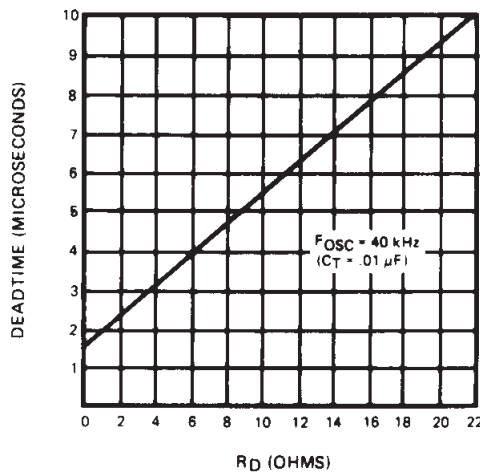
Soft Start Time vs  $C_S$



Output Driver Saturation Voltage



Output Driver Deadtime vs  $R_D$  Value



Oscillator Period vs  $R_T$  and  $C_T$

