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Power Control IC Single Chip PowerSupply

The HIP5060 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC. Both the standard "Boost" and the "SEPIC" (Single-Ended Primary Inductance Converter) power supply topologies are easily implemented with this single control IC.

Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Moreover, over-temperature and over-voltage detection circuitry is incorporated within the IC to monitor the chip temperature and the actual power supply output voltage. These circuits can disable the drive to the power transistor to protect both the transistor and, most importantly, the load from over-voltage.

As a result of the power DMOS transistor's current and voltage capability (10A and 60V), power supplies with output power capability up to 100 watts are possible.

Features

- Single Chip Current Mode Control IC
- 60V, 10A On-Chip DMOS Transistor
- Thermal Protection
- Over-Voltage Protection
- Over-Current Protection
- 1MHz Operation or External Clock
- Synchronization Output
- On-Chip Reference Voltage - 5.1V
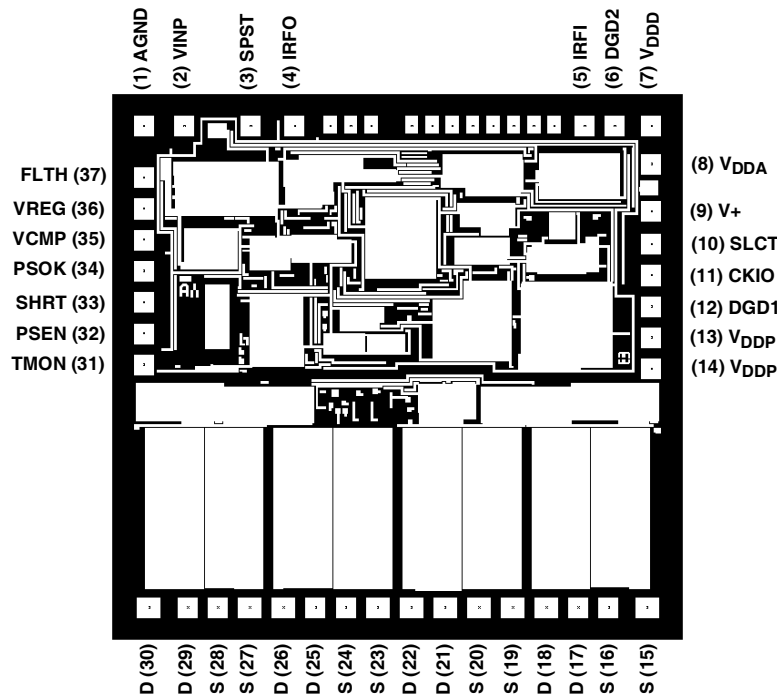- Output Rise and Fall Times ~ 3ns
- Designed for 27V to 45V Operation

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5060DY	0^oC to $+85^oC$	37 Pad Chip
HIP5060DW	0^oC to $+85^oC$	Wafer

Chip

NOTE: Unused pads are for trim and test.
153 mils x 165 mils (3.88mm x 4.19mm)

Simplified Block Diagram
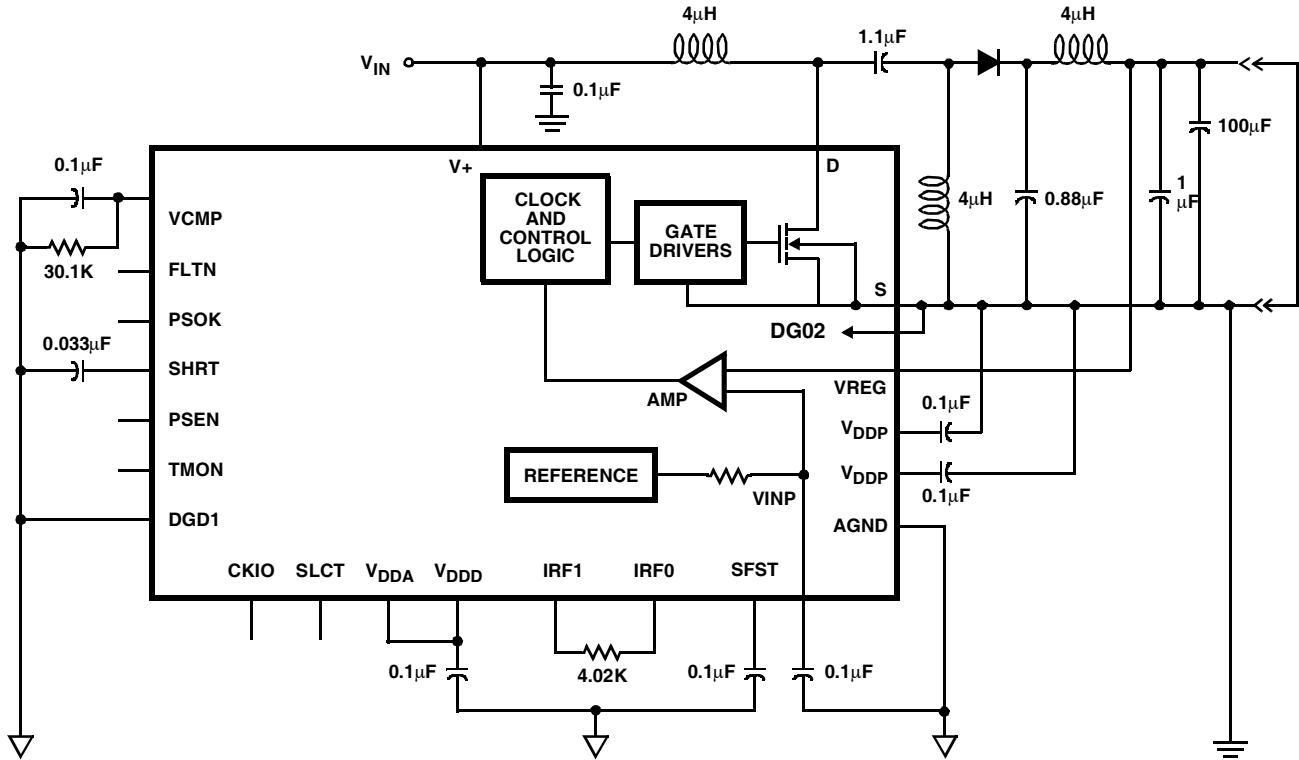
TYPICAL SEPIC CONFIGURATION

HIP5060

Absolute Maximum Ratings

DC Supply Voltage, V+. . . . . -0.3V to 45V
DMOS Drain Voltage . . . . -0.3V to 60V
DMOS Drain Current 20A
DC Logic Supply. . . . . -0.3V to 16V
Output Voltage, Logic Outputs . . . . -0.3V to 16V
Input Voltage, Analog and Logic. . . . . -0.3V to 16V
Operating Junction Temperature Range . . . . .0°C to +110°C
Storage Temperature Range . . . . -55°C to +150°C

Thermal Information

Thermal Resistance θ_{JC}
  (Solder Mounted to . . . . 3°C/W Max
  0.050" Thick Copper Heat Sink)
Maximum Junction Temperature. . . . .+110°C
  (Controlled By Thermal Shutdown Circuit)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V+ = 36V$, $T_J = 0^oC$ to $+110^oC$; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I+	Supply Current	PSEN = 12V	-	19.5	32	mA
V_{DDA}	Internal Regulator Output Voltage	V+ = 15V to 45V, I_{OUT} = 10mA	11.0	-	13.2	V
VINP	Reference Voltage	I_{VINP} = 0mA	5.01	5.1	5.19	V
R_{VINP}	VINP Resistance	VINP = 0	-	900	-	Ω
ERROR AMPLIFIERS						
$|V_{IO}|$	Input Offset Voltage (VREG - VINP)	I_{VCMP} = 0mA	-	-	10	mV
R_{IN} VREG	Input Resistance to GND	VREG = 5.1V	-	56	-	kΩ
g_m (VREG)	VREG Transconductance $I_{VCMP}/(VREG - VINP)$	VCMP = 1V to 8V, SFST = 11V	15	30	50	mS
g_m (SFST)	SFST Transconductance $I_{VCMP}/(VREG - SFST)$	V_{SFST} < 4.9V	0.8	-	6	mS
I_{VCMP}	Maximum Source Current	VREG = 4.95V, VCMP = 8V	-2.5	-	-0.75	mA
I_{VCMP}	Maximum Sink Current	VREG = 5.25V, VCMP = 0.4V	0.75	-	2.5	mA
OVTH	Over-Voltage Threshold	Voltage at VREG for FLTN to be latched	6.2	-	6.7	V
CLOCK						
fq	Internal Clock Frequency	SLCT = 0V, V_{DDD} = 12V	0.9	1.0	1.1	MHz
V_{TH} CKIN	External Clock Input Threshold Voltages	SLCT = 12V	33	-	66	%V_{DDD}
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 5A, T_J = +25°C	-	-	0.13	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	μA
CURRENT CONTROLLED PWM						
$|V_{IO}|$ VCMP	Buffer Offset Voltage (VCMP - V_{IRFO})	IRFO = 0mA to -5mA, VCMP = 0.2V to 7.6V	-	-	125	mV
V_{TH} IRFO	Voltage at IRFO that disables PWM. This is due to low load current		100	-	270	mV

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Electrical Specifications V+ = 36V, T_J = 0°C to +110°C; Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT CONTROLLED PWM (Continued)						
I_{TH} IRFO	Voltage at IRFO to enable SHRT output current. This is due to Regulator Over Current Condition		7.4	-	8.0	V
I_{SHRT}	SHRT Output Current, During Over-Current	V_{IRFO} = 8.1V	-37	-	-17	μA
V_{TH} SHRT	Threshold voltage on SHRT to set FLTN latch		4	6	8	V
I_{GAIN}	I_{PEAK} (DMOS$_{DRAIN}$)/I_{IRFI}	ΔI (DMOS$_{DRAIN}$)/Δt = 1A/ms	3.8	-	4.9	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{IRFI} = 2mA	150	-	360	Ω
t_{RS} (Note 1)	Current Comparator Response Time	ΔI (DMOS$_{DRAIN}$)/Δt > 1A/μs	-	30	-	ns
MCPW (Note 1)	Minimum Controllable Pulse Width		25	50	100	ns
MCPI (Note 1)	Minimum Controllable DMOS Peak Current		200	400	800	mA
START-UP						
V+	Rising V+ Power-On Reset Voltage		22	-	27	V
V+	Falling V+ Power-Off Set Voltage		-	15	-	V
V+	V+ Power-On Hysteresis		9	-	12	V
V_{TH} PSEN	Voltage at PSEN to Enable Supply		0.8	-	2.0	V
r_{PSEN}	Internal Pull-Up Resistance, to 5.1V		-	20	-	KΩ
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 0V to 10V	-1.0	-0.7	-0.4	μA
I_{PSOK}	PSOK High-State Leakage Current	SFST = 0V, PSOK = 12V	-1	-	1	μA
V_{PSOK}	PSOK Low-State Voltage	SFST = 11V, I_{PSOK} = 1mA	-	-	0.4	V
V_{TH} SFST	PSOK Threshold, Rising V_{SFST}		9.4	-	11	V
THERMAL MONITOR						
TEMP (Note 1)	Substrate Temperature for Thermal Monitor to Trip	TMON pin open	105	-	135	°C

NOTE:

1. Determined by design, not a measured parameter.

Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1	AGND	Analog ground.
2	VINP	Internal 5.1V reference.
3	SFST	Controls the rate of rise of the output voltage. Time is determined by an internal 0.7μA current source and an external capacitor.
4	IRFO	A resistor placed between this pad and IRFI converts the VCMP signal to a current for the current sense comparator. The maximum current is set by the value of the resistor, according to the equation: $I_{PEAK} = 32/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 17.8A. This assumes VCMP is 7.3V. Maximum output current should be kept below 20A.
5	IRFI	See IRFO
6	DGD2	Ground of the DMOS gate driver. This pad is used for bypassing.
7	V_{DDD}	Voltage input for the chip's digital circuits. This pad also allows decoupling of this supply.
8	V_{DDA}	This is the analog supply and internal 12V regulator output.
9	V+	This is the main supply voltage input pad to the regulator IC. Because of the high peak currents this pad must be well bypassed with at least a 0.7μF capacitor and may be composed of seven, single 0.1μF chip capacitors.
10	SLCT	This pad provides for the option of using either internal 1MHz operation of for an external clock. Floating or grounding this pad will place the internal clock at the CKIO pad. Returning this terminal to V_{DDD} or 12V will allow application of an external clock to the IC via the CKIO pad. There is an internal 50K pull down
11	CKIO	Clock output when SLCT is floated or grounded. External clock input when SLCT is returned to 12V.
12	DGD1	This pad is the return for the digital supply.
13 & 14	V_{DDP}	These pads are used to decouple the high current pulses to the output driver transistors. The capacitor should be at least a 0.1μF chip capacitor placed close to this pad and the DMOS source pads.
15, 16, 19, 20, 23, 24, 27, 28	S	Source pads of the DMOS power transistor.
17, 18, 21, 22, 25, 26, 29, 30	D	Drain pads of the DMOS power transistor.
31	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to 12V the function is disabled. Returning this pad to ground will put the IC into the thermal shutdown state. Normally, this pad is left floating. Thermal shutdown occurs at a nominal junction temperature of +125°C.
32	PSEN	This terminal is provided to activate the converter. This terminal may be left open or returned to 5V for normal operation. When the input is low, the DMOS driver is disabled.
33	SHRT	25μA is internally applied to this node when there is an over-current condition.
34	PSOK	This pad provides a delayed positive indication when the supply is enabled.
35	VCMP	Output of the transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
36	VREG	Input to the transconductance error amplifier is available on this pad. The other input is internally connected to the 5.1V reference, VINP, Pad 2.
37	FLTN	This is an open drain output that remains low when V+ is too low for proper operation. This node and PSEN are useful in multiple converter configurations. This pad will be latched low when over-temperature, over-voltage or over-current is experienced.

Functional Block Diagram