NEC

MOS INTEGRATED CIRCUIT

μPD789304, 789306, 789314, 789316

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD789304, 789306, 789314, and 789316 belong to the μPD789306, 789316 Subseries (for LCD drivers) in the 78K/0S Series.

Flash memory versions (μPD78F9306, 78F9316) that can be operated using the same power supply voltage as mask ROM versions are available, along with various development tools.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789306, 789316 Subseries User's Manual: U14800E
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- ROM and RAM capacities

Item / Part Number	Program Memory (ROM)	Data Memory	
		Internal High-Speed RAM	LCD Display RAM
μPD789304, 789314	8 KB	512 bytes	24 bytes
μPD789306, 789316	16 KB		

- Main system clock
  Ceramic/crystal oscillation: μPD789304, 789306
  RC oscillation: μPD789314, 789316
- I/O ports: 23
- Serial interface: 2 channels
  Switchable between 3-wire serial I/O mode and UART mode: 1 channel
  3-wire serial I/O mode: 1 channel
- LCD controller/driver
  Segment signals: 24, common signals: 4
- Timer: 5 channels
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Remote control devices, healthcare equipment, etc.

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The mark ★ shows major revised points.

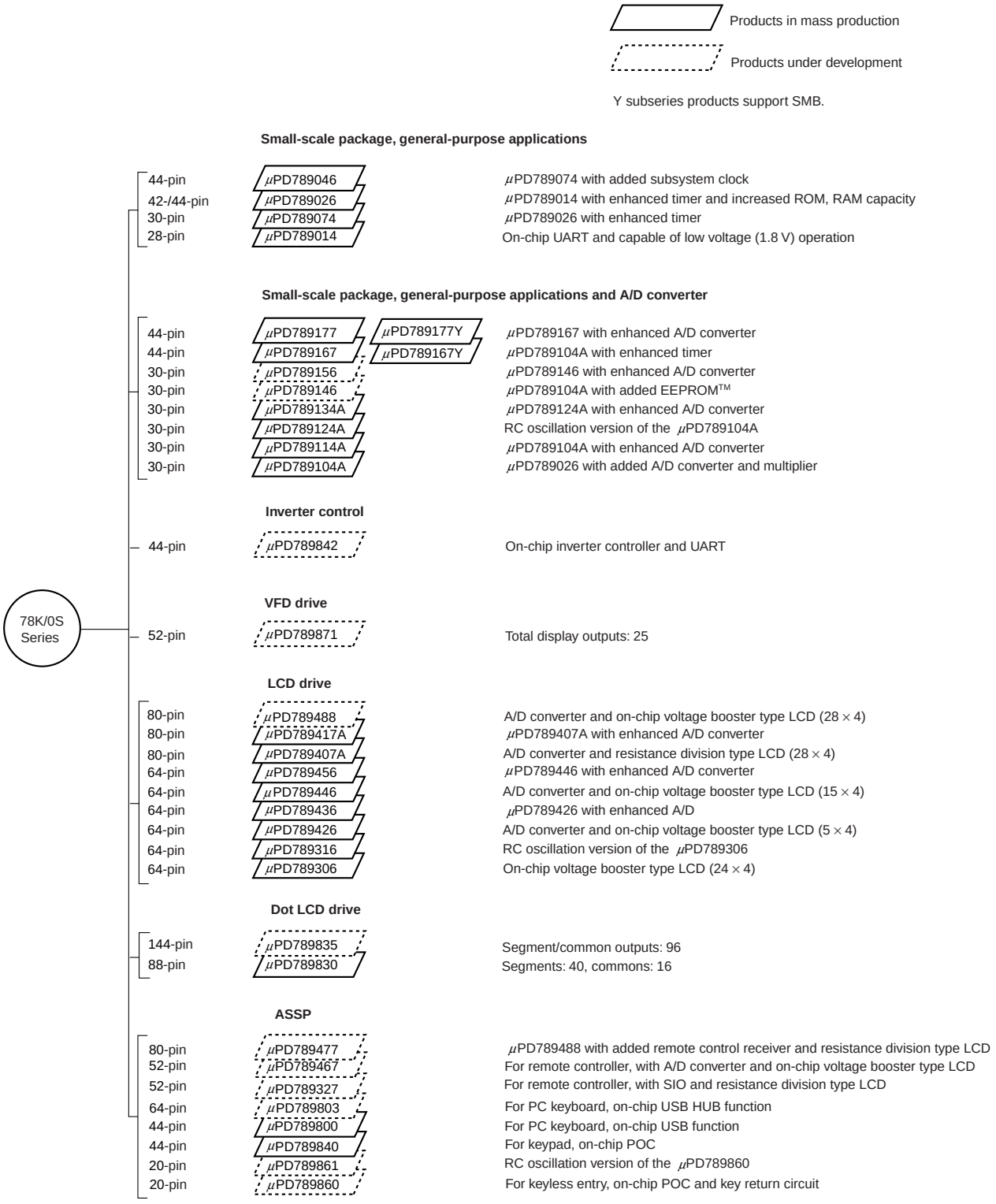
ORDERING INFORMATION

Part Number	Package
μPD789304GC-×××-AB8	64-pin plastic QFP (14 × 14)
μPD789304GK-×××-9ET	64-pin plastic TQFP (12 × 12)
μPD789306GC-×××-AB8	64-pin plastic QFP (14 × 14)
μPD789306GK-×××-9ET	64-pin plastic TQFP (12 × 12)
μPD789314GC-×××-AB8	64-pin plastic QFP (14 × 14)
μPD789314GK-×××-9ET	64-pin plastic TQFP (12 × 12)
μPD789316GC-×××-AB8	64-pin plastic QFP (14 × 14)
μPD789316GK-×××-9ET	64-pin plastic TQFP (12 × 12)

Remark ××× indicates ROM code suffix.

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	8-Bit	16-Bit	Watch	WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789074	2 K to 8 K								24		
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch		–	8 ch	1 ch (UART: 1 ch)	31		–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC-oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	μPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789417A	12 K to 24 K						7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC-oscillation version
	μPD789306											–
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	μPD789477	24 K	3 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch (UART: 1 ch)	45	1.8 V	On-chip LCD
	μPD789467	4 K to 24 K	2 ch	–			1 ch		–	18		
	μPD789327						–		1 ch	21		
	μPD789803	8 K to 16 K			–				2 ch (USB: 1 ch)	41	3.6 V	–
	μPD789800	8 K								31	4.0 V	
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					–		–	14	1.8 V	RC-oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		μPD789304	μPD789306	μPD789314	μPD789316
Internal memory	ROM	8 KB	16 KB	8 KB	16 KB
	High-speed RAM	512 bytes			
	LCD display RAM	24 bytes			
Main system clock (oscillation frequency)		Ceramic/crystal oscillation (1.0 to 5.0 MHz)		RC oscillation (2.0 to 4.0 MHz)	
Subsystem clock (oscillation frequency)		Crystal oscillation (32.768 kHz)			
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0 MHz operation with main system clock)		0.5 μs/2.0 μs (@ 4.0 MHz operation with main system clock)	
		122 μs (@ 32.768 kHz operation with subsystem clock)			
General-purpose registers		8 bits × 8 registers			
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test)			
I/O ports		Total: 23 • CMOS I/O: 19 • N-ch open drain: 4			
Timers		• 16-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel			
Serial interface		• Switchable between 3-wire serial I/O mode and UART mode: 1 channel • 3-wire serial I/O mode: 1 channel			
LCD controller/driver		• Segment signal outputs: 24 (Max.) • Common signal outputs: 4 (Max.)			
Vectored interrupt sources	Maskable	Internal: 9, External: 5			
	Non-maskable	Internal: 1			
Power supply voltage		V_{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85°C			
Package		• 64-pin plastic QFP (14 × 14) • 64-pin plastic TQFP (12 × 12)			

CONTENTS

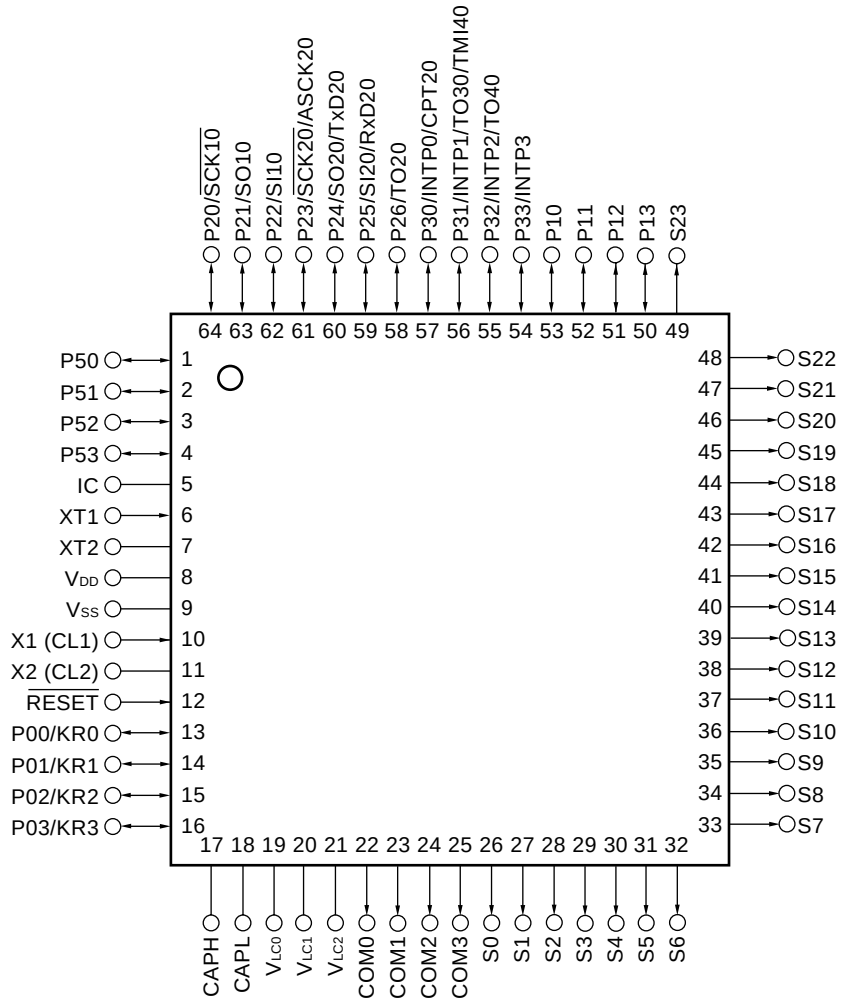
1. PIN CONFIGURATION (TOP VIEW)

64-pin plastic QFP (14 × 14)

μPD789304GC-×××-AB8
μPD789306GC-×××-AB8
μPD789314GC-×××-AB8
μPD789316GC-×××-AB8

64-pin plastic TQFP (12 × 12)

μPD789304GK-×××-9ET
μPD789306GK-×××-9ET
μPD789314GK-×××-9ET
μPD789316GK-×××-9ET

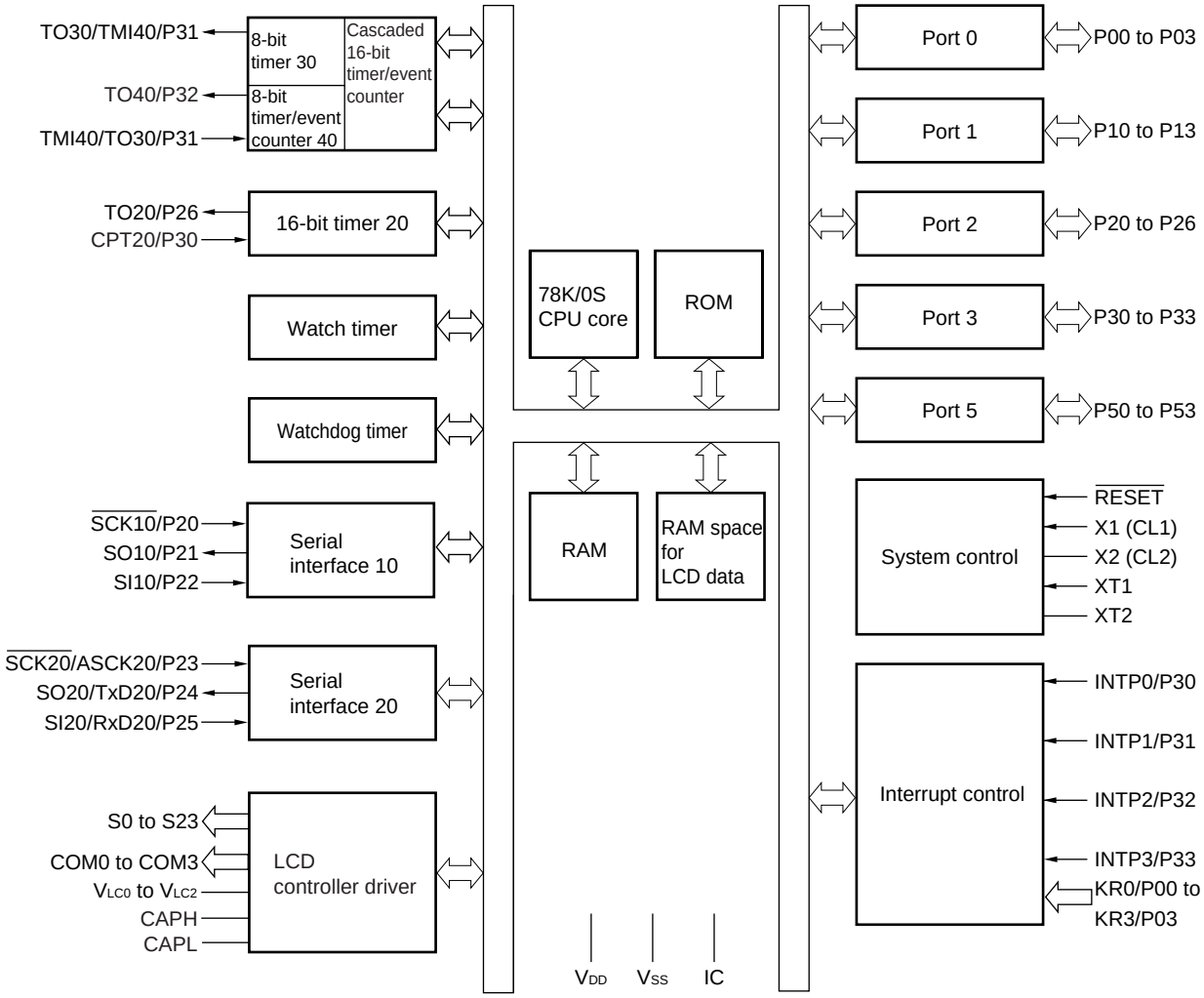


Caution Connect the IC (Internally Connected) pin directly to the V_{SS} pin.

Remark Pin names enclosed in parentheses are when using the μPD789314, 789316.

ASCK20:	Asynchronous serial input
CAPH, CAPL:	LCD power supply capacitance control
CL1, CL2:	RC oscillator
COM0 to COM3:	Common output
CPT20:	Capture trigger input
IC:	Internally connected
INTP0 to INTP3:	External interrupt input
KR0 to KR3:	Key return
P00 to P03:	Port 0
P10 to P13:	Port 1
P20 to P26:	Port 2
P30 to P33:	Port 3
P50 to P53:	Port 5
$\overline{\text{RESET}}$:	Reset
RxD20:	Receive data
S0 to S23:	Segment output
$\overline{\text{SCK10}}$, $\overline{\text{SCK20}}$:	Serial clock
SI10, SI20:	Serial input
SO10, SO20:	Serial output
TMI40:	Timer input
TO20, TO30, TO40:	Timer output
TxD20:	Transmit data
V_{DD}:	Power supply
V_{LC0} to V_{LC2}:	LCD power supply
V_{SS}:	Ground
X1, X2:	Crystal/ceramic oscillator
XT1, XT2:	Crystal oscillator

2. BLOCK DIAGRAM



Remark Pin names enclosed in parentheses are when using the μPD789314, 789316.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in port units by software.	Input	KR0 to KR3
P10 to P13	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in port units by software.	Input	–
P20	I/O	Port 2. 7-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units by software.	Input	$\overline{\text{SCK10}}$
P21				SO10
P22				SI10
P23				$\overline{\text{SCK20}}$/ASCK20
P24				SO20/TxD20
P25				SI20/RxD20
P26				TO20
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units by software.	Input	INTP0/CPT20
P31				INTP1/TO30/TMI40
P32				INTP2/TO40
P33				INTP3
P50 to P53	I/O	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified in bit units by the mask option.	Input	–

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/CPT20
INTP1				P31/TO30/TMI40
INTP2				P32/TO40
INTP3				P33
KR0 to KR3	Input	Key return signal detection	Input	P00 to P03
$\overline{SCK10}$	I/O	Serial clock input/output for serial interface (SIO10)	Input	P20
$\overline{SCK20}$		Serial clock input/output for serial interface (SIO20)		P23/ASCK20
SI10	Input	Serial data input for SIO10 serial interface	Input	P22
SI20		Serial data input for SIO20 serial interface		P25/RxD20
SO10	Output	Serial data output for SIO10 serial interface	Input	P21
SO20		Serial data output for SIO20 serial interface		P24/TxD20
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P23/$\overline{SCK20}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P25/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P24/SO20
TO20	Output	16-bit timer (TM20) output	Input	P26
CPT20	Input	Capture edge input	Input	P30/INTP0
TO30	Output	8-bit timer (TM30) output	Input	P31/INTP1/TMI40
TO40	Output	8-bit timer (TM40) output	Input	P32/INTP2
TMI40	Input	External count clock input to 8-bit timer (TM40)	Input	P31/INTP1/TO30
S0 to S23	Output	Segment signal output for LCD controller/driver	Output	–
COM0 to COM3	Output	Common signal output for LCD controller/driver	Output	–
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
CAPH	–	Connection pin for LCD driver's capacitor	–	–
CAPL	–		–	–
X1[Note 1]	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2[Note 1]	–		–	–
CL1[Note 2]	Input	Connections to resistor (R) and capacitor (C) for main system clock oscillation	–	–
CL2[Note 2]	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{RESET}$	Input	System reset input	Input	–
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
IC	–	Internally connected. Connect directly to V_{SS}.	–	–

Notes 1. μPD789304, 789306 only

2. μPD789314, 789316 only

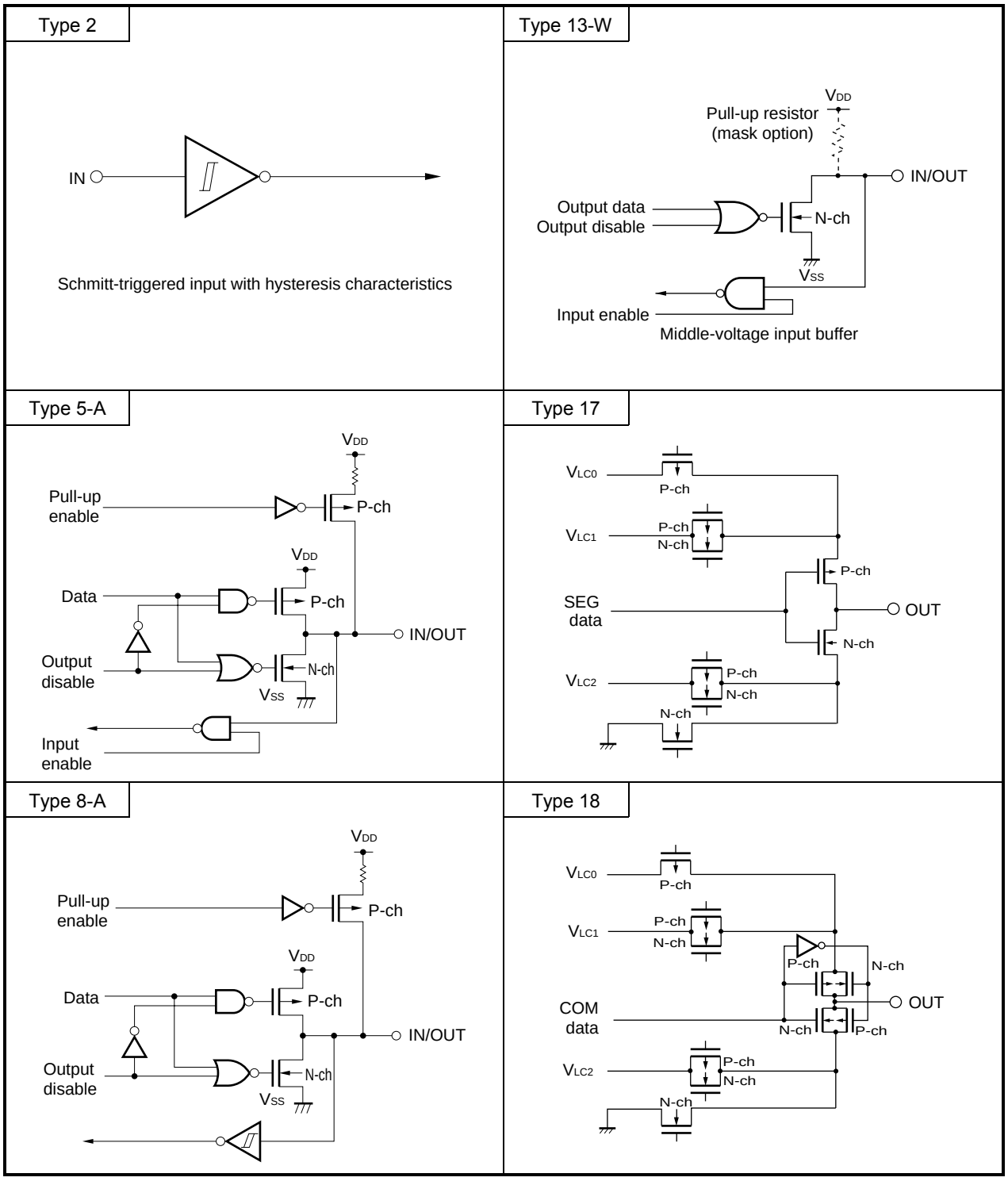
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.
For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/KR0 to P03/KR3	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P10 to P13	5-A		
P20/$\overline{SCK10}$	8-A		
P21/SO10			
P22/SI10			
P23/$\overline{SCK20}$/ASCK20			
P24/SO20/TxD20			
P25/SI20/RxD20			
P26/TO20			
P30/INTP0/CPT20			Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P31/INTP1/TO30/ TMI40			
P32/INTP2/TO40			
P33/INTP3			
P50 to P53	13-W		Input: Independently connect to V_{DD} via a resistor. Output: Leave open.
S0 to S23	17	Output	Leave open.
COM0 to COM3	18		
V_{LC0} to V_{LC2}	–	–	
CAPH, CAPL	–		
XT1	–	Input	Connect to V_{SS}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
IC	–	–	Directly connect to V_{SS}.

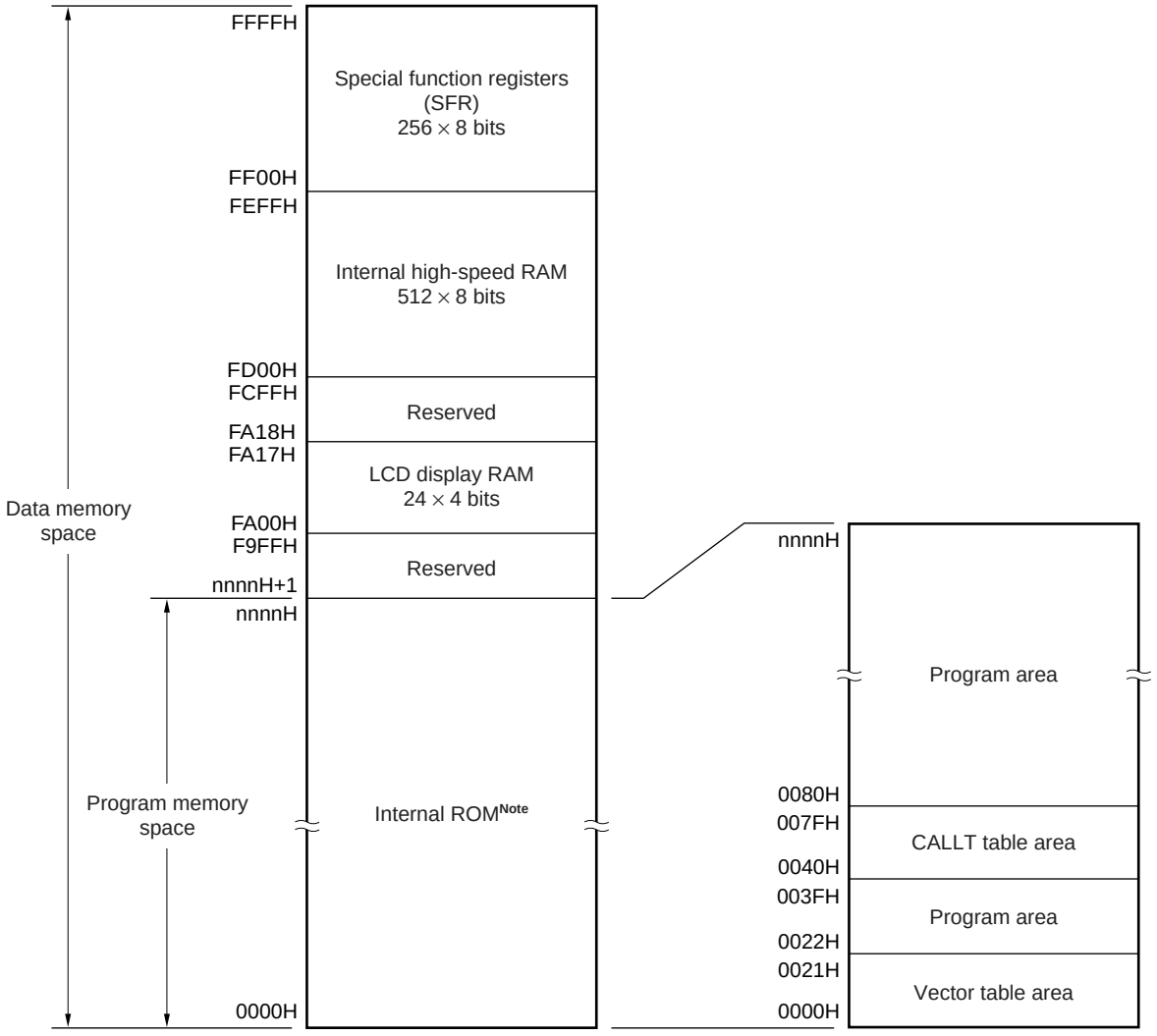
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD789304, 789306, 789314, and 789316.

Figure 4-1. Memory Map



Note The internal ROM capacity depends on the product (see the following table).

Part Number	Last Address of Internal ROM nnnnH
μPD789304, 789314	1FFFH
μPD789306, 789316	3FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The I/O ports are listed below.

- CMOS I/O: 19
- N-ch open-drain I/O: 4

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P03	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 1	P10 to P13	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 2	P20 to P26	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 3	P30 to P33	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 5	P50 to P53	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by the mask option.

5.2 Clock Generator

The specifications of the main system clock generator differ depending on the product as shown below.

(1) Main system clock generator

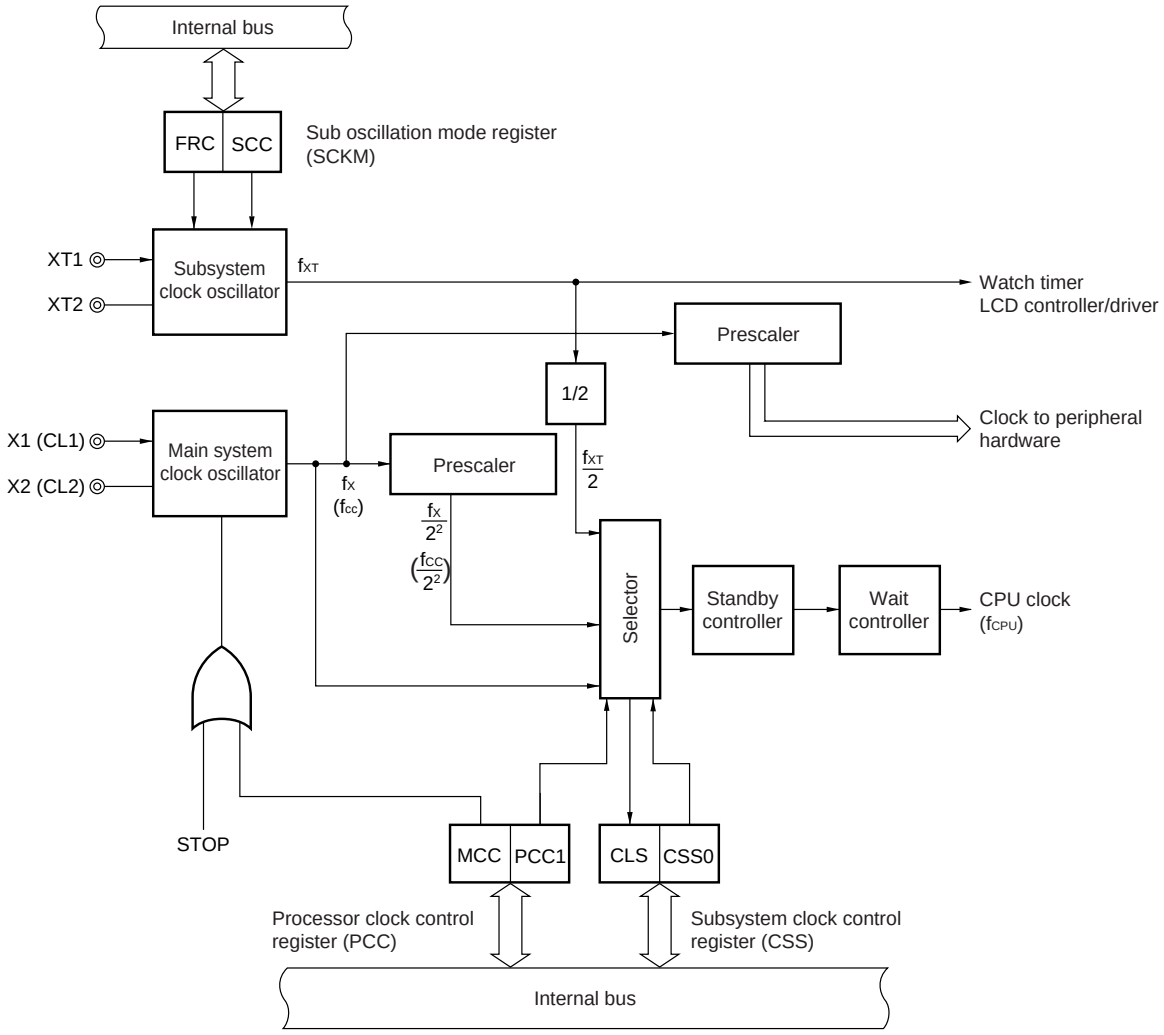
- Ceramic/crystal oscillation: μPD789304, 789306
  This generator's oscillation frequency range is 1.0 to 5.0 MHz. The minimum instruction execution time can be changed from 0.4 to 1.6 μs (@ 5.0 MHz operation).

- RC oscillation: μPD789314, 789316
  This generator's oscillation frequency range is 2.0 to 4.0 MHz. The minimum instruction execution time can be changed from 0.5 to 2.0 μs (@ 4.0 MHz operation).

(2) Subsystem clock generator (crystal oscillation)

This generator's oscillation frequency is 32.768 kHz. The minimum instruction execution time is 122 μs (@ 32.768 kHz operation).

Figure 5-1. Block Diagram of Clock Generator



Remark Pins names enclosed in parentheses are when using the RC oscillation (μPD789314, 789316).

5.3 Timer

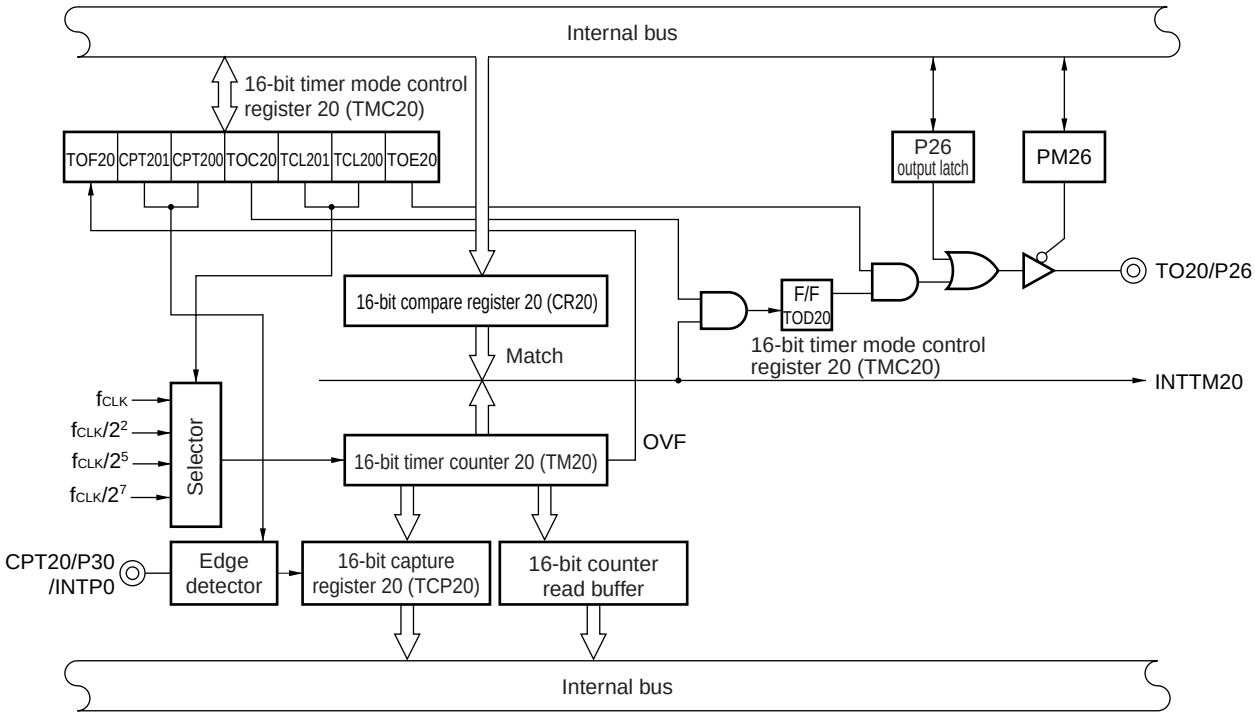
Five timer channels are incorporated.

- 16-bit timer (TM20): 1 channel
- 8-bit timer (TM30, TM40): 2 channels
- Watch timer (WT): 1 channel
- Watchdog timer (WTM): 1 channel

Table 5-2. Timer Operation

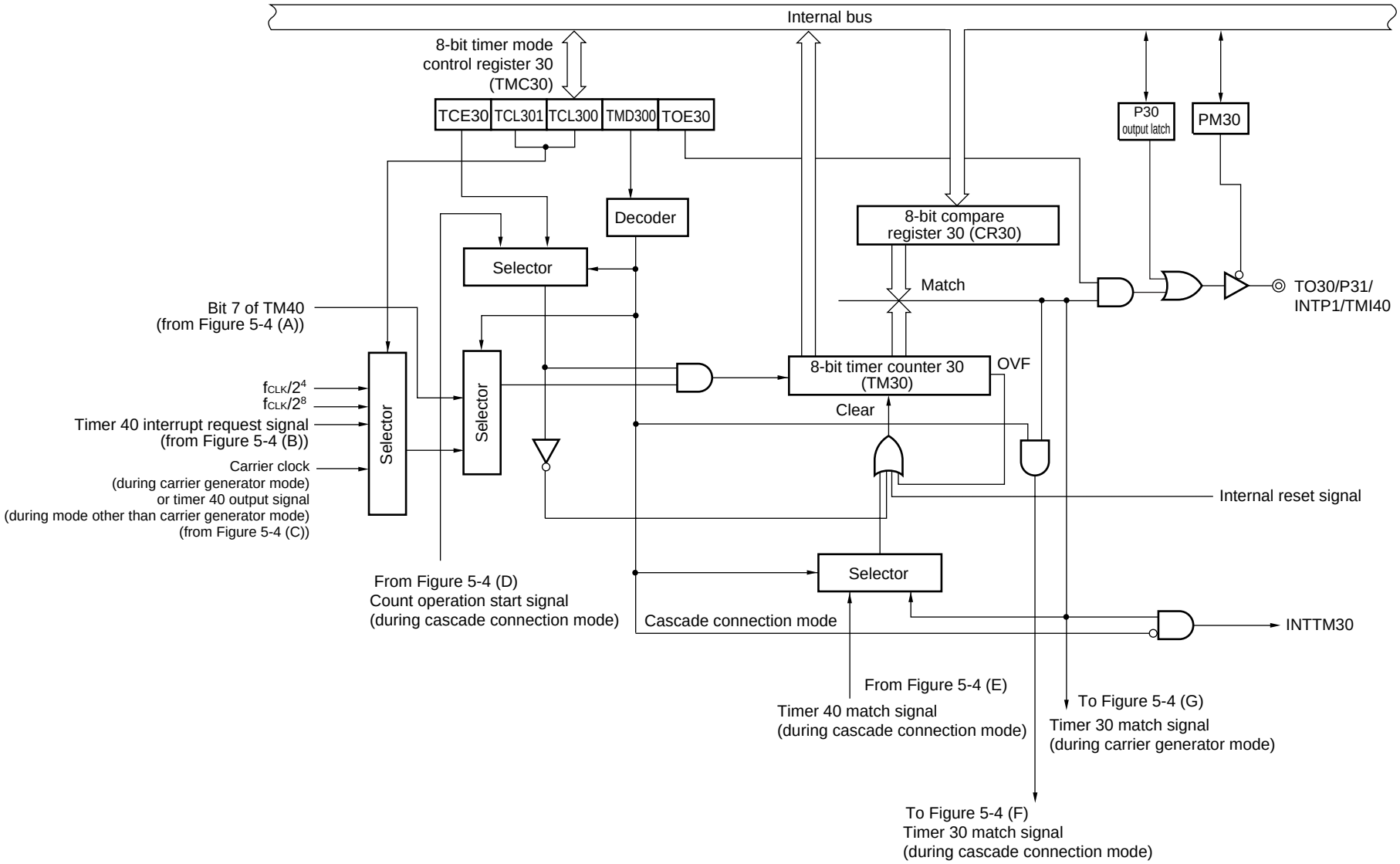
		TM20	TM30	TM40	WT	WTM
Operation mode	Interval time	1 channel	1 channel	1 channel	1 channel	1 channel
	External event counter	–	1 channel	1 channel	–	–
Function	Timer output	1 output	1 output	1 output	–	–
	Square wave output	–	1 output	1 output	–	–
	Interrupt request	1	1	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer (TM20)



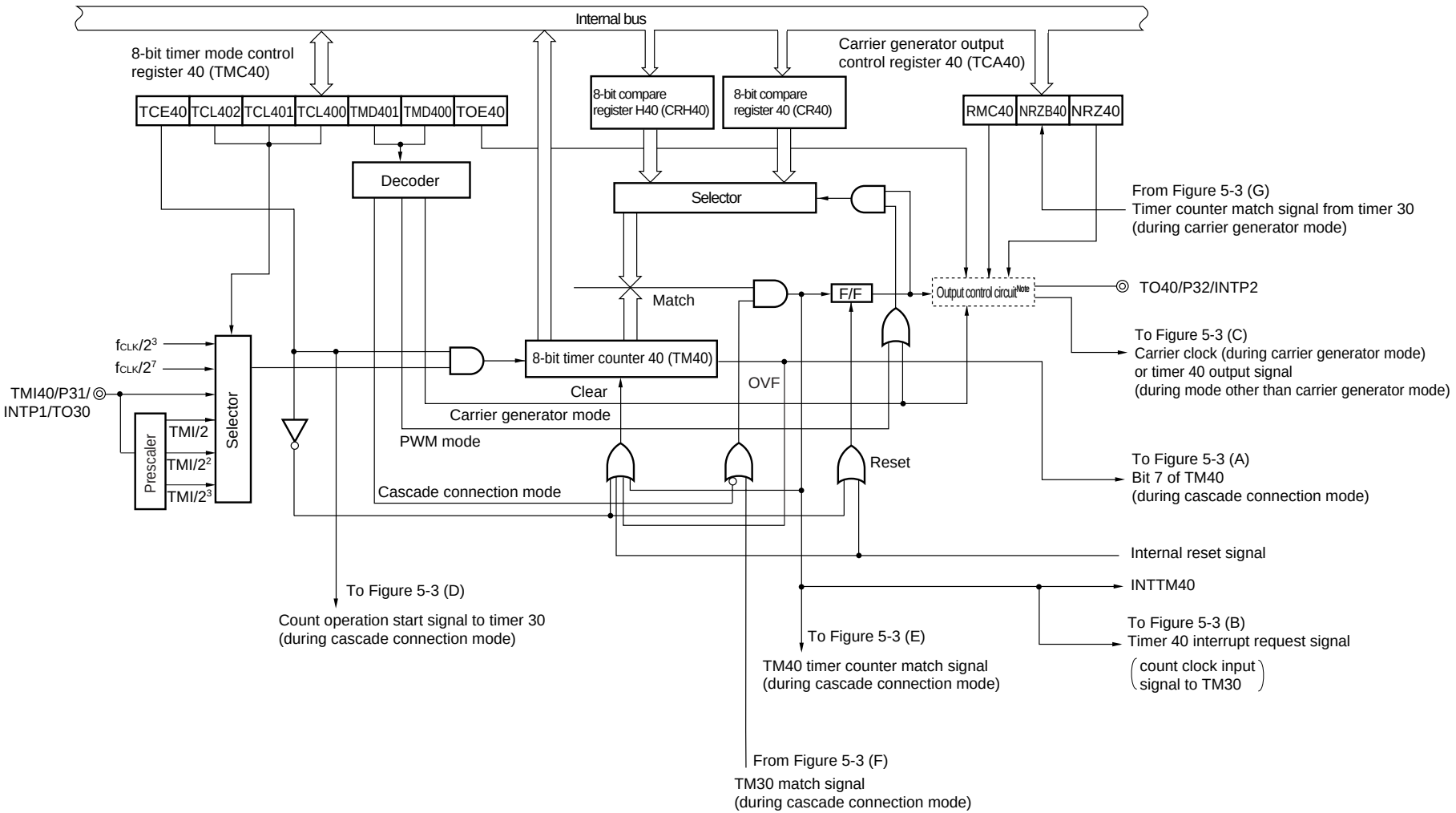
Remark f_{CLK}: fx or fCC

Figure 5-3. Block Diagram of Timer 30 (TM30)



Remark f_{CLK}: fx or f_{CC}

Figure 5-4. Block Diagram of Timer 40 (TM40)



Note For details, see **Figure 5-5**.

Remark f_{CLK}: fx or fcc

Figure 5-5. Block Diagram of Output Controller (Timer 40)

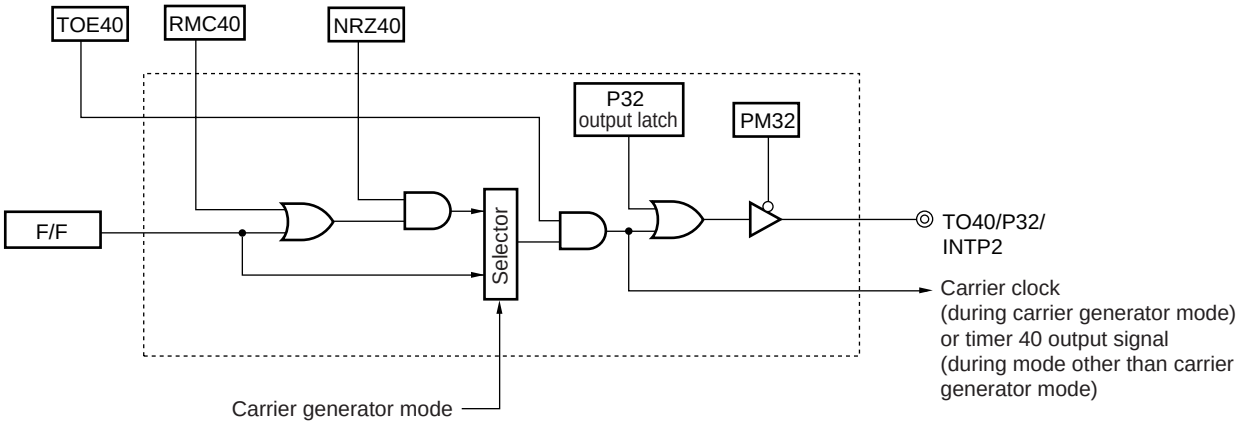
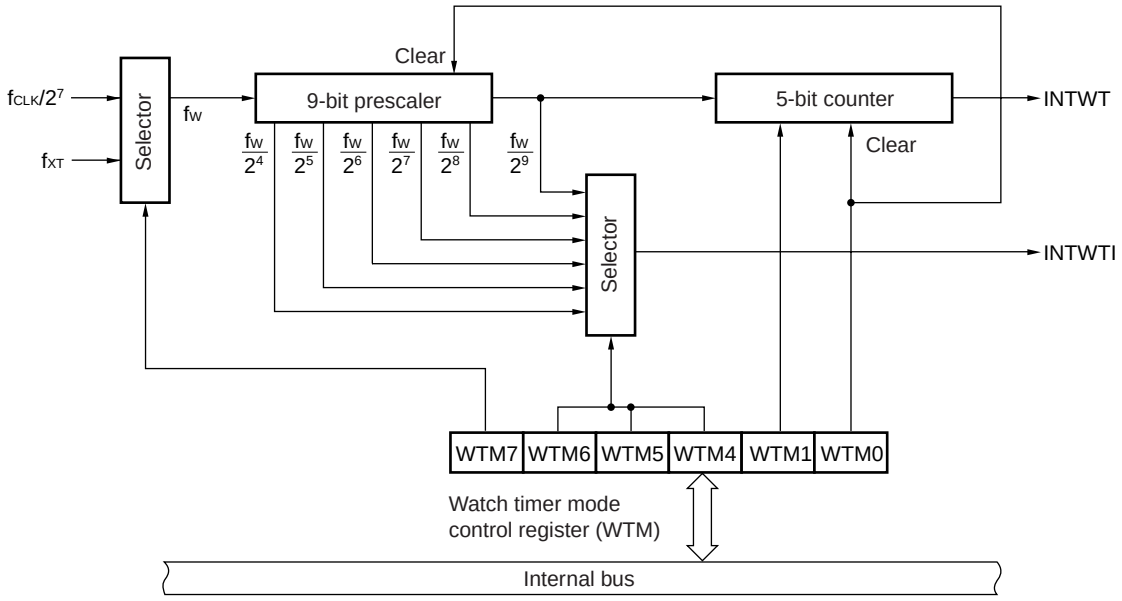
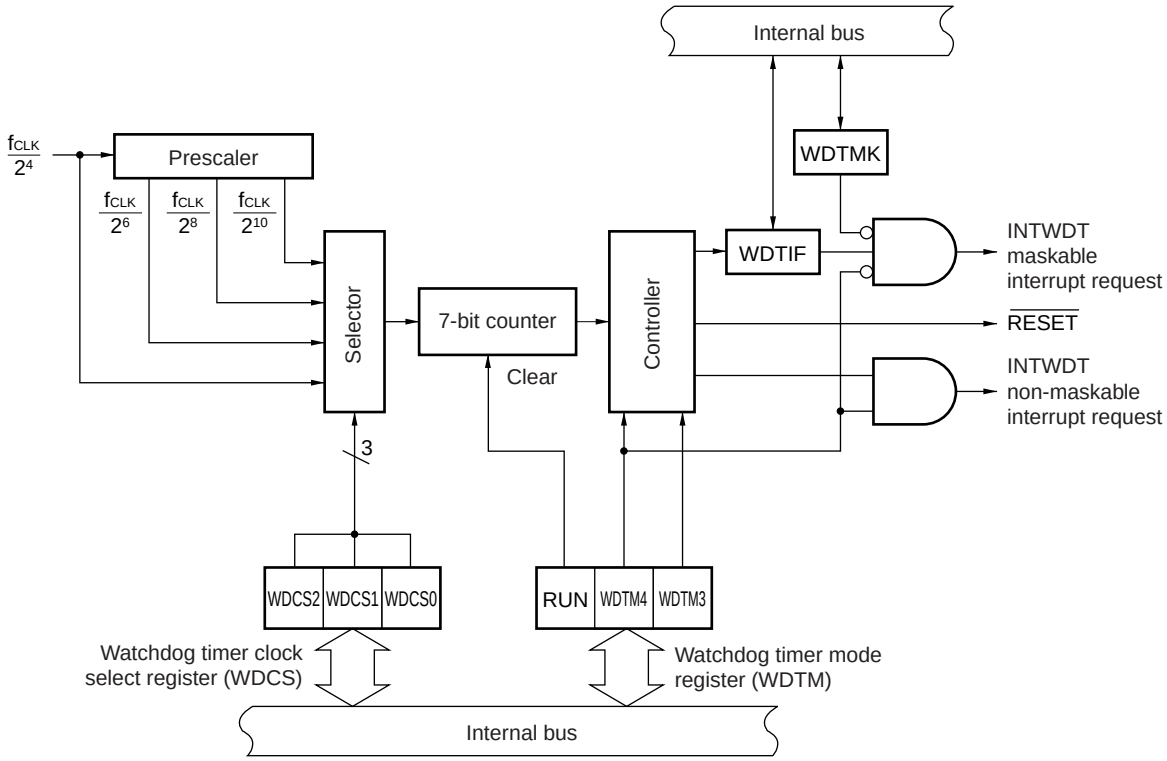


Figure 5-6. Block Diagram of Watch Timer (WT)



Remark f_{CLK}: f_X or f_{CC}

Figure 5-7. Block Diagram of Watchdog Timer (WTM)



Remark f_{CLK}: fx or f_{CC}

5.4 Serial Interface

5.4.1 Serial interface 10 (SIO10)

Serial interface 10 (SIO10) has the following two types of modes.

- Operation stop mode
- 3-wire serial I/O mode

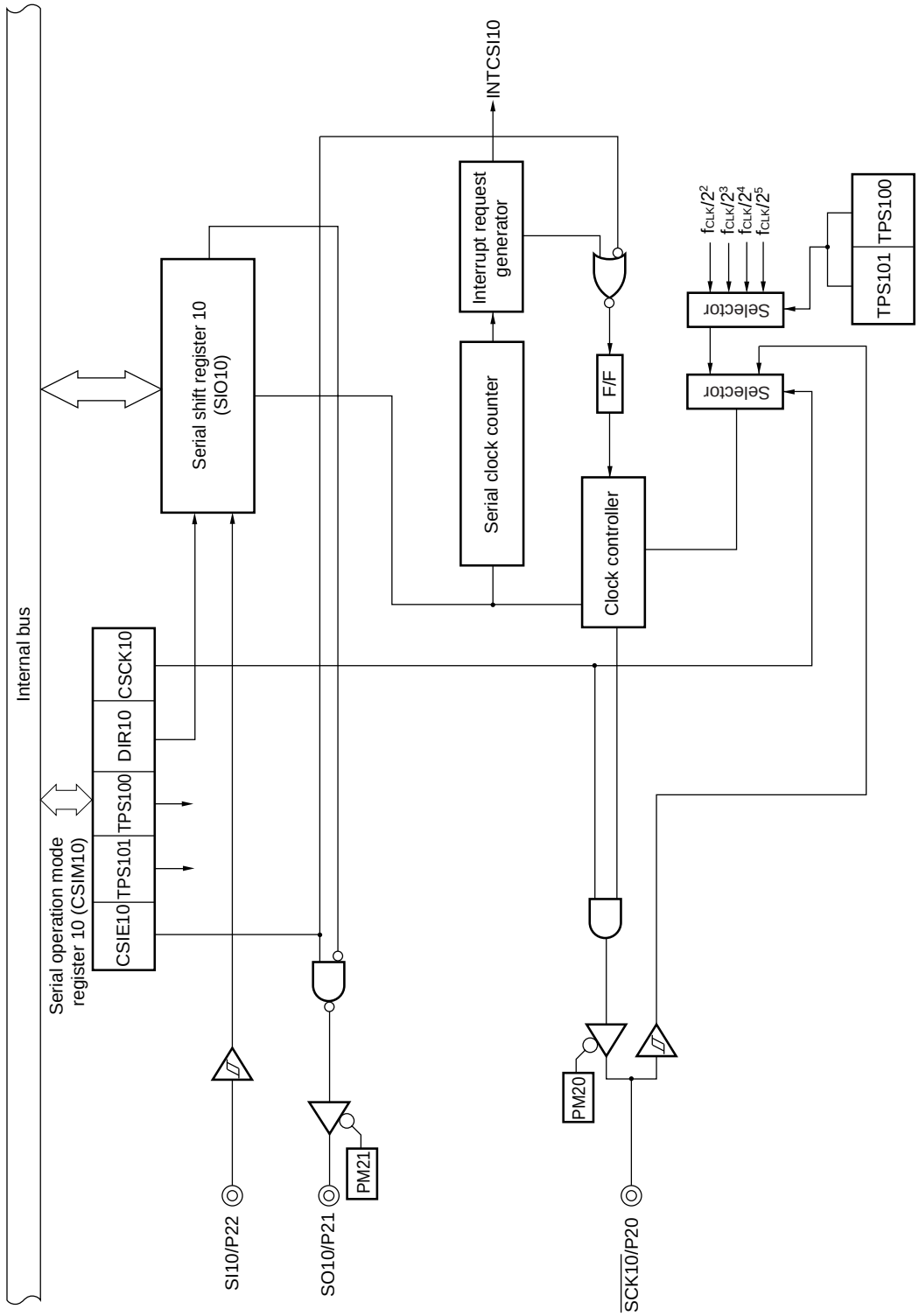


Figure 5-8. Block Diagram of Serial Interface 10

Remark f_{CLK}: fx or fcc

5.4.2 Serial interface 20 (SIO20)

Serial interface 20 (SIO20) has the following three types of modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode
- 3-wire serial I/O mode

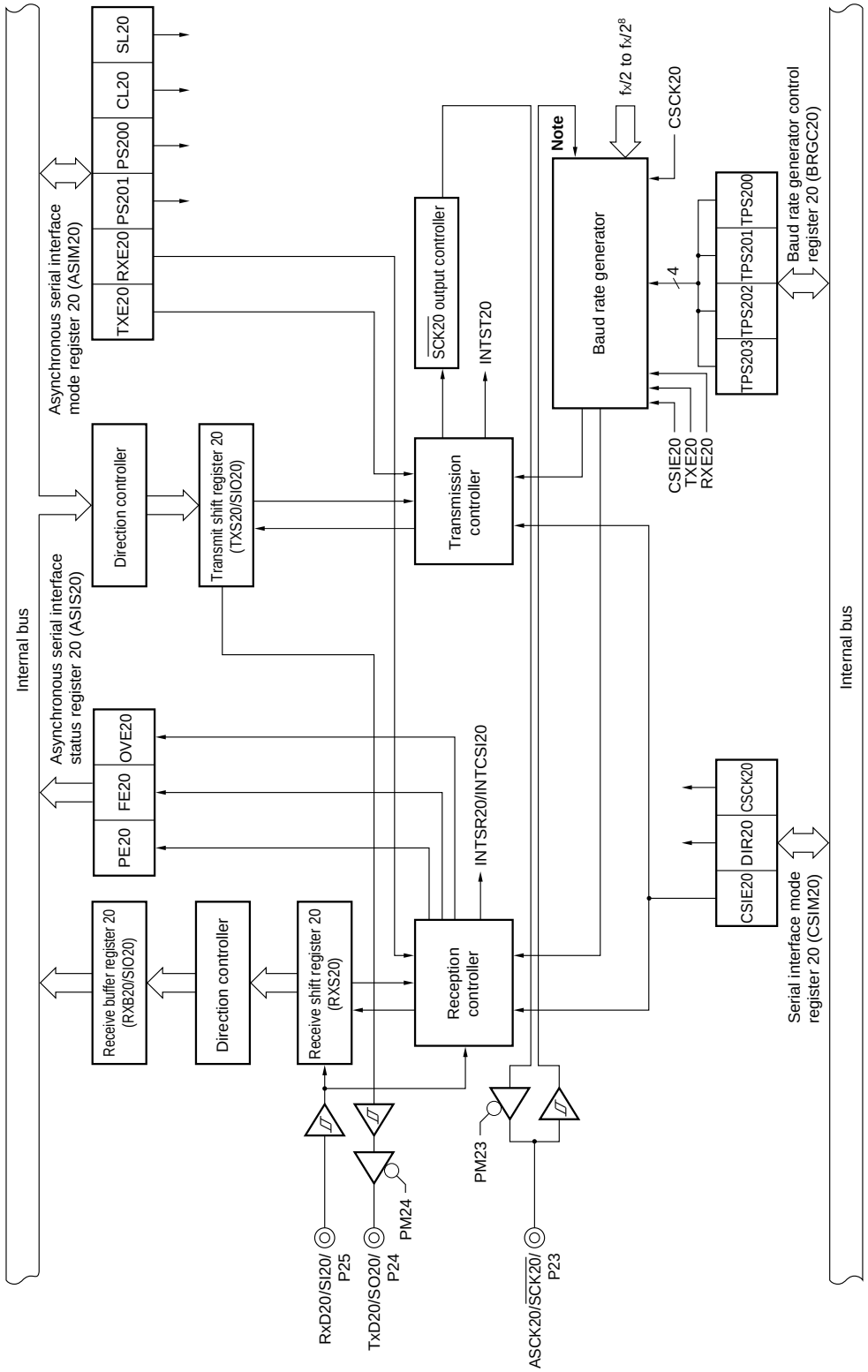


Figure 5-9. Block Diagram of Serial Interface 20

Note See **Figure 5-10** for the configuration of the baud rate generator.

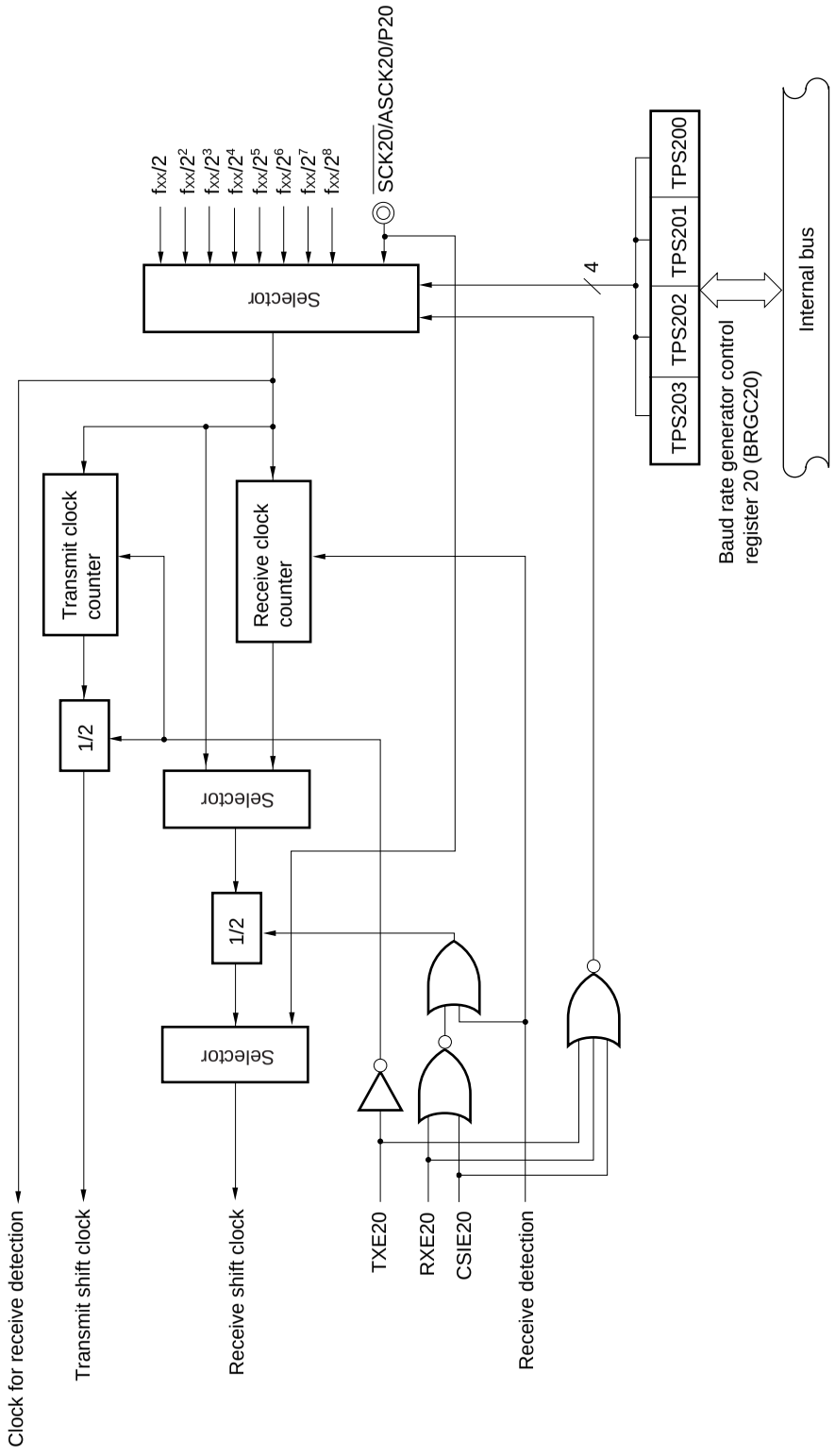


Figure 5-10. Block Diagram of Baud Rate Generator 20

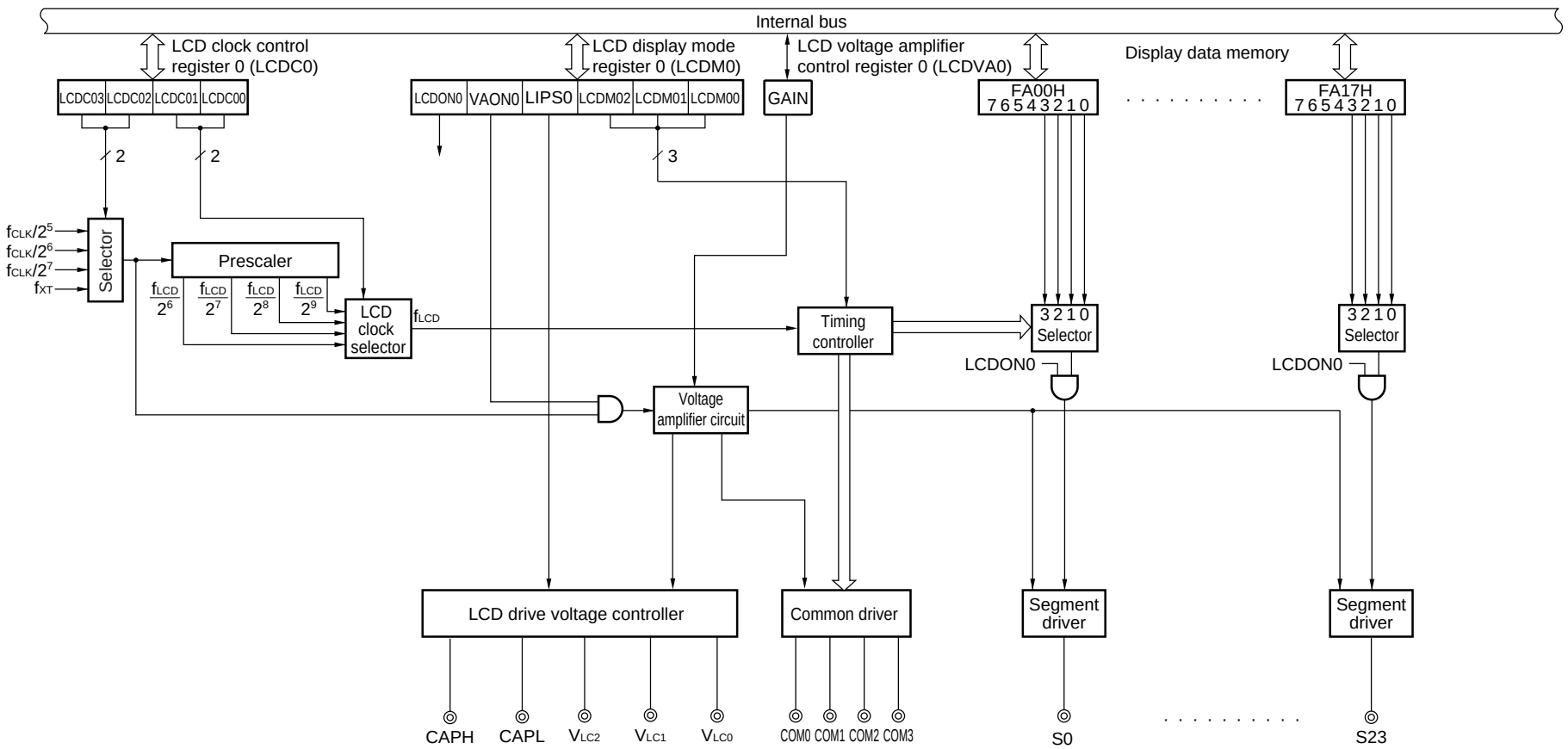
5.5 LCD Controller/Driver

The LCD controller/driver has the following functions.

(1) Enables automatic output of segment signals and common signals by automatically reading from display data memory.
(2) Two types of display modes can be selected:
- 1/3 duty (1/3 bias)
- 1/4 duty (1/3 bias)

(3) Any of four frame frequency settings can be selected for each display mode.
(4) There are up to 24 segment signal outputs (S0 to S23) and four common signal outputs (COM0 to COM3).
(5) Operation using the subsystem clock is also supported.

Figure 5-11. Block Diagram of LCD Controller/Driver



Remark f_{CLK}: fx or f_{CC}

6. INTERRUPT FUNCTIONS

A total of 15 interrupt sources divided into the following two types are provided.

- Non-maskable: 1
- Maskable: 14

Table 6-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR20	End of serial interface 20 UART reception	Internal	000EH	(B)
		INTCSI20	End of serial interface 20 3-wire SIO transfer reception			
	6	INTCSI10	End of serial interface 10 3-wire SIO transfer reception		0010H	
	7	INTST20	End of serial interface 20 UART transmission		0012H	
	8	INTWTI	Watch timer interval timer interrupt		0014H	
	9	INTTM20	Generation of match signal of 16-bit timer 20		0016H	
	10	INTTM30	Generation of match signal of 8-bit timer 30		0018H	
	11	INTTM40	Generation of match signal of 8-bit timer/event counter 40		001AH	
	12	INTWT	Watch timer interrupt		001EH	
	13	INTKR00	Key return signal detection	External	0020H	(C)

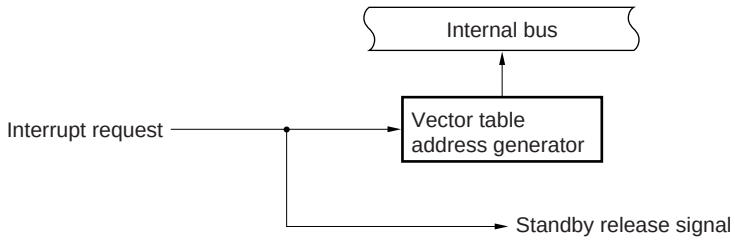
Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 13 is the lowest order.

2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 6-1.

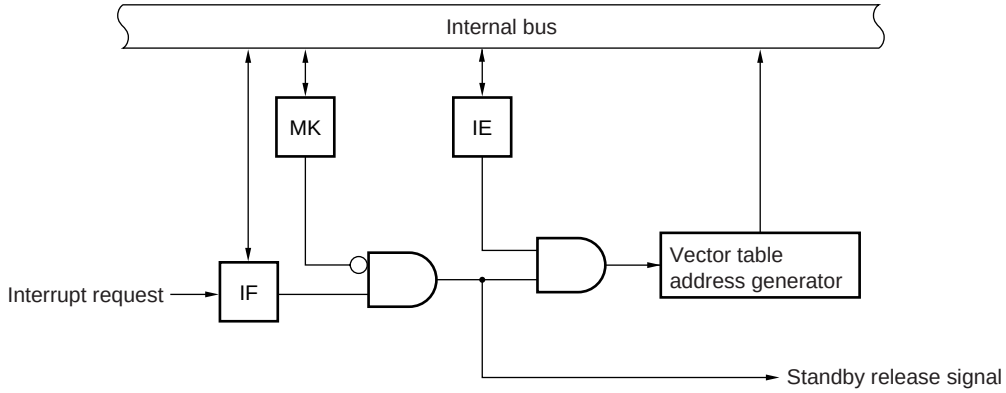
Remark Two watchdog timer interrupt sources (INTWDT): a non-maskable interrupt and a maskable interrupt (internal), are available, either of which can be selected.

Figure 6-1. Basic Configuration of Interrupt Function

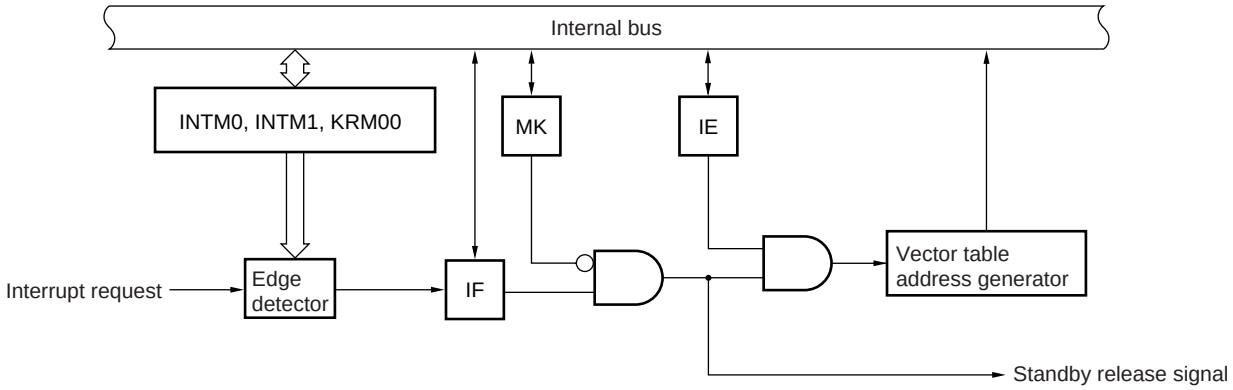
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



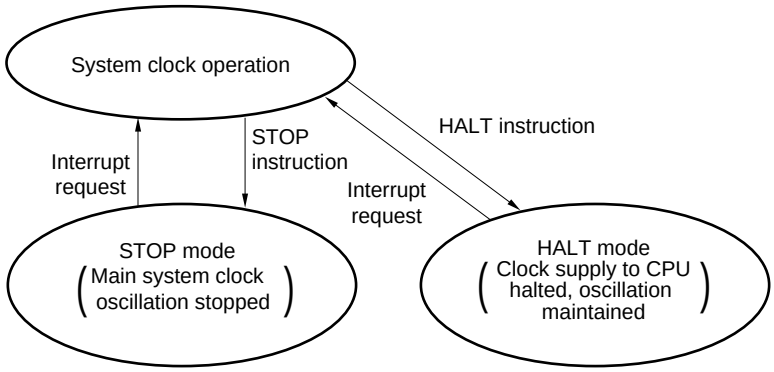
INTM0: External interrupt mode register 0
INTM1: External interrupt mode register 1
KRM00: Key return mode register 00
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7. STANDBY FUNCTION

The following two standby modes are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All operations performed on the main system clock are suspended resulting in extremely small power consumption.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer program loop time detection

9. MASK OPTIONS

The μPD789304, 789306, 789314, and 789316 have the following mask options.

- Mask options for P50 to P53
  An on-chip pull-up resistor can be selected.
  <1> Specifies on-chip pull-up resistor in 1-bit units.
  <2> Does not specify on-chip pull-up resistor.

10. OVERVIEW OF INSTRUCTION SET

This section lists the instruction set for the μPD789304, 789306, 789314, and 789316.

10.1 Conventions

10.1.1 Operand expressions and description methods

Operands are described in “Operand” column of each instruction in accordance with the description method of the instruction operand expression (see the assembler specifications for details). When there are two or more description methods, select one of them. Uppercase letters and symbols, #, !, $, and [ ] are key words and are described as they are. The meaning of each symbol is described below.

- # : Immediate data specification
- ! : Absolute address specification
- $: Relative address specification
- [ ] : Indirect address specification

For immediate data, enter an appropriate numeric value or a label. When using a label, be sure to enter the #, !, $ and [ ] symbols.

For operand register expressions, r and rp, either function names (X, A, C, etc.) or absolute names (names in parenthesis in the table below, R0, R1, R2, etc.) can be used for the description.

Table 10-1. Operand Expressions and Description Methods

Expression	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: immediate data or label FE20H to FF1FH: immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: immediate data or label (even addresses only for 16-bit data transfer instruction) 0040H to 007FH: immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

10.1.2 Description of “Operation” column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Flag indicating non-maskable interrupt servicing in progress
( ):	Memory contents indicated by address or register contents in parenthesis
X_H, X_L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
$\veebar$:	Exclusive logical sum (exclusive OR)
$\overline{\quad}$:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

10.1.3 Description of “Flag” column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
×:	Set/cleared according to the result
R:	Previously saved value is restored

10.2 List of Operations

Mnemonic	Operand	Bytes	Clocks	Operation	Flags Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			
XCHW	AX, rp Note 3	1	8	AX ↔ rp			

Notes 1. Except r = A

2. Except r = A, X

3. rp = BC, DE and HL only

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags
					Z AC CY
OR	A, #byte	2	4	A ← A ∨ byte	×
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×
	A, r	2	4	A ← A ∨ r	×
	A, saddr	2	4	A ← A ∨ (saddr)	×
	A, !addr16	3	8	A ← A ∨ (addr16)	×
	A, [HL]	1	6	A ← A ∨ (HL)	×
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×
XOR	A, #byte	2	4	A ← A ⊻ byte	×
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×
	A, r	2	4	A ← A ⊻ r	×
	A, saddr	2	4	A ← A ⊻ (saddr)	×
	A, !addr16	3	8	A ← A ⊻ (addr16)	×
	A, [HL]	1	6	A ← A ⊻ (HL)	×
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×
CMP	A, #byte	2	4	A – byte	× × ×
	saddr, #byte	3	6	(saddr) – byte	× × ×
	A, r	2	4	A – r	× × ×
	A, saddr	2	4	A – (saddr)	× × ×
	A, !addr16	3	8	A – (addr16)	× × ×
	A, [HL]	1	6	A – (HL)	× × ×
	A, [HL + byte]	2	6	A – (HL + byte)	× × ×
ADDW	AX, #word	3	6	AX, CY ← AX + word	× × ×
SUBW	AX, #word	3	6	AX, CY ← AX – word	× × ×
CMPW	AX, #word	3	6	AX – word	× × ×
INC	r	2	4	r ← r + 1	× ×
	saddr	2	4	(saddr) ← (saddr) + 1	× ×
DEC	r	2	4	r ← r – 1	× ×
	saddr	2	4	(saddr) ← (saddr) – 1	× ×
INCW	rp	1	4	rp ← rp + 1	
DECW	rp	1	4	rp ← rp – 1	
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1 time	×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1 time	×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1 time	×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1 time	×

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags
					Z AC CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1	
	sfr. bit	3	6	sfr. bit ← 1	
	A. bit	2	4	A. bit ← 1	
	PSW. bit	3	6	PSW. bit ← 1	× × ×
	[HL]. bit	2	10	(HL). bit ← 1	
CLR1	saddr. bit	3	6	(saddr. bit) ← 0	
	sfr. bit	3	6	sfr. bit ← 0	
	A. bit	2	4	A. bit ← 0	
	PSW. bit	3	6	PSW. bit ← 0	× × ×
	[HL]. bit	2	10	(HL). bit ← 0	
SET1	CY	1	2	CY ← 1	1
CLR1	CY	1	2	CY ← 0	0
NOT1	CY	1	2	CY ← $\overline{CY}$	×
CALL	!addr16	3	6	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, PC ← addr16, SP ← SP – 2	
CALLT	[addr5]	1	8	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_H \leftarrow (00000000, addr5+1)$, $PC_L \leftarrow (00000000, addr5)$, SP ← SP – 2	
RET		1	6	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, SP ← SP + 2	
RETI		1	8	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R R R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1	
	rp	1	4	$(SP-1) \leftarrow rp_H$, $(SP-2) \leftarrow rp_L$, SP ← SP – 2	
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R R R
	rp	1	6	$rp_H \leftarrow (SP+1)$, $rp_L \leftarrow (SP)$, SP ← SP + 2	
MOVW	SP, AX	2	8	SP ← AX	
	AX, SP	2	6	AX ← SP	
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	$PC_H \leftarrow A$, $PC_L \leftarrow X$	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flags
					Z AC CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}			–0.3 to +6.5	V
Input voltage	V_{I1}	P00 to P03, P10 to P13, P20 to P26, P30 to P33, X1 (CL1), X2 (CL2), XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3[Note]	V
	V_{I2}	P50 to P53	N-ch open drain	–0.3 to +13	V
			On-chip pull-up resistor	–0.3 to V_{DD} + 0.3[Note]	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3[Note]	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for all pins		–30	mA
Output current, low	I_{OL}	Per pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note 6.5 V or less

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

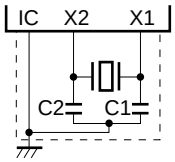
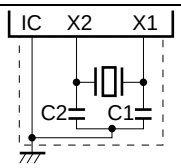
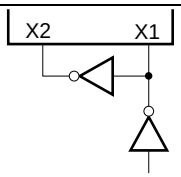
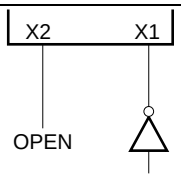
Remarks 1. Pin names enclosed in parentheses are when using the μPD789304, 789306.

2. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics

Ceramic/crystal oscillation (μPD789304, 789306)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequencyNote 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
★		X1 input frequency (f_X)Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

★ **2.** Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation stabilizes within the oscillation stabilization wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

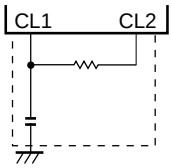
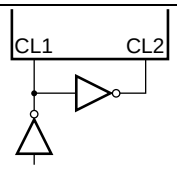
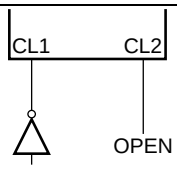
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

RC oscillation (μPD789314, 789316)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator		Oscillation frequency (f_{CC})[Note 1]		2.0		4.0	MHz
★		Oscillation stabilization time[Note 2]	V_{DD} = 2.7 to 5.5 V	32			μs
				128			μs
External clock		CL1 input frequency (f_{CC})[Note 1]		1.0		4.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		100		500	ns
★		CL1 input frequency (f_{CC})[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		4.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	100		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

★ **2.** Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

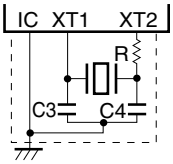
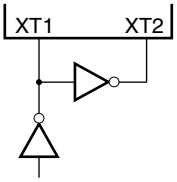
★ **RC Oscillation Frequency Characteristics (T_A = –40 to +85°C)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{CC1}	R = 11.0 kΩ, C = 22 pF Target: 2 MHz	V_{DD} = 2.7 to 5.5 V	1.5	2.0	2.5	MHz
	f_{CC2}		V_{DD} = 1.8 to 3.6 V	0.5	2.0	2.5	MHz
	f_{CC3}		V_{DD} = 1.8 to 5.5 V	0.5	2.0	2.5	MHz
	f_{CC4}	R = 6.8 kΩ, C = 22 pF Target: 3 MHz	V_{DD} = 2.7 to 5.5 V	2.5	3.0	3.5	MHz
	f_{CC5}		V_{DD} = 1.8 to 3.6 V	0.75	3.0	3.5	MHz
	f_{CC6}		V_{DD} = 1.8 to 5.5 V	0.75	3.0	3.5	MHz
	f_{CC7}	R = 4.7 kΩ, C = 22 pF Target: 4 MHz	V_{DD} = 2.7 to 5.5 V	3.5	4.0	4.7	MHz
	f_{CC8}		V_{DD} = 1.8 to 3.6 V	1.0	4.0	4.7	MHz
	f_{CC9}		V_{DD} = 1.8 to 5.5 V	1.0	4.0	4.7	MHz

Remarks 1. Set the RC to one of the above nine values so that the typical value of the oscillation frequency is within 2.0 to 4.0 MHz.

2. The resistor (R) and capacitor (C) error is not included.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/4)

	Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
	Output current, low	I_{OL}	Per pin					10	mA
			All pins					80	mA
	Output current, high	I_{OH}	Per pin					–1	mA
			All pins					–15	mA
	Input voltage, high	V_{IH1}	P10 to P13		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
						0.9V_{DD}		V_{DD}	V
		V_{IH2}	P50 to P53	N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
						0.9V_{DD}		12	V
				On-chip pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
						0.9V_{DD}		V_{DD}	V
		V_{IH3}	$\overline{RESET}$, P00 to P03, P20 to P26, P30 to P33		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
						0.9V_{DD}		V_{DD}	V
★		V_{IH4}	X1 (CL1), X2 (CL2), XT1, XT2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
						V_{DD} – 0.1		V_{DD}	V
	Input voltage, low	V_{IL1}	P10 to P13		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
						0		0.1V_{DD}	V
		V_{IL2}	P50 to P53		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
						0		0.1V_{DD}	V
		V_{IL3}	$\overline{RESET}$, P00 to P03, P20 to P26, P30 to P33		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
						0		0.1V_{DD}	V
★		V_{IL4}	X1 (CL1), X2 (CL2), XT1, XT2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
						0		0.1	V
	Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
			V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
	Output voltage, low	V_{OL1}	P00 to P03, P10 to P13, P20 to P26, P30 to P33		4.5 ≤ V_{DD} ≤ 5.5 V, I_{OL} = 10 mA			1.0	V
					1.8 ≤ V_{DD} < 4.5 V, I_{OL} = 400 μA			0.5	V
		V_{OL2}	P50 to P53		4.5 ≤ V_{DD} < 5.5 V, I_{OL} = 10 mA			1.0	V
					1.8 ≤ V_{DD} < 4.5 V, I_{OL} = 1.6 mA			0.4	V

Remarks 1. Pin names enclosed in parentheses are when using the μPD789314, 789316.

2. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P13, P20 to P26, P30 to P33, RESET			3	μA
	I_{LIH2}		X1 (CL1), X2 (CL2), XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P13, P20 to P26, P30 to P33, RESET			–3	μA
	I_{LIL2}		X1 (CL1), X2 (CL2), XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3[Note]	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R_1	V_{IN} = 0 V	P00 to P03, P10 to P13, P20 to P26, P30 to P33	50	100	200	kΩ
Mask option pull-up resistor	R_2	V_{IN} = 0 V	P50 to P53	10	30	60	kΩ

Note If there is no on-chip pull-up resistor for P50 to P53 (specified by the mask option), if P50 to P53 have been set to input mode when a read instruction is executed to read from P50 to P53, a low-level input leakage current of up to –30 μA flows during only one cycle. At all other times, the maximum leakage current is –3 μA.

Remarks 1. Pin names enclosed in parentheses are when using the μPD789314, 789316.

2. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (3/4)**

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1] (Ceramic/crystal oscillation)	I_{DD1}	5.0 MHz crystal oscillation operation mode (C1 = C2 = 22 pF)		V_{DD} = 5.0 V ±10%[Note 2]		1.8	2.9	mA
				V_{DD} = 3.0 V ±10%[Note 3]		0.36	0.9	mA
				V_{DD} = 2.0 V ±10%[Note 3]		0.16	0.45	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)		V_{DD} = 5.0 V ±10%[Note 2]		0.96	1.92	mA
				V_{DD} = 3.0 V ±10%[Note 3]		0.26	0.76	mA
				V_{DD} = 2.0 V ±10%[Note 3]		0.1	0.34	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)		V_{DD} = 5.0 V ±10%		30	58	μA
				V_{DD} = 3.0 V ±10%		9	26	μA
				V_{DD} = 2.0 V ±10%		4	12	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	LCD not operating	V_{DD} = 5.0 V ±10%		25	48	μA
				V_{DD} = 3.0 V ±10%		7	20	μA
				V_{DD} = 2.0 V ±10%		4	10	μA
			LCD operating[Note 5]	V_{DD} = 5.0 V ±10%		28	57	μA
				V_{DD} = 3.0 V ±10%		9.6	27.8	μA
				V_{DD} = 2.0 V ±10%		6	16	μA
	I_{DD5}	STOP mode[Note 6]		V_{DD} = 5.0 V ±10%		0.1	10	μA
				V_{DD} = 3.0 V ±10%		0.05	5.0	μA
				V_{DD} = 2.0 V ±10%		0.05	3.0	μA

Notes 1. The port current (including the current that flows to the on-chip pull-up resistor) is not included.

2. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when PCC is set to 02H)

4. When the main system clock is stopped

5. This is the total current that flows when the LCD controller/driver is operating (LCDON0 = 1, VAON0 = 1, LIPS0 = 1). The power supply current when the LCD is not operating (LCDON0 = 0, VAON0 = 1, LIPS0 = 0) is included in I_{DD2}.

6. This is the current when the LCD voltage booster circuit is stopped (LCDON0 = 0, VAON0 = 1).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (4/4)**

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1] (RC oscillation)	I_{DD1}	4.0 MHz RC oscillation operation mode (R = 4.7 kΩ, C = 22 pF)		V_{DD} = 5.0 V ±10%[Note 2]		1.65	3.0	mA
				V_{DD} = 3.0 V ±10%[Note 3]		0.65	1.44	mA
				V_{DD} = 2.0 V ±10%[Note 3]		0.38	1.05	mA
	I_{DD2}	4.0 MHz RC oscillation HALT mode (R = 4.7 kΩ, C = 22 pF)		V_{DD} = 5.0 V ±10%[Note 2]		1.1	2.29	mA
				V_{DD} = 3.0 V ±10%[Note 3]		0.6	1.28	mA
				V_{DD} = 2.0 V ±10%[Note 3]		0.35	0.82	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)		V_{DD} = 5.0 V ±10%		30	58	μA
				V_{DD} = 3.0 V ±10%		9	26	μA
				V_{DD} = 2.0 V ±10%		4	12	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	LCD not operating	V_{DD} = 5.0 V ±10%		25	48	μA
				V_{DD} = 3.0 V ±10%		7	20	μA
				V_{DD} = 2.0 V ±10%		4	10	μA
			LCD operating[Note 5]	V_{DD} = 5.0 V ±10%		28	57	μA
				V_{DD} = 3.0 V ±10%		9.6	27.8	μA
				V_{DD} = 2.0 V ±10%		6	16	μA
	I_{DD5}	STOP mode[Note 6]		V_{DD} = 5.0 V ±10%		0.1	10	μA
				V_{DD} = 3.0 V ±10%		0.05	5.0	μA
				V_{DD} = 2.0 V ±10%		0.05	3.0	μA

Notes 1. The port current (including the current that flows to the on-chip pull-up resistor) is not included.

2. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when PCC is set to 02H)

4. When the main system clock is stopped

5. This is the total current that flows when the LCD controller/driver is operating (LCDON0 = 1, VAON0 = 1, LIPS0 = 1). The power supply current when the LCD is not operating (LCDON0 = 0, VAON0 = 1, LIPS0 = 0) is included in I_{DD2}.

6. This is the current when the LCD voltage booster circuit is stopped (LCDON0 = 0, VAON0 = 1).

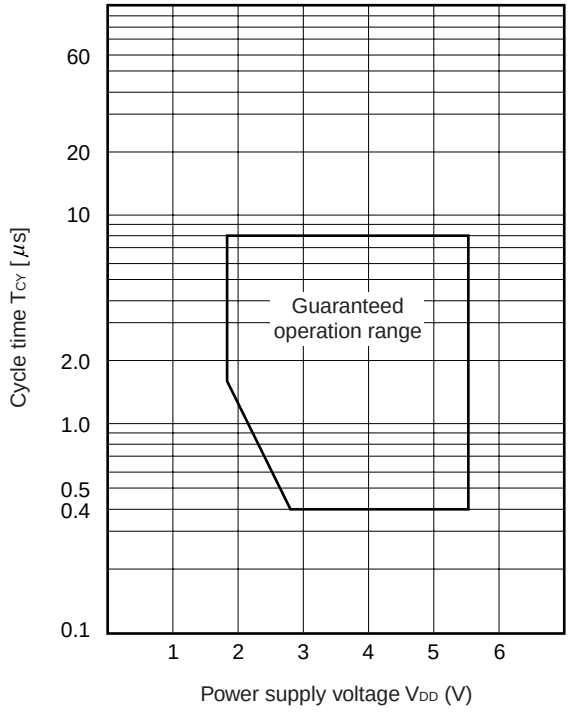
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY1}	Operating with main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8.0	μs
				1.6		8.0	μs
		Operating with subsystem clock		114	122	125	μs
TMI40 input frequency	f_{TMI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
★ TMI40 input high-/low-level width	t_{TIMH}, t_{TIML}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
Key return input low-level width	t_{KRL}	KR00 to KR03		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface 10, 20 (SIO10, SIO20) (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode (internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKn0}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCKn0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SIn0 setup time (to $\overline{SCKn0}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SIn0 hold time (from $\overline{SCKn0}$↑)	t_{SI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
Delay time from $\overline{SCKn0}$↓ to SOn0 output	t_{SO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SOn0 output lines.

Remark n = 1, 2

(b) 3-wire serial I/O mode (external clock input)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★	$\overline{SCKn0}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
★					3200			ns
	$\overline{SCKn0}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
					1600			ns
	SIn0 setup time (to $\overline{SCKn0}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
					150			ns
	SIn0 hold time (from $\overline{SCKn0}$↑)	t_{SI2}	V_{DD} = 2.7 to 5.5 V		400			ns
					600			ns
	Delay time from $\overline{SCKn0}$↓ to SOn0 output	t_{SO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
					0		1000	ns

Note R and C are the load resistance and load capacitance of the SOn0 output lines.

Remark n = 1, 2

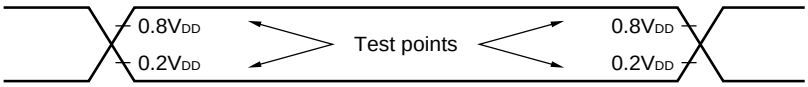
(c) UART mode (SIO20 only) (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

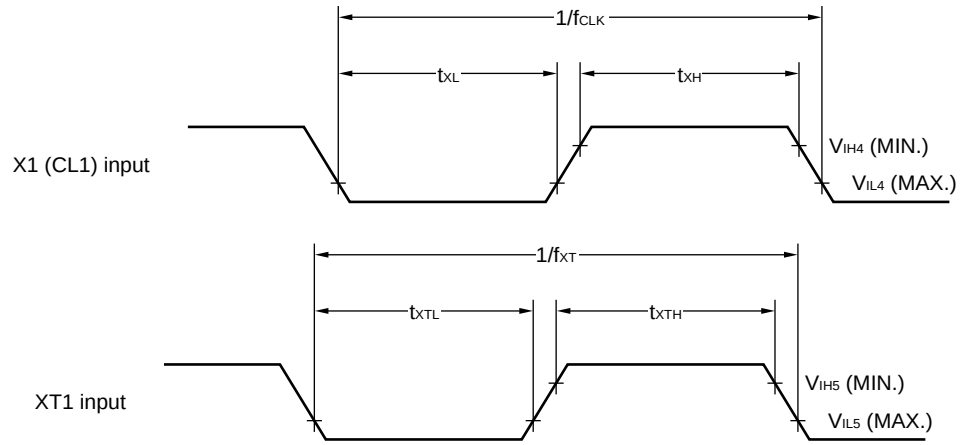
(d) UART mode (SIO20 only) (external clock input)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
★				3200			ns
	ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
				1600			ns
	Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
						9766	bps
	ASCK20 rise/fall time	t_R, t_F				1	μs

AC Timing Test Points (excluding X1 (CL1) and XT1 inputs)

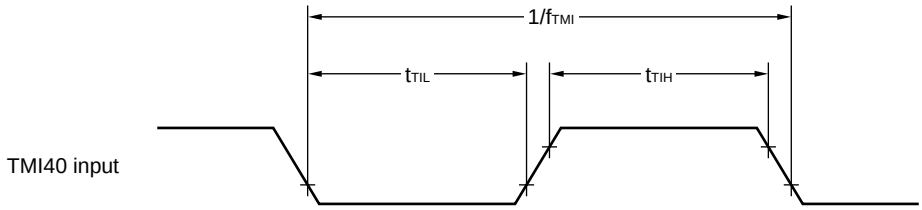


Clock Timing

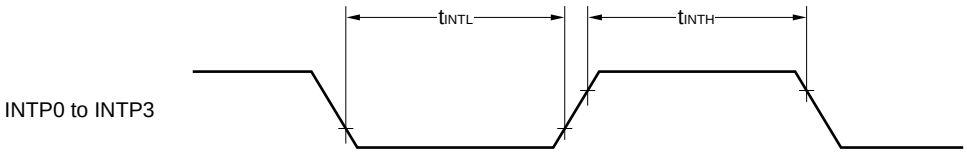


Remark f_{CLK}: fx or fCC

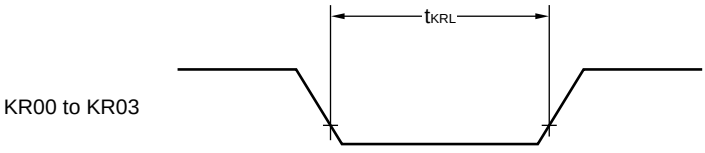
TMI Timing



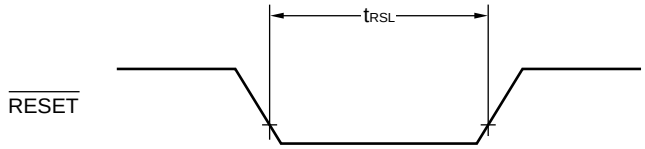
Interrupt Input Timing



Key Return Input Timing

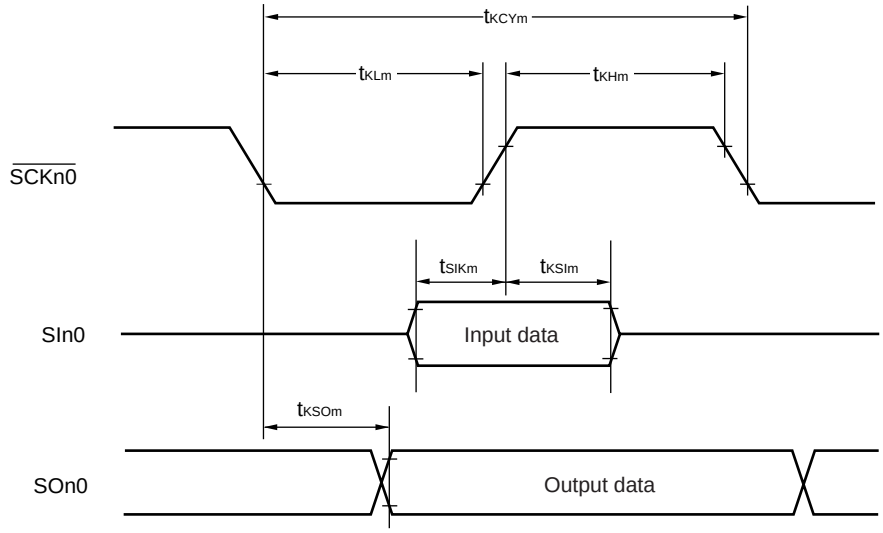


$\overline{\text{RESET}}$ Input Timing



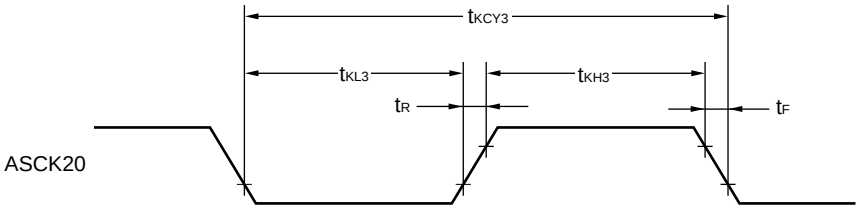
Serial Transfer Timing

3-wire serial I/O mode:



Remark n, m = 1, 2

UART mode (external clock input):



★ **LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{LCD2}	c1 to c4 = 0.47 μF	GAIN = 1	0.84	1.0	1.165	V
			GAIN = 0	1.26	1.5	1.74	V
Doubler output	V_{LCD1}	c1 to c4 = 0.47 μF		$2V_{LCD2}$ – 0.1	$2.0V_{LCD2}$	$2.0V_{LCD2}$	V
Tripler output	V_{LCD0}	c1 to c4 = 0.47 μF		$3V_{LCD2}$ – 0.15	$3.0V_{LCD2}$	$3.0V_{LCD2}$	V
Voltage boost wait time[Note 1]	t_{VAWAIT}	GAIN = 0		0.5			s
		GAIN = 1	5.0 ≤ V_{DD} ≤ 5.5 V	2.0			s
			4.5 ≤ V_{DD} < 5.0 V	1.0			s
			1.8 ≤ V_{DD} < 4.5 V	0.5			s
LCD output voltage differential[Note 2] (common)	V_{ODC}	I_O = ±5 μA		0		±0.2	V
LCD output voltage differential[Note 2] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Notes 1. This is the wait time from when voltage boosting is started (VAON0 = 1) until display is enabled (LCDON0 = 0).

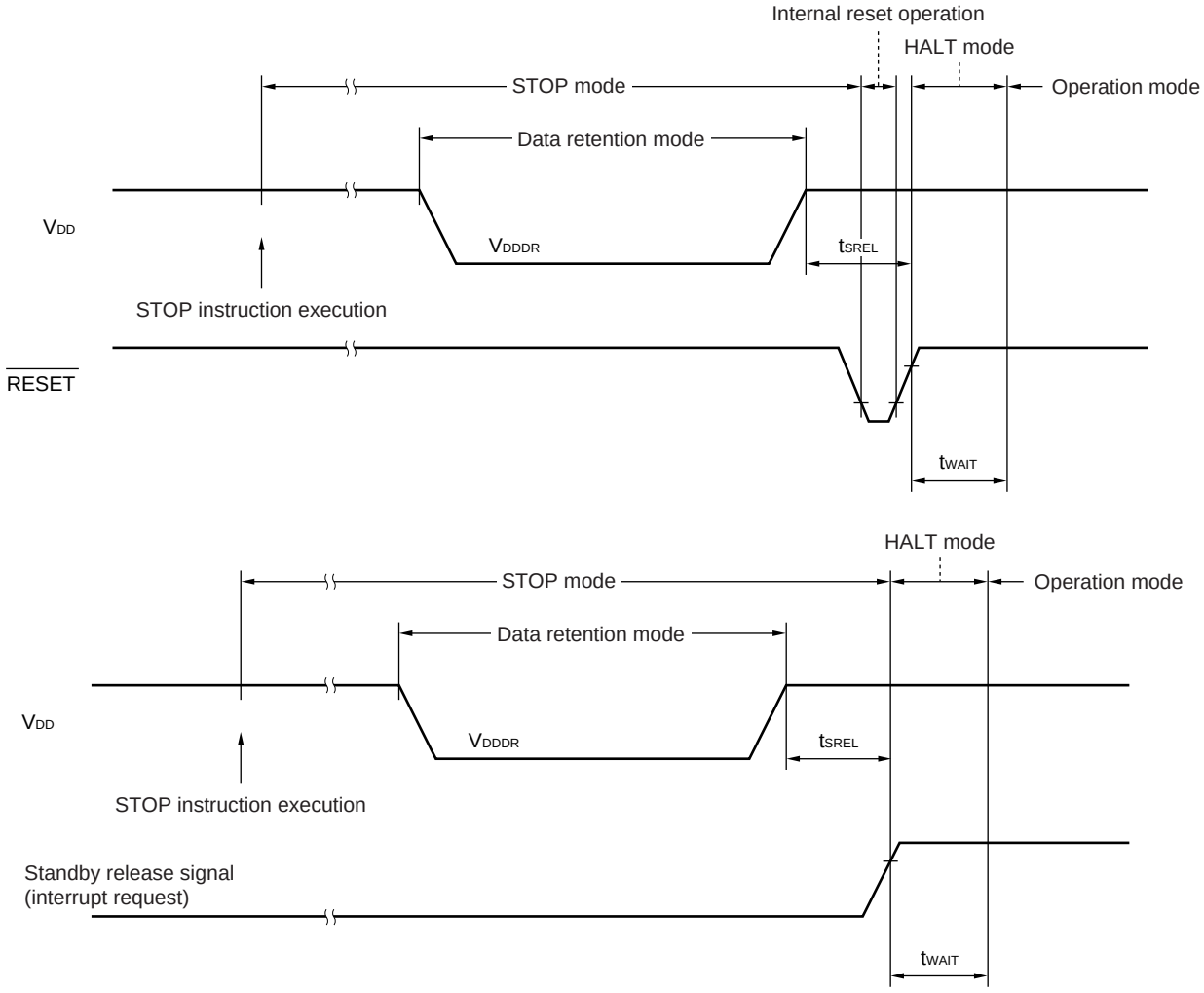
2. The voltage differential is the difference between the segment and common signal output's actual and ideal output voltages.

Remark c1: Capacitor connected between CAPH and CAPL
c2: Capacitor connected between V_{LC0} and ground
c3: Capacitor connected between V_{LC1} and ground
c4: Capacitor connected between V_{LC2} and ground

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs

Data Retention Timing



Oscillation Stabilization Wait Time (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization wait time[Note 1] (ceramic/crystal oscillation)	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt		**Note 2**		s
Oscillation stabilization wait time (RC oscillation)	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{CC}$		s
		Release by interrupt		$2^7/f_{CC}$		s

Notes 1. Use a resonator whose oscillation stabilizes within the oscillation stabilization wait time.

2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

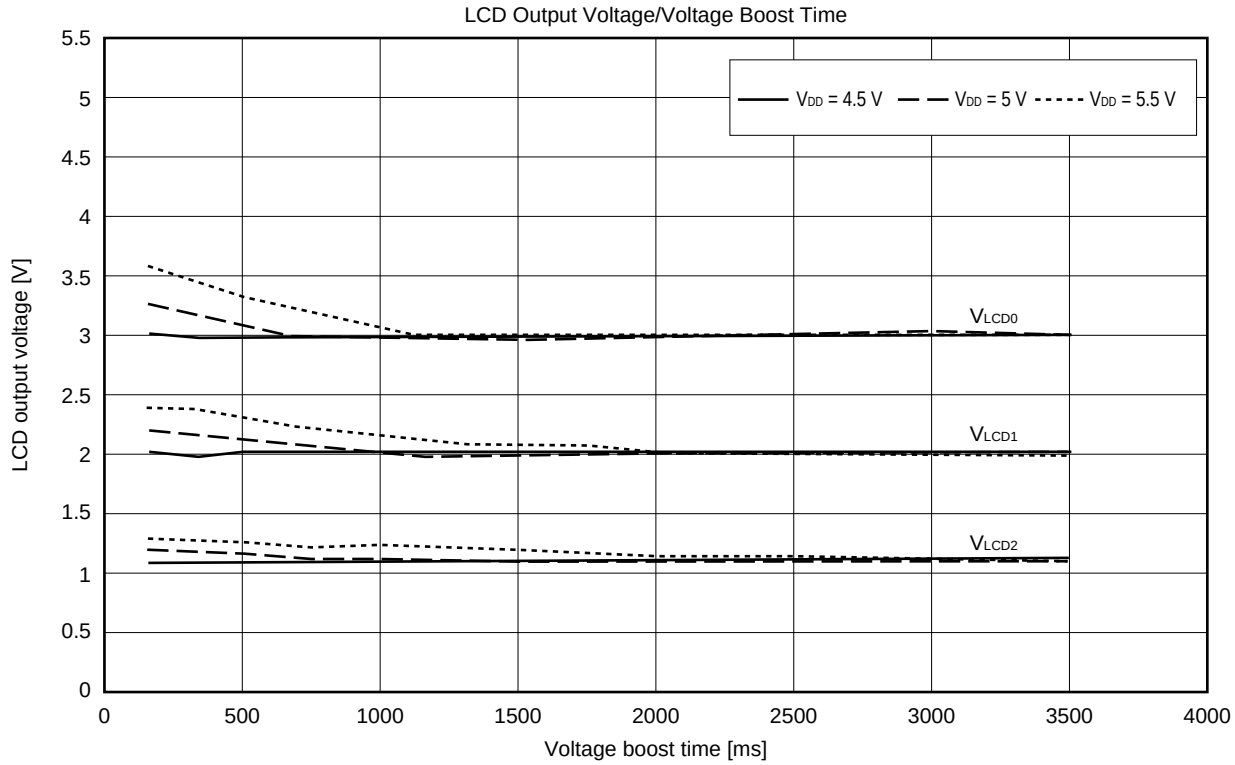
Remarks 1. f_X: Main system clock oscillation frequency (ceramic/crystal oscillation)

2. f_{CC}: Main system clock oscillation frequency (RC oscillation)

★ 12. CHARACTERISTICS CURVES OF LCD CONTROLLER/DRIVER (REFERENCE VALUES)

(1) Characteristics curves of voltage boost stabilization time

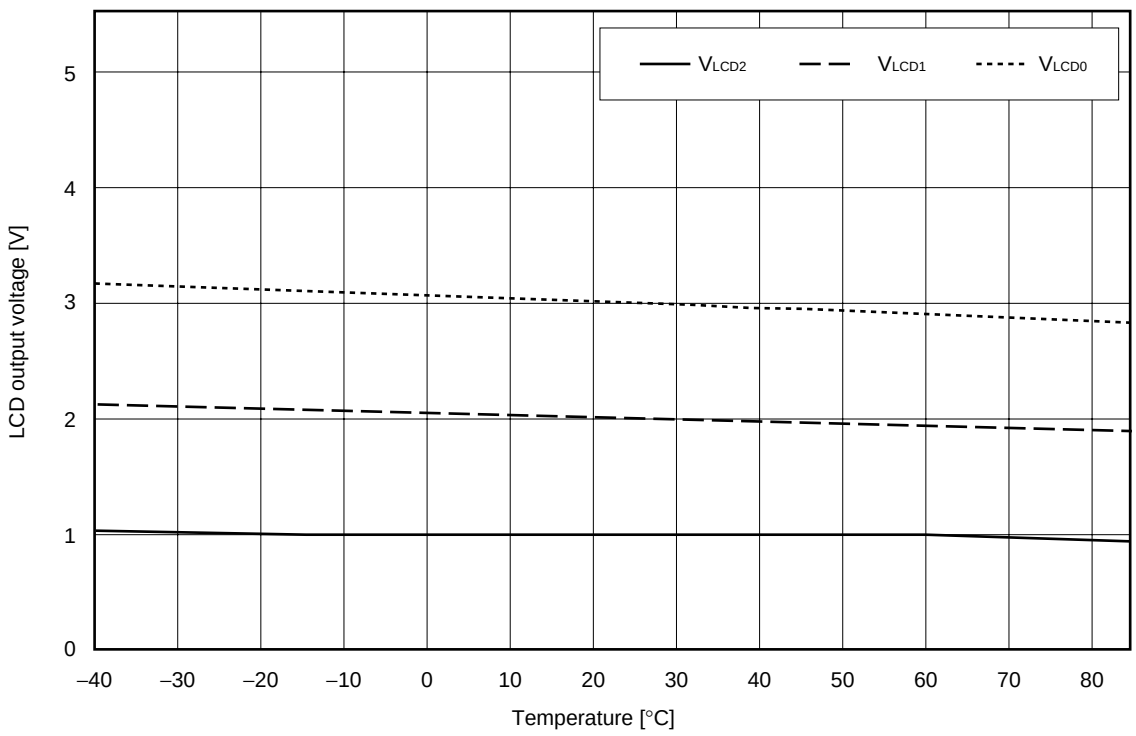
The following shows the characteristics curves of the time from the start of voltage boost (VAON0 = 1) and the changes in the LCD output voltage (when GAIN is set to 1 (using the 3 V display panel))



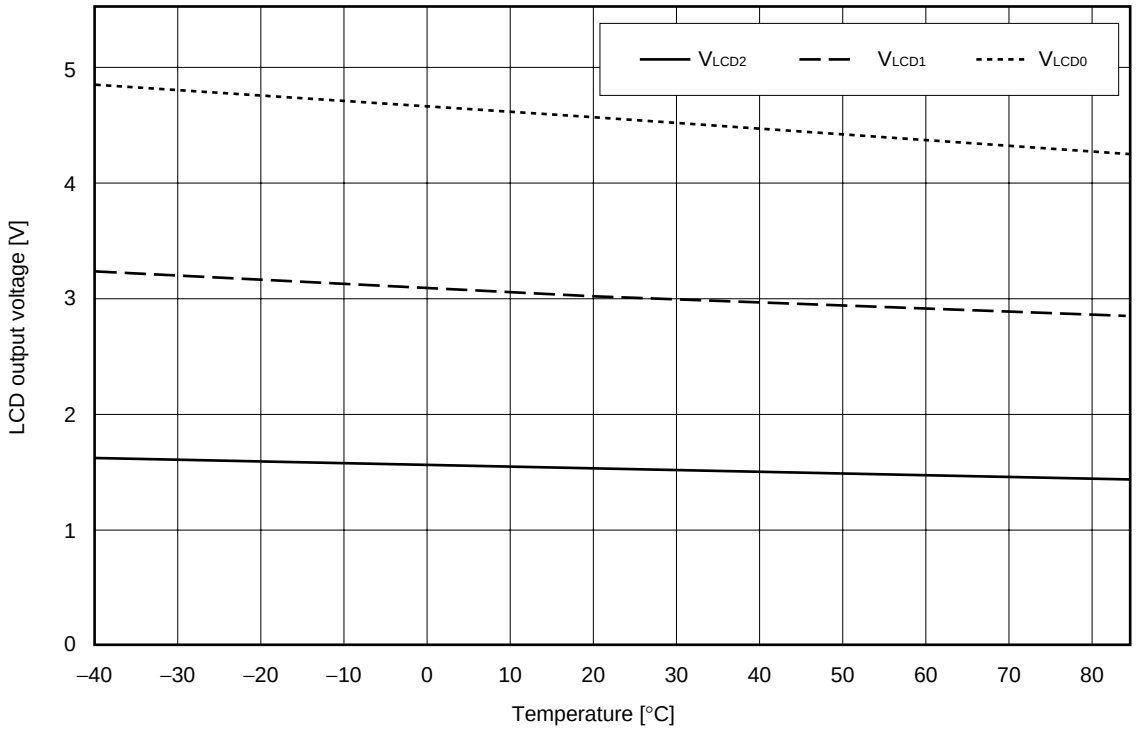
(2) Temperature characteristics of LCD output voltage

The following shows the temperature characteristics curves of LCD output voltage.

LCD Output Voltage/Temperature (When GAIN = 1)

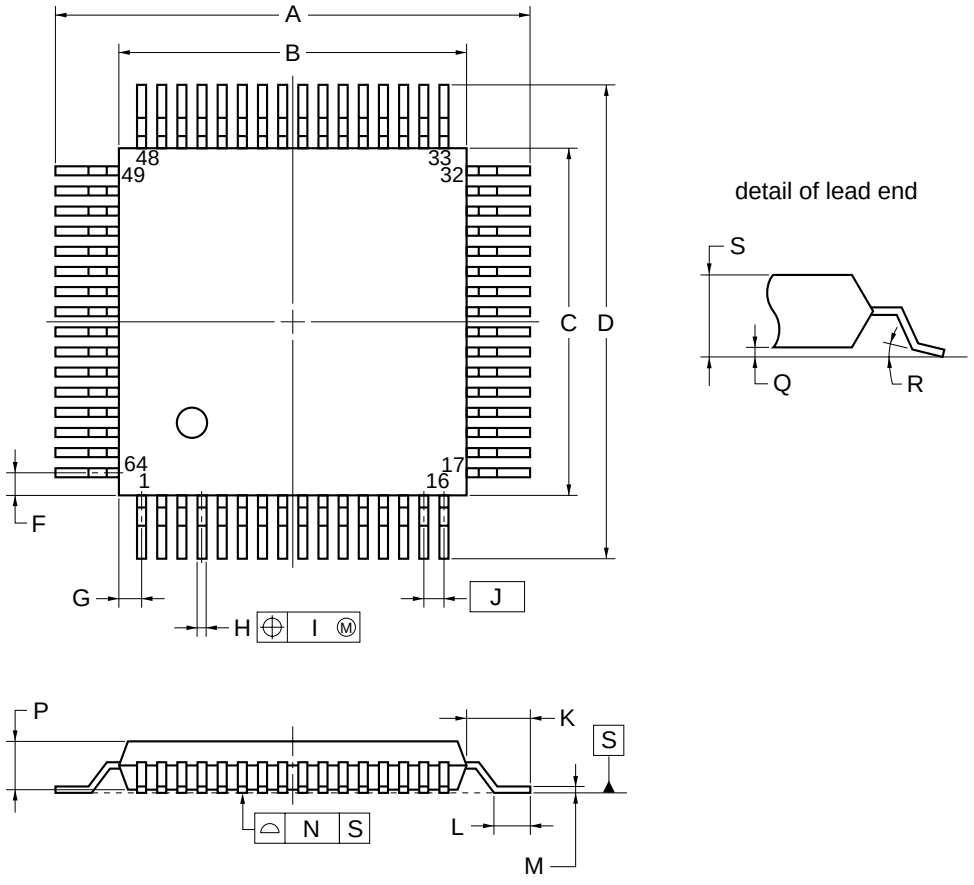


LCD Output Voltage/Temperature (When GAIN = 0)



13. PACKAGE DRAWINGS

64-PIN PLASTIC QFP (14x14)



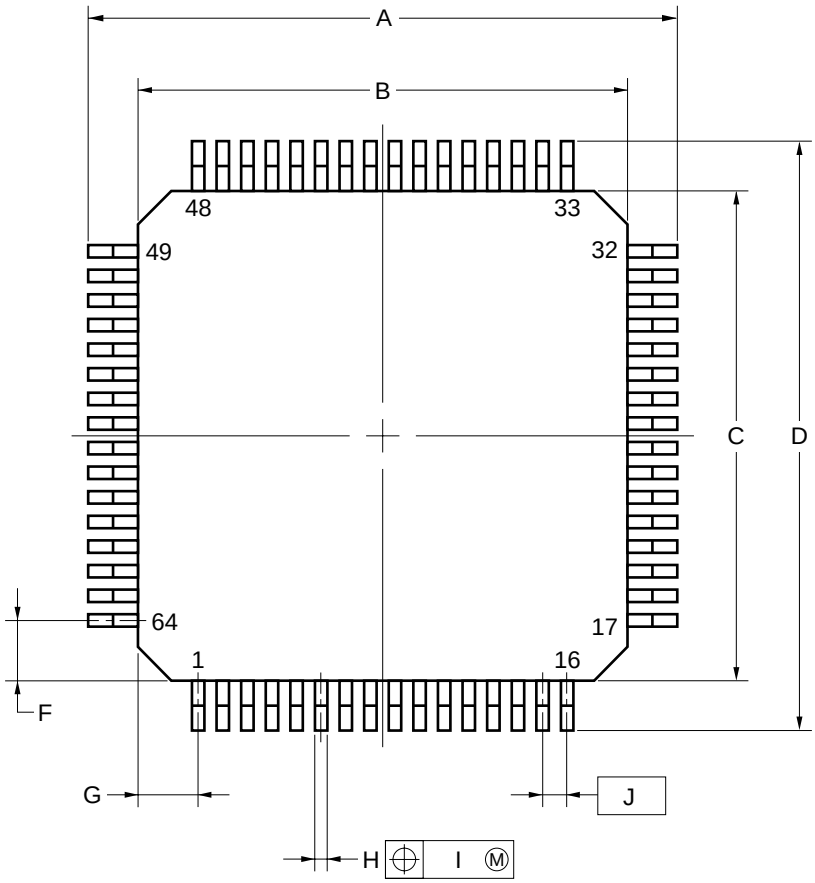
NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

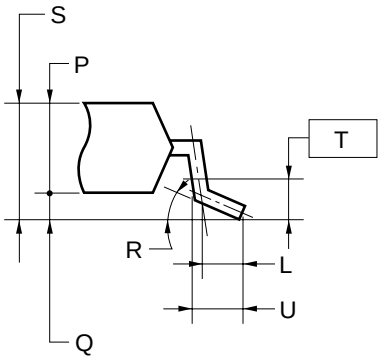
ITEM	MILLIMETERS
A	17.6±0.4
B	14.0±0.2
C	14.0±0.2
D	17.6±0.4
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.15
J	0.8 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	2.55±0.1
Q	0.1±0.1
R	5°±5°
S	2.85 MAX.

P64GC-80-AB8-5

64-PIN PLASTIC TQFP (12x12)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.125
G	1.125
H	$0.32^{+0.06}_{-0.10}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P64GK-65-9ET-2

★ 14. RECOMMENDED SOLDERING CONDITIONS

The μPD789304, 789306, 789314, and μPD789316 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD789304GC-×××-AB8: 64-pin plastic QFP (14 × 14)
μPD789306GC-×××-AB8: 64-pin plastic QFP (14 × 14)
μPD789314GC-×××-AB8: 64-pin plastic QFP (14 × 14)
μPD789316GC-×××-AB8: 64-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering method together (except for partial heating).

μPD789304GK-×××-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)
μPD789306GK-×××-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)
μPD789314GK-×××-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)
μPD789316GK-×××-9ET: 64-pin plastic TQFP (fine pitch) (12 × 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max. Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering method together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD789304, 789306, 789314, and 789316.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
★ DF789306[Notes 1, 2, 3]	Device file for μPD789306, 789316 Subseries
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64GC[Note 4]	Flash memory writing adapter for 64-pin plastic QFP (GC-AB8 type)
FA-64GK[Note 4]	Flash memory writing adapter for 64-pin plastic TQFP (fine pitch) (GK-9ET type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	This is an in-circuit emulator for debugging hardware and software of application system using the 78K/0S Series. It supports the integrated debugger (ID78K0S-NS). It is used with an AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-70000-MC-PS-B AC adapter	This is the adapter for supplying power from an AC-100 to 240 V outlet.
IE-70000-98-IF-C Interface adapter	This adapter is needed when PC-9800 series PC (except notebook type) is used as the host machine for an IE-78K0S-NS (supports C bus).
IE-70000-CD-IF-A PC card interface	This PC card and interface cable are needed when a PC-9800 series notebook-type PC is used as the host machine for an IE-78K0S-NS (supports PCMCIA socket).
IE-70000-PC-IF-C Interface adapter	This adapter is needed when an IBM PC/AT™ or compatible PC is used as the host machine for an IE-78K0S-NS (supports ISA bus).
★ IE-70000-PCI-IF-A Interface adapter	This adapter is needed when a PC that includes a PCI bus is used as the host machine for an IE-78K0S-NS.
★ IE-789306-NS-EM1 Emulation board	This is an emulation board for emulating the peripheral hardware inherent to the device. It is used with an in-circuit emulator.
NP-64GC[Note 4]	This is a board that is used to connect an in-circuit emulator to the target system. It is for 64-pin plastic QFP (GC-AB8 type).
NP-64GK[Note 4]	This is a board that is used to connect an in-circuit emulator to the target system. It is for 64-pin plastic TQFP (GK-9ET type).
SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
★ DF789306[Notes 1, 2]	Device file for μPD789306, 789316 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on PC-9800 series (Japanese Windows)

2. Based on IBM PC/AT compatible (Japanese/English Windows)

3. Based on HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), or NEWS™ (NEWS-OS™)

4. This product is manufactured by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-44-822-3813).

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789306.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.
μPD789304, 789306, 789314, 789316 Data Sheet	This manual
μPD78F9306, 78F9316 Data Sheet	To be prepared
μPD789306, 789316 Subseries User's Manual	U14800E
78K/0S Series User's Manual Instructions	U11047E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID-78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E
IE-78K0S-NS In-Circuit Emulator		U13549E
IE-789306-NS-EM1 Emulation Board		To be prepared

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.
78K/0S Series OS MX78K0S	Fundamental	U12938E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

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Fax: 02-66 75 42 99

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Tel: 040-2445845
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Fax: 01-3067-5899

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Madrid Office
Madrid, Spain
Tel: 091-504-2787
Fax: 091-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

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