# 12-Bit Rail-to-Rail Micropower DACs in SO-8

## FEATURES

- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- 3V Operation (LTC1453), $I_{CC}$: 250µA Typ
- 5V Operation (LTC1451), $I_{CC}$: 400µA Typ
- 3V to 5V Operation (LTC1452), $I_{CC}$: 225µA Typ
- Built-In Reference: 2.048V (LTC1451)
  1.220V (LTC1453)
- Multiplying Version (LTC1452)
- Power-On Reset
- **SO-8 Package**
- 3-Wire Cascadable Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Low Cost

## APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

## DESCRIPTION

The LTC®1451/LTC1452/LTC1453 are complete single supply, rail-to-rail voltage output 12-bit digital-to-analog converters (DACs) in an SO-8 package. They include an output buffer amplifier and an easy-to-use 3-wire cascadable serial interface.

The LTC1451 has an onboard reference of 2.048V and a full-scale output of 4.095V. It operates from a single 4.5V to 5.5V supply.

The LTC1452 is a multiplying DAC with a full-scale output of twice the reference input voltage. It operates from a single supply of 2.7V to 5.5V.

The LTC1453 has an onboard 1.22V reference and a full-scale output of 2.5V. It operates from a single supply of 2.7V to 5.5V.

The low power supply current makes the LTC1451 family ideal for battery-powered applications. The space saving 8-pin SO package and operation with no external components provide the smallest 12-bit DAC system available.
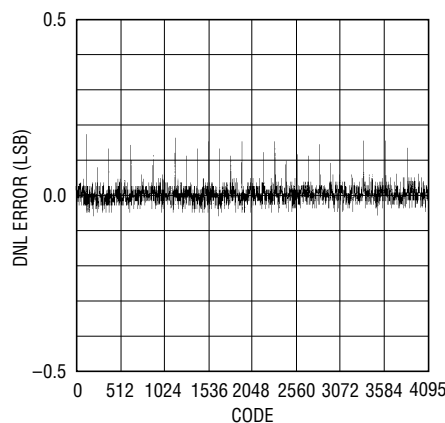
## TYPICAL APPLICATION

**Daisy-Chained Control Outputs**
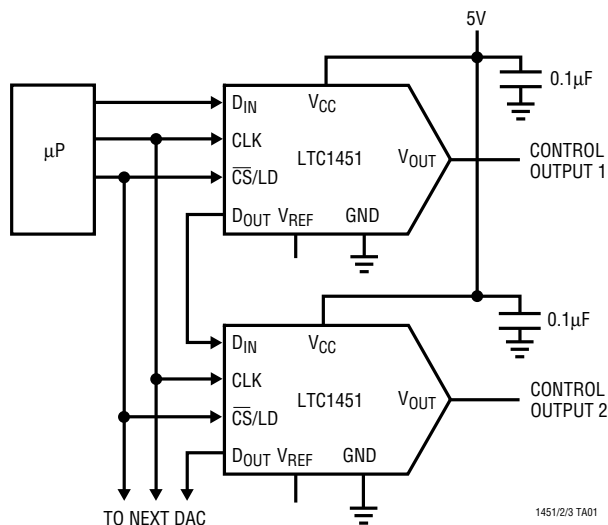


1451/2/3 TA01

**Differential Nonlinearity vs Input Code**



1451/2/3 TA02
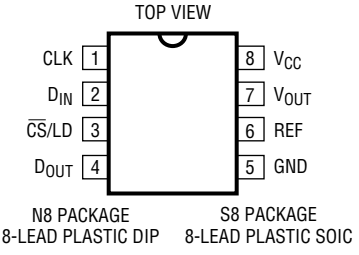
# ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND ............................................. −0.5V to 7.5V
TTL Input Voltage ................................. −0.5V to 7.5V
$V_{OUT}$ ............................................ −0.5V to $V_{CC}$ + 0.5V
REF ............................................... −0.5V to $V_{CC}$ + 0.5V
Maximum Junction Temperature ......... −65°C to 125°C

Operating Temperature Range
    Commercial ......................................... 0°C to 70°C
    Industrial ...................................... −40°C to 85°C
Storage Temperature Range ............... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ................ 300°C

# PACKAGE/ORDER INFORMATION

TOP VIEW

```
CLK     1    8   V_CC
D_IN    2    7   V_OUT
CS/LD   3    6   REF
D_OUT   4    5   GND
```

N8 PACKAGE      S8 PACKAGE
8-LEAD PLASTIC DIP    8-LEAD PLASTIC SOIC

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 100°C/W (N)
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 150°C/W (S)

| ORDER PART NUMBER | | S8 PART MARKING |
|---|---|---|
| LTC1451CN8 | LTC1451CS8 | 1451C |
| LTC1452CN8 | LTC1452CS8 | 1451I |
| LTC1453CN8 | LTC1453CS8 | 1452C |
| LTC1451IN8 | LTC1451IS8 | 1452I |
| LTC1452IN8 | LTC1452IS8 | 1453C |
| LTC1453IN8 | LTC1453IS8 | 1453I |

Consult factory for Military grade parts.

# ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), $V_{OUT}$ and REF unloaded, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DAC** | | | | | | | |
| | Resolution | | ● | 12 | | | Bits |
| DNL | Differential Nonlinearity | Guaranteed Monotonic (Note 1) | ● | | | ±0.5 | LSB |
| INL | Integral Nonlinearity | $T_A$ = 25°C | | | | ±3.5 | LSB |
| | | (Note 1) | ● | | | ±4 | LSB |
| $V_{OS}$ | Offset Error | $T_A$ = 25°C | | | | ±12 | mV |
| | | | ● | | | ±18 | mV |
| $V_{OS}$TC | Offset Error Temperature Coefficient | | | | ±15 | | μV/°C |
| $V_{FS}$ | Full-Scale Voltage | When Using Internal Reference, LTC1451, $T_A$ = 25°C | | 4.065 | 4.095 | 4.125 | V |
| | | LTC1451 | ● | 4.045 | 4.095 | 4.145 | V |
| | | External 2.048V Reference, $V_{CC}$ = 5V, LTC1452 | ● | 4.075 | 4.095 | 4.115 | V |
| | | When Using Internal Reference, LTC1453, $T_A$ = 25°C | | 2.470 | 2.500 | 2.530 | V |
| | | LTC1453 | ● | 2.460 | 2.500 | 2.540 | V |
| $V_{FS}$TC | Full-Scale Voltage Temperature Coefficient | When Using Internal Reference, LTC1451 | | | ±0.10 | | LSB/°C |
| | | When Using External 2.048V Reference, LTC1452 | | | ±0.02 | | LSB/°C |
| | | When Using Internal Reference, LTC1453 | | | ±0.10 | | LSB/°C |

LINEAR
TECHNOLOGY

# ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), $V_{OUT}$ and REF unloaded, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Reference (LTC1451/LTC1453)** | | | | | | | |
| | Reference Output Voltage | LTC1451 | ● | 2.008 | 2.048 | 2.088 | V |
| | | LTC1453 | ● | 1.195 | 1.220 | 1.245 | V |
| | Reference Output Temperature Coefficient | | | | ±0.08 | | LSB/°C |
| | Reference Line Regulation | | ● | | 0.7 | ±2 | LSB/V |
| | Reference Load Regulation | $0 \leq I_{OUT} \leq 100\mu A$, LTC1451 | ● | | 0.2 | ±1.5 | LSB |
| | | LTC1453 | ● | | 0.6 | ±3 | LSB |
| | Reference Input Range | $V_{REF} \leq V_{CC} - 1.5V$ | ● | | | $V_{CC}/2$ | V |
| | Reference Input Resistance | | ● | 8 | 14 | 30 | kΩ |
| | Reference Input Capacitance | | | | 15 | | pF |
| | Short-Circuit Current | REF Shorted to GND | ● | | | 80 | mA |
| **Power Supply** | | | | | | | |
| $V_{CC}$ | Positive Supply Voltage | For Specified Performance, LTC1451 | ● | 4.5 | | 5.5 | V |
| | | LTC1452 | ● | 2.7 | | 5.5 | V |
| | | LTC1453 | ● | 2.7 | | 5.5 | V |
| $I_{CC}$ | Supply Current | $4.5V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1451 | ● | 300 | 400 | 620 | μA |
| | | $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1452 | ● | 120 | 225 | 350 | μA |
| | | $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1453 | ● | 150 | 250 | 500 | μA |
| **Op Amp DC Performance** | | | | | | | |
| | Short-Circuit Current Low | $V_{OUT}$ Shorted to GND | ● | | | 100 | mA |
| | Short-Circuit Current High | $V_{OUT}$ Shorted to $V_{CC}$ | ● | | | 120 | mA |
| | Output Impedance to GND | Input Code = 0 | ● | | 40 | 120 | Ω |
| **AC Performance** | | | | | | | |
| | Voltage Output Slew Rate | (Note 2) | ● | 0.5 | 1.0 | | V/μs |
| | Voltage Output Settling Time | (Notes 2, 3) to ±0.5LSB | | | 14 | | μs |
| | Digital Feedthrough | | | | 0.3 | | nV•s |
| | AC Feedthrough | REF = 1kHz, $2V_{P-P}$, LTC1452 | | | −95 | | dB |
| SINAD | Signal-to-Noise + Distortion | REF = 1kHz, $2V_{P-P}$, (Code: All 1s) LTC1452 | | | 85 | | dB |

# LTC1451
# LTC1452/LTC1453

# ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5V (LTC1451 LTC1452), $V_{CC}$ = 3V (LTC1453), $T_A = T_{MIN}$ to $T_{MAX}$

| SYMBOL | PARAMETER | CONDITIONS | | LTC1451/LTC1452 MIN | TYP | MAX | LTC1453 MIN | TYP | MAX | UNITS |
|--------|-----------|------------|---|------|------|------|------|------|------|-------|
| **Digital I/O** | | | | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | | ● | 2.4 | | | 2.0 | | | V |
| $V_{IL}$ | Digital Input Low Voltage | | ● | | | 0.8 | | | 0.6 | V |
| $V_{OH}$ | Digital Output High Voltage | $I_{OUT}$ = –1mA | ● | | | $V_{CC}$ – 1.0 | | | $V_{CC}$ – 0.7 | V |
| $V_{OL}$ | Digital Output Low Voltage | $I_{OUT}$ = 1mA | ● | 0.4 | | | 0.4 | | | V |
| $I_{LEAK}$ | Digital Input Leakage | V = GND to $V_{CC}$ | ● | | | ±10 | | | ±10 | µA |
| $C_{IN}$ | Digital Input Capacitance | Guaranteed by Design Not Subject to Test | ● | | | 10 | | | 10 | pF |
| **Switching** | | | | | | | | | | |
| $t_1$ | $D_{IN}$ Valid to CLK Setup | | ● | | | 40 | | | 60 | ns |
| $t_2$ | $D_{IN}$ Valid to CLK Hold | | ● | | | 0 | | | 0 | ns |
| $t_3$ | CLK High Time | | ● | | | 40 | | | 60 | ns |
| $t_4$ | CLK Low Time | | ● | | | 40 | | | 60 | ns |
| $t_5$ | $\overline{CS}$/LD Pulse Width | | ● | | | 50 | | | 80 | ns |
| $t_6$ | LSB CLK to $\overline{CS}$/LD | | ● | | | 40 | | | 60 | ns |
| $t_7$ | $\overline{CS}$/LD Low to CLK | | ● | | | 20 | | | 30 | ns |
| $t_8$ | $D_{OUT}$ Output Delay | $C_{LOAD}$ = 15pF | ● | | | 150 | | | 220 | ns |
| $t_9$ | CLK Low to $\overline{CS}$/LD Low | | ● | | | 20 | | | 30 | ns |

The ● denotes specifications which apply over the full operating temperature range.

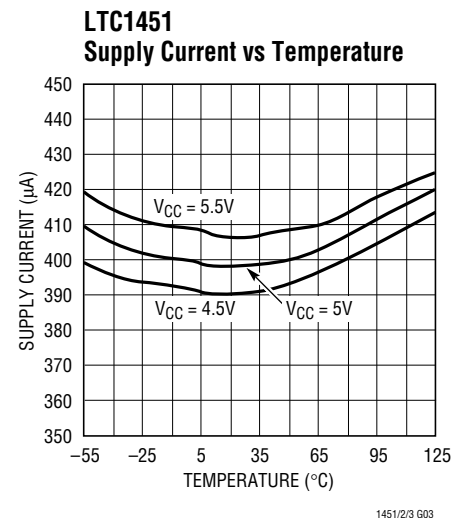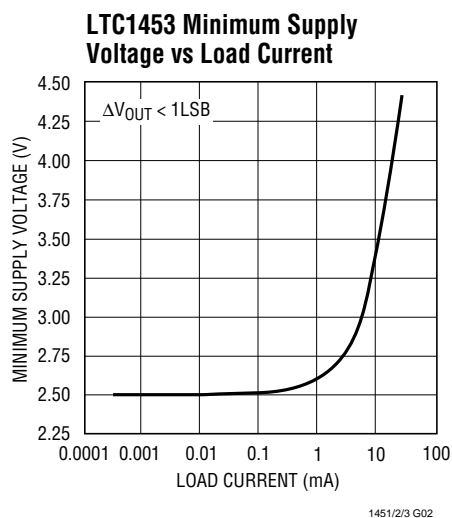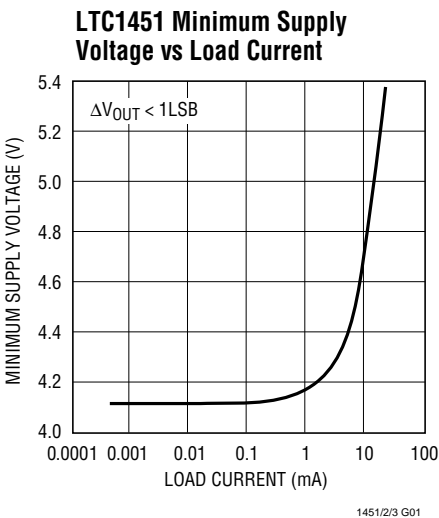**Note 1:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

**Note 2:** Load is 5kΩ in parallel with 100pF.

**Note 3:** DAC switched between all 1s and the code corresponding to $V_{OS}$ for the part, i.e., LTC1451: code 18; LTC1453: code 30.
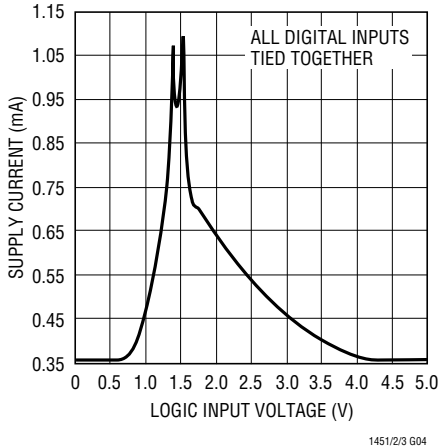
**Note 4:** Digital inputs at 0V or $V_{CC}$.
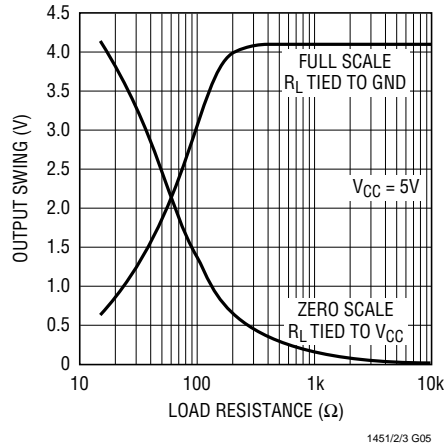
# TYPICAL PERFORMANCE CHARACTERISTICS



**LTC1451 Minimum Supply Voltage vs Load Current**

1451/2/3 G01



**LTC1453 Minimum Supply Voltage vs Load Current**

1451/2/3 G02



**LTC1451 Supply Current vs Temperature**

1451/2/3 G03

# TYPICAL PERFORMANCE CHARACTERISTICS

**LTC1451**
**Supply Current vs Logic Input Voltage**

ALL DIGITAL INPUTS TIED TOGETHER

SUPPLY CURRENT (mA) vs LOGIC INPUT VOLTAGE (V)

1451/2/3 G04

**LTC1451**
**Output Swing vs Load Resistance**

FULL SCALE
R_L TIED TO GND

V_CC = 5V

ZERO SCALE
R_L TIED TO V_CC

OUTPUT SWING (V) vs LOAD RESISTANCE (Ω)

1451/2/3 G05

**LTC1451**
**Pull-Down Voltage vs Output Sink Current Capability**

125°C
25°C
−55°C

OUTPUT PULL-DOWN VOLTAGE (mV) vs OUTPUT SINK CURRENT (mA)

1451/2/3 G06
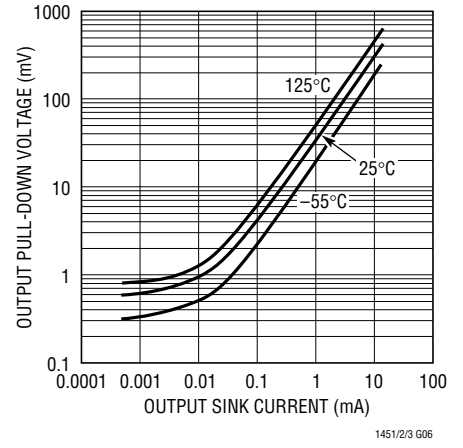
**LTC1451**
**Offset Voltage vs Temperature**

OFFSET VOLTAGE (µV) vs TEMPERATURE (°C)

1451/2/3 G07
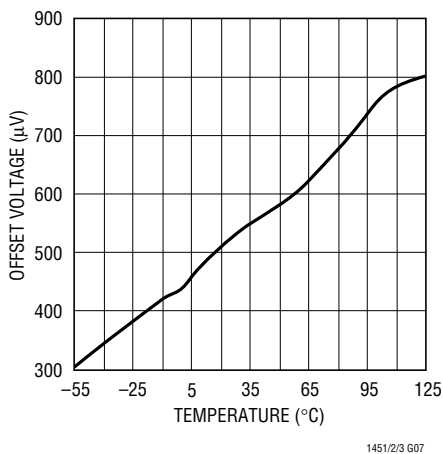
**LTC1451**
**Differential Nonlinearity (DNL)**

DNL ERROR (LSB) vs CODE

1451/2/3 TA02
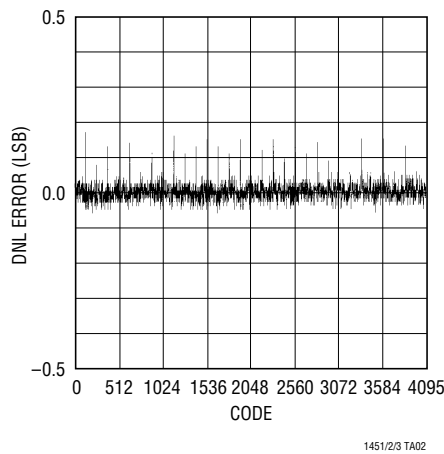
**LTC1451**
**Integral Nonlinearity (INL)**

V_CC = 5V
INTERNAL REFERENCE
T_A = 25°C

ERROR (LSB) vs CODE

1451/2/3 G09
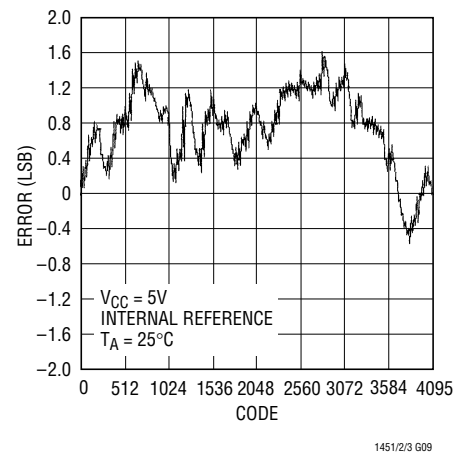
**LTC1452**
**Total Harmonic Distortion + Noise vs Frequency**

V_CC = 5V
V_IN = 2V_P-P
V_OUT = 4V_P-P

TOTAL HARMONIC DISTORTION + NOISE (dB) vs FREQUENCY (Hz)

1451/2/3 G08
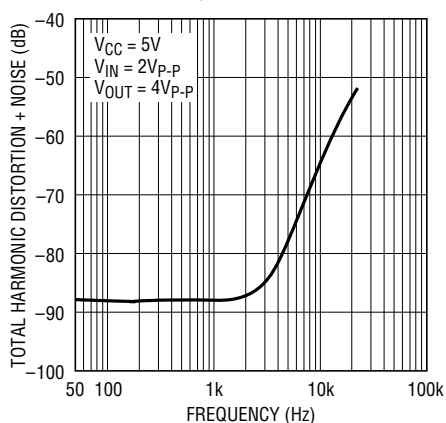
**LTC1451**
**Broadband Output Noise**

0.2LSB/DIV

200mV          2ms

5ms/DIV

CODE = FFFH
BW = 3Hz TO 1.4MHz
GAIN = 1000

1451/2/3 G10
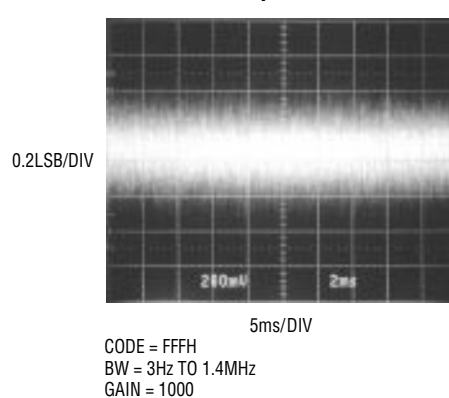
# PIN FUNCTIONS

**CLK:** The TTL Level Input for the Serial Interface Clock.

**$D_{IN}$:** The TTL Level Input for the Serial Interface Data. Data on the $D_{IN}$ pin is latched into the shift register on the rising edge of the serial clock.

**$\overline{CS}$/LD:** The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the CLK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

**$D_{OUT}$:** The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.
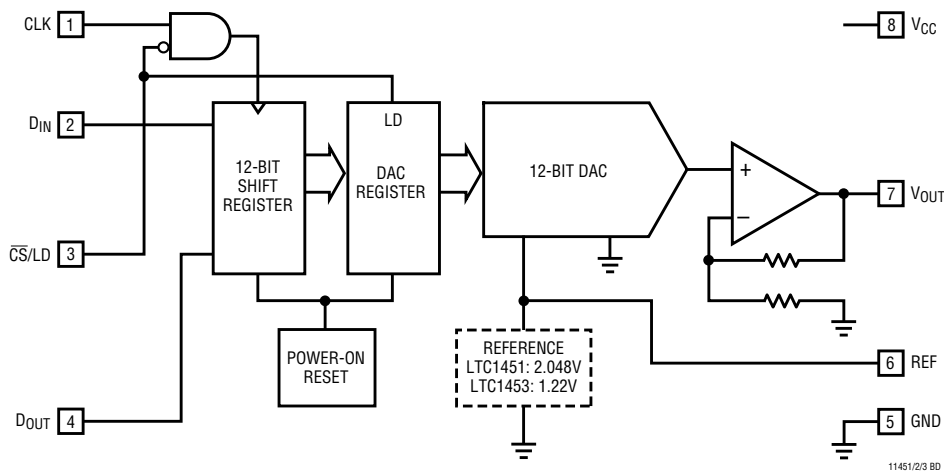
**GND:** Ground.

**REF:** The Output of the Internal Reference and the Input to the DAC Resistor Ladder. An external reference with voltage up to $V_{CC}$/2 may be used for the LTC1452.

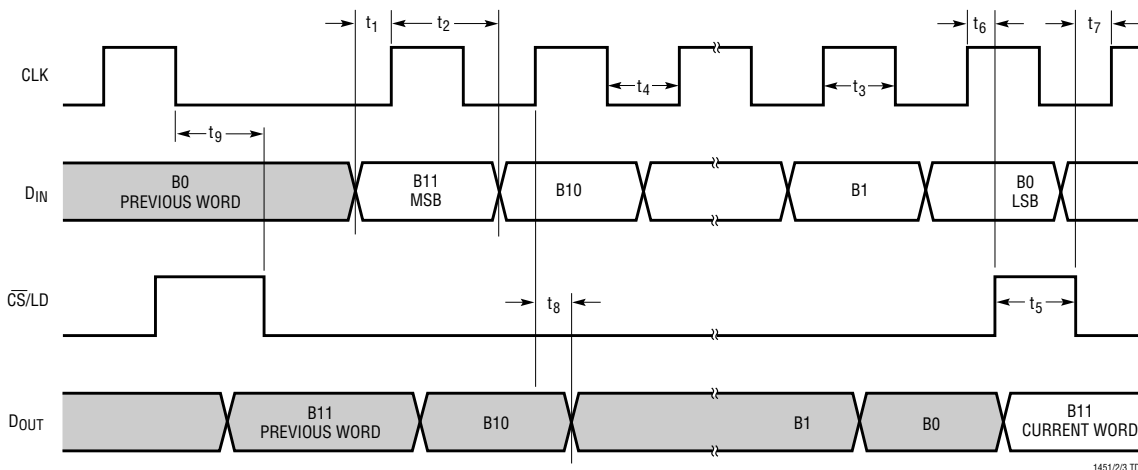**$V_{OUT}$:** The Buffered DAC Output.

**$V_{CC}$:** The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$ (LTC1451), $2.7 \leq V_{CC} \leq 5.5V$ (LTC1452/LTC1453). Requires a bypass capacitor to ground.

# BLOCK DIAGRAM



# TIMING DIAGRAM

# DEFINITIONS

**Resolution (n):** Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states ($2^n$) that divide the full-scale range. The resolution does not imply linearity.

**Full-Scale Voltage ($V_{FS}$):** This is the output of the DAC when all bits are set to 1.

**Voltage Offset Error ($V_{OS}$):** The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code \times V_{FS})/(2^n - 1)]$$

**Least Significant Bit (LSB):** One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

| | |
|---|---|
| LTC1451 | LSB = 4.095V/4095 = 1mV |
| LTC1452 | LSB = V(REF)/4095 |
| LTC1453 | LSB = 2.5V/4095 = 0.610mV |

**Integral Nonlinearity (INL):** End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

INL $\quad= [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$
$V_{OUT} =$ The output voltage of the DAC measured at the given input code

**Differential Nonlinearity (DNL):** DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

DNL $\quad= (\Delta V_{OUT} - LSB)/LSB$
$\Delta V_{OUT} =$ The measured voltage difference between two adjacent codes

**Digital Feedthrough:** The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in $nV \times sec$.
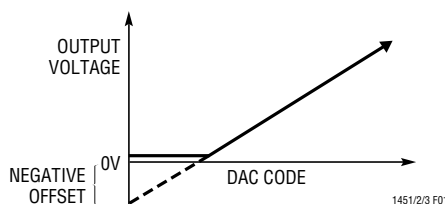


**Figure 1. Effect of Negative Offset**

# OPERATION

### Serial Interface

The data on the $D_{IN}$ input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when $\overline{CS}$/LD is pulled high. The CLK is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

The buffered output of the 12-bit shift register is available on the $D_{OUT}$ pin which swings from GND to $V_{CC}$.

Multiple LTC1451/LTC1452/LTC1453s may be daisy-chained together by connecting the $D_{OUT}$ pin to the $D_{IN}$ pin of the next chip, while the CLK and $\overline{CS}$/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

### Reference

The LTC1451 includes an internal 2.048V reference, making 1LSB equal to 1mV (gain of 2). The LTC1453 has an internal reference of 1.22V with a full scale of 2.5V (gain of 2.05). The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The LTC1452 has no internal reference and the REF pin must be driven externally. The buffer gain is 2, so the external reference must be less than $V_{CC}/2$ and be capable of driving the 8k minimum DAC resistor ladder.

### Voltage Output

The LTC1451 family's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

# TYPICAL APPLICATIONS

**An Isolated 4mA to 20mA Process Controller
Has 3.3V Minimum Loop Voltage**



OPTO-ISOLATORS

11451/2/3 TA04
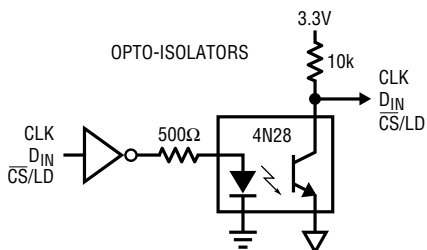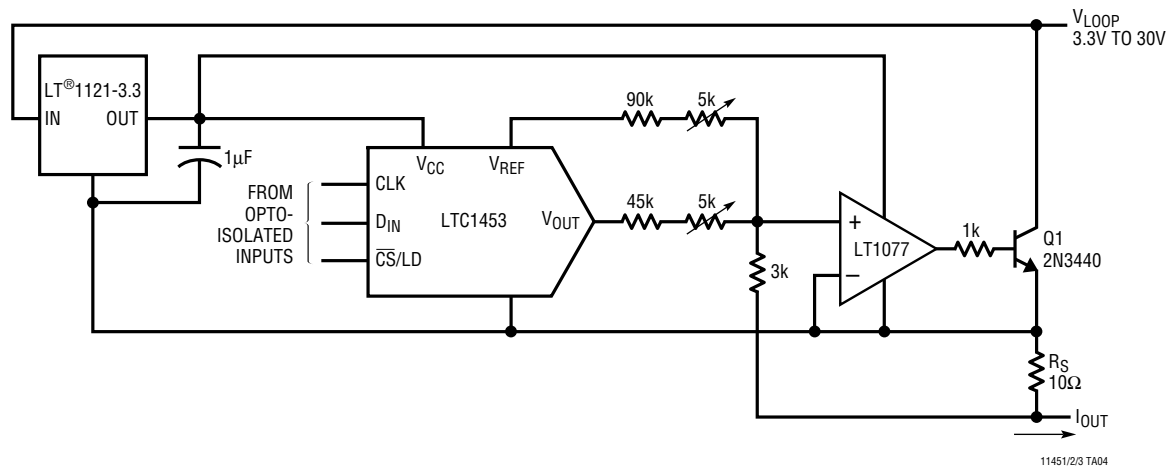
This circuit shows how to use an LTC1453 to make an opto-isolated digitally controlled 4mA to 20mA process controller. The controller circuitry, including the opto-isolation, is powered by the loop voltage that can have a wide range of 3.3V to 30V. The 1.22V reference output of the LTC1453 is used for the 4mA offset current and $V_{OUT}$ is used for the digitally controlled 0mA to 16mA current. $R_S$ is a sense resistor and the op amp modulates the transistor Q1 to provide the 4mA to 20mA current through this resistor. The potentiometers allow for offset and full-scale adjustment. The control circuitry dissipates well under the 4mA budget at zero-scale.

# TYPICAL APPLICATIONS

**12-Bit 3V to 5V Voltage Output DAC**

LTC1451: 4.5V TO 5.5V
LTC1452: 2.7V TO 5.5V
LTC1453: 2.7V TO 5.5V

0.1µF

µP

D<sub>IN</sub>   V<sub>CC</sub>
CLK
$\overline{CS}$/LD        LTC145X    V<sub>OUT</sub>
D<sub>OUT</sub>  V<sub>REF</sub>   GND

OUTPUT
LTC1451: 0V TO 4.095V
LTC1452: 0V TO 2 • REF
LTC1453: 0V TO 2.5V

TO NEXT DAC FOR
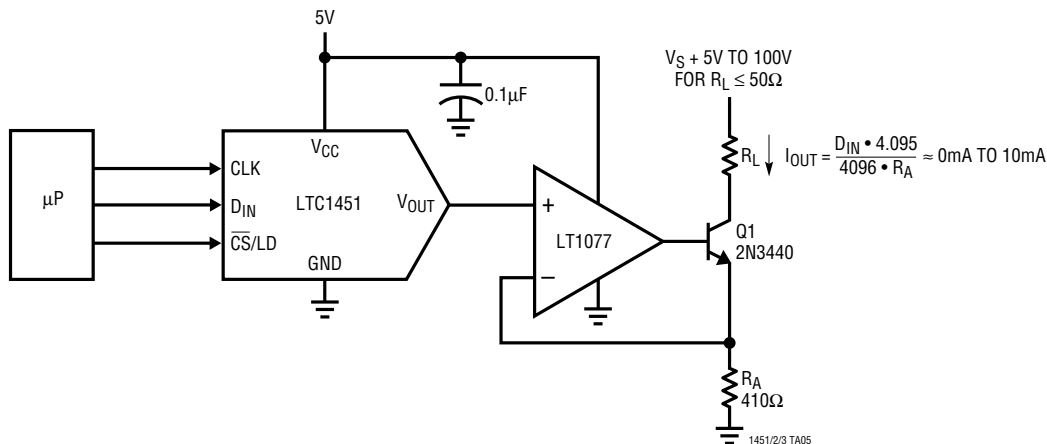DAISY-CHAINING

LTC1451: 2.048V
LTC1452: EXTERNAL
LTC1453: 1.22V

1451/2/3 TA03

**Digitally Programmable Current Source**

5V

0.1µF

V<sub>S</sub> + 5V TO 100V
FOR R<sub>L</sub> ≤ 50Ω

µP

CLK    V<sub>CC</sub>
D<sub>IN</sub>    LTC1451   V<sub>OUT</sub>
$\overline{CS}$/LD    GND

LT1077

R<sub>L</sub>   $I_{OUT} = \dfrac{D_{IN} \cdot 4.095}{4096 \cdot R_A} \approx$ 0mA TO 10mA

Q1
2N3440

R<sub>A</sub>
410Ω

1451/2/3 TA05
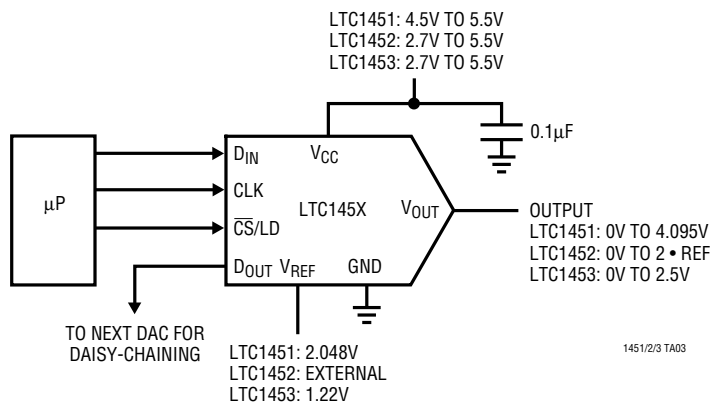
This circuit shows a digitally programmable current source from an external voltage source using an external op amp, an LT1077 and an NPN transistor (2N3440). Any digital word from 0 to 4095 is loaded into the LTC1451 and its output correspondingly swings from 0V to 4.095V. In the configuration shown, this voltage will be forced across the

resistor $R_A$. If $R_A$ is chosen to be 410Ω the output current will range from 0mA at zero-scale to 10mA at full-scale. The minimum voltage for $V_S$ is determined by the load resistor $R_L$ and Q1's $V_{CESAT}$ voltage. With a load resistor of 50Ω, the voltage source can be as low as 5V.

# TYPICAL APPLICATIONS

**A Wide Swing, Bipolar Output 12-Bit DAC**



$$V_{OUT}: \frac{2 \cdot D_{IN} \cdot 4.095}{4096} - 4.096V$$
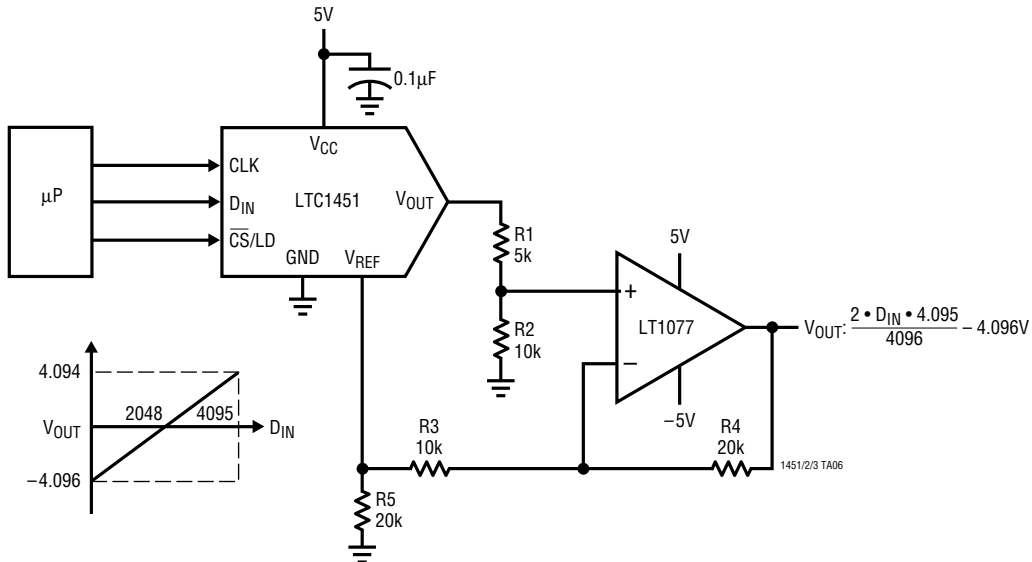
This circuit shows how to make a bipolar output 12-bit DAC with a wide output swing using an LTC1451 and an LT®1077. R1 and R2 resistively divide down the LTC1451 output and an offset is summed in using the LTC1451 onboard 2.048V reference and R3 and R4. R5 ensures that the onboard reference is always sourcing current and never has to sink any current even when $V_{OUT}$ is at full-scale. The LT1077 output will have a wide bipolar output swing of –4.096V to 4.094V as shown in the figure above. With this output swing 1LSB = 2mV.

# PACKAGE DESCRIPTION
**Dimensions in inches (millimeters) unless otherwise noted.**

**N8 Package**
**8-Lead Plastic DIP**

$0.300 - 0.325$
$(7.620 - 8.255)$

$0.009 - 0.015$
$(0.229 - 0.381)$

$0.325 \begin{smallmatrix} +0.025 \\ -0.015 \end{smallmatrix}$
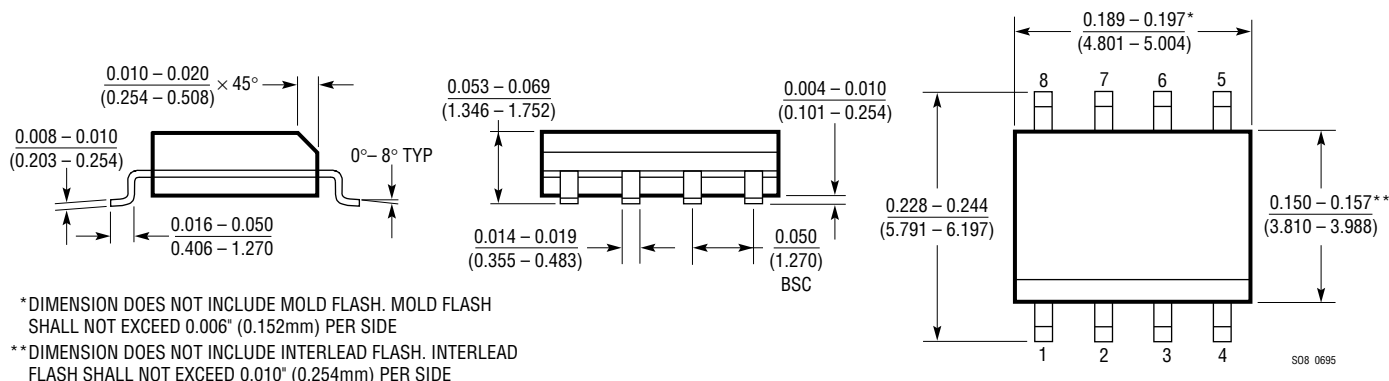$\left( 8.255 \begin{smallmatrix} +0.635 \\ -0.381 \end{smallmatrix} \right)$

$0.045 - 0.065$
$(1.143 - 1.651)$

$0.130 \pm 0.005$
$(3.302 \pm 0.127)$

$0.065$
$(1.651)$
TYP

$0.005$
$(0.127)$
MIN

$0.125$
$(3.175)$
MIN

$0.015$
$(0.380)$
MIN

$0.100 \pm 0.010$
$(2.540 \pm 0.254)$

$0.018 \pm 0.003$
$(0.457 \pm 0.076)$

$0.400*$
$(10.160)$
MAX

$0.255 \pm 0.015*$
$(6.477 \pm 0.381)$

N8 0695
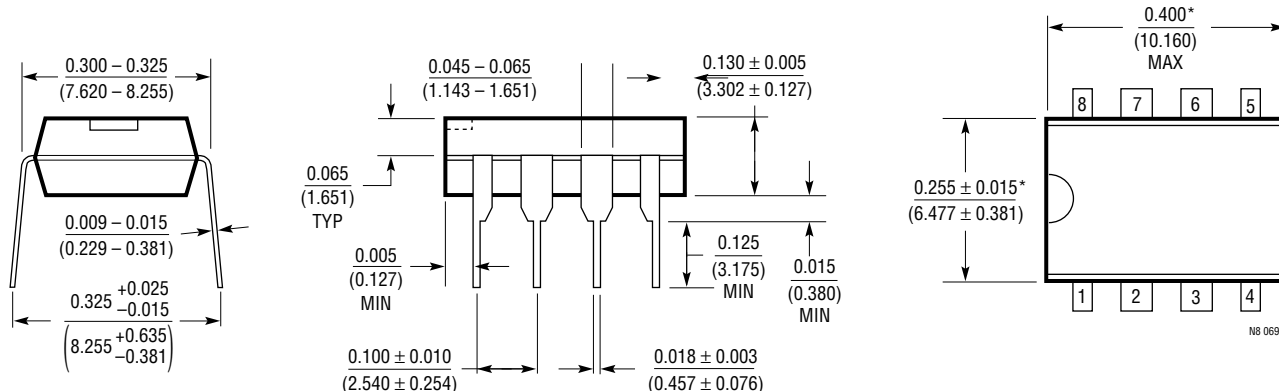
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

**S8 Package**
**8-Lead Plastic SOIC**

$0.010 - 0.020$
$(0.254 - 0.508)$ $\times 45°$

$0.008 - 0.010$
$(0.203 - 0.254)$

$0°- 8°$ TYP

$0.016 - 0.050$
$0.406 - 1.270$

$0.053 - 0.069$
$(1.346 - 1.752)$

$0.004 - 0.010$
$(0.101 - 0.254)$

$0.014 - 0.019$
$(0.355 - 0.483)$

$0.050$
$(1.270)$
BSC

$0.189 - 0.197*$
$(4.801 - 5.004)$

$0.228 - 0.244$
$(5.791 - 6.197)$

$0.150 - 0.157**$
$(3.810 - 3.988)$

SO8 0695

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1257 | Single 12-Bit $V_{OUT}$ DAC, Full Scale: 2.048V, $V_{CC}$: 4.75V to 15.75V. Reference Can Be Overdriven Up to 12V, i.e., FS MAX = 12V | 5V to 15V Single Supply, Complete $V_{OUT}$ DAC in SO-8 Package |
| LTC7541 | 12-Bit Multiplying Parallel $I_{OUT}$ DAC | 5V to 16V Supply, 12-Bit Wide Interface |
| LTC7543/LTC8143 | 12-Bit Multiplying Serial $I_{OUT}$ DAC | 5V Supply, Clear Pin and Serial Data Output (LTC8143) |
| LTC8043 | 12-Bit Multiplying Serial $I_{OUT}$ DAC | 5V Supply, SO-8 Package |

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