Ordering number : EN*5815A

CMOS IC

LC72121, 72121M, 72121V

PLL Frequency Synthesizers for Electronic Tuning

Preliminary

Overview

The LC72121 and the LC72121M and the LC72121V are high input sensitivity (20 mVrms at 130 MHz) PLL frequency synthesizers for 3 V systems. These ICs are serial data (CCB) compatible with the LC72131, and feature the improved input sensitivity and lower spurious radiation (provided by a redesigned ground system) required in high-performance AM/FM tuners.

Functions

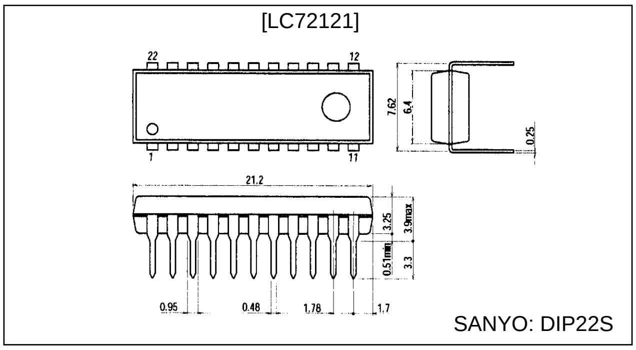
- High-speed programmable divider
  - — FMIN: 10 to 160 MHz ... Pulse swallower technique (With built-in divide-by-2 prescaler)
  - — AMIN: 2 to 40 MHz ... Pulse swallower technique
    0.5 to 10 MHz ... Direct division technique
- IF counter
  - — IFIN: 0.4 to 12 MHz ... For AM and FM IF counting
- Reference frequency
  - — One of 12 reference frequencies can be selected (using a 4.5 or 7.2 MHz crystal element)
    1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 15, 25, 50, or 100 kHz
- Phase comparator
  - — Supports dead zone control.
  - — Built-in unlocked state detection circuit
  - — Built-in deadlock clear circuit
- An MOS transistor for an active low-pass filter is built in.
- I/O ports
  - — Output-only ports: 4 pins
  - — I/O ports: 2 pins
  - — Supports the output of a clock time base signal.
- Operating ranges
  - — Supply voltage: 2.7 to 3.6 V
  - — Operating temperature: – 40 to 85°C
- Package
  - — DIP22S, MFP24S, SSOP24
- Comparison with the LC72131/M
  - — Serial data compatible (CCB)
  - — Identical pin functions
  - — Two V_{SS} pins were added.
  - — The DIP version is pin compatible (V_{SS} pins were inserted as the DIP22S NC pins.)
  - — The MFP product provides a modified pin assignment (The MFP20 package was replaced by an MFP24 package, and extra V_{SS} pins were added.)
  - — The SSOP24 is a newly developed package that has the same pin assignment as the MFP24S product.

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Package Dimensions

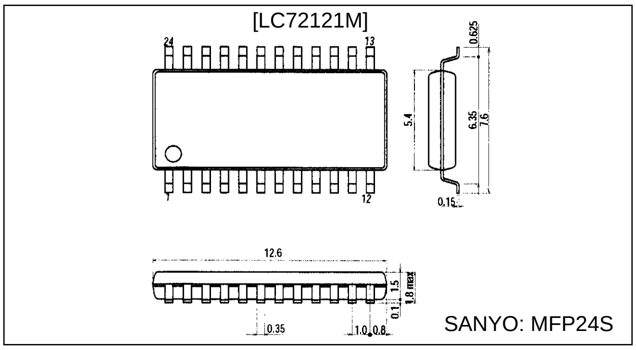
unit: mm

3059-DIP22S



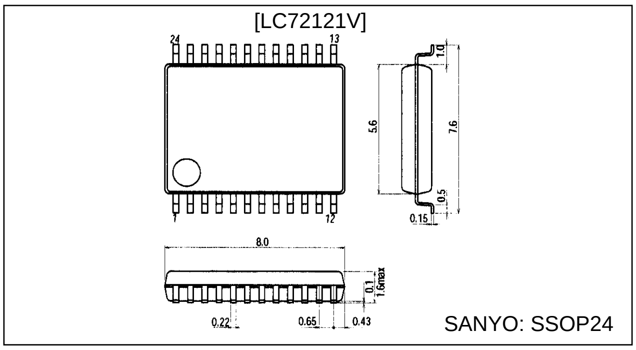
unit: mm

3112-MFP24S

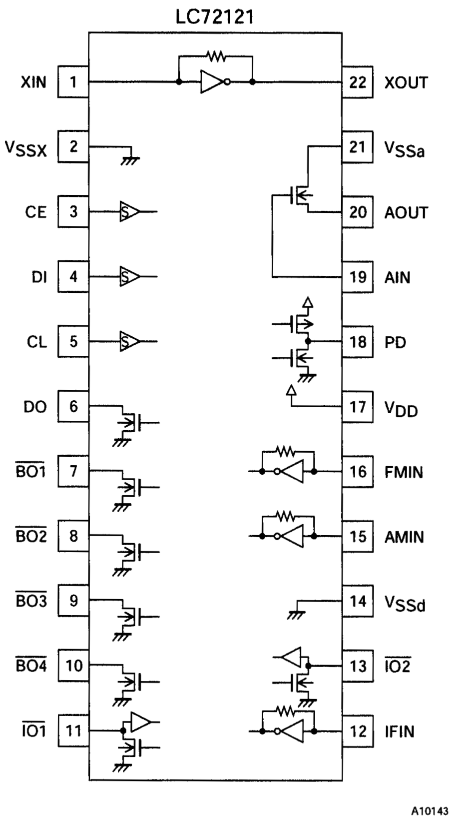


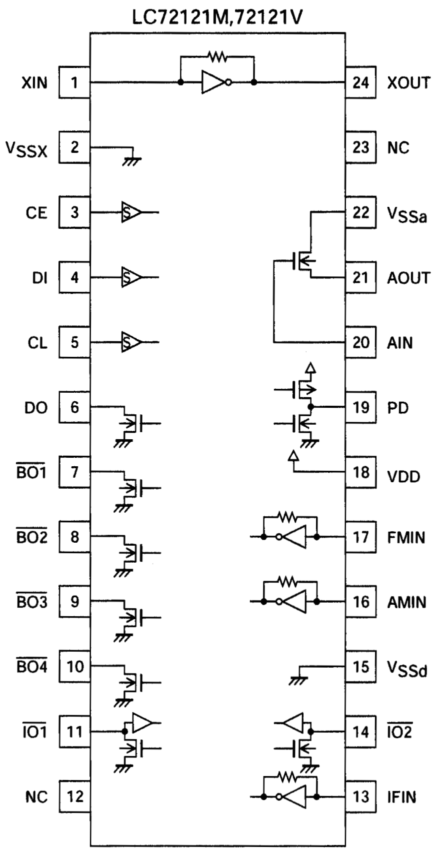
unit: mm

3175A-SSOP24



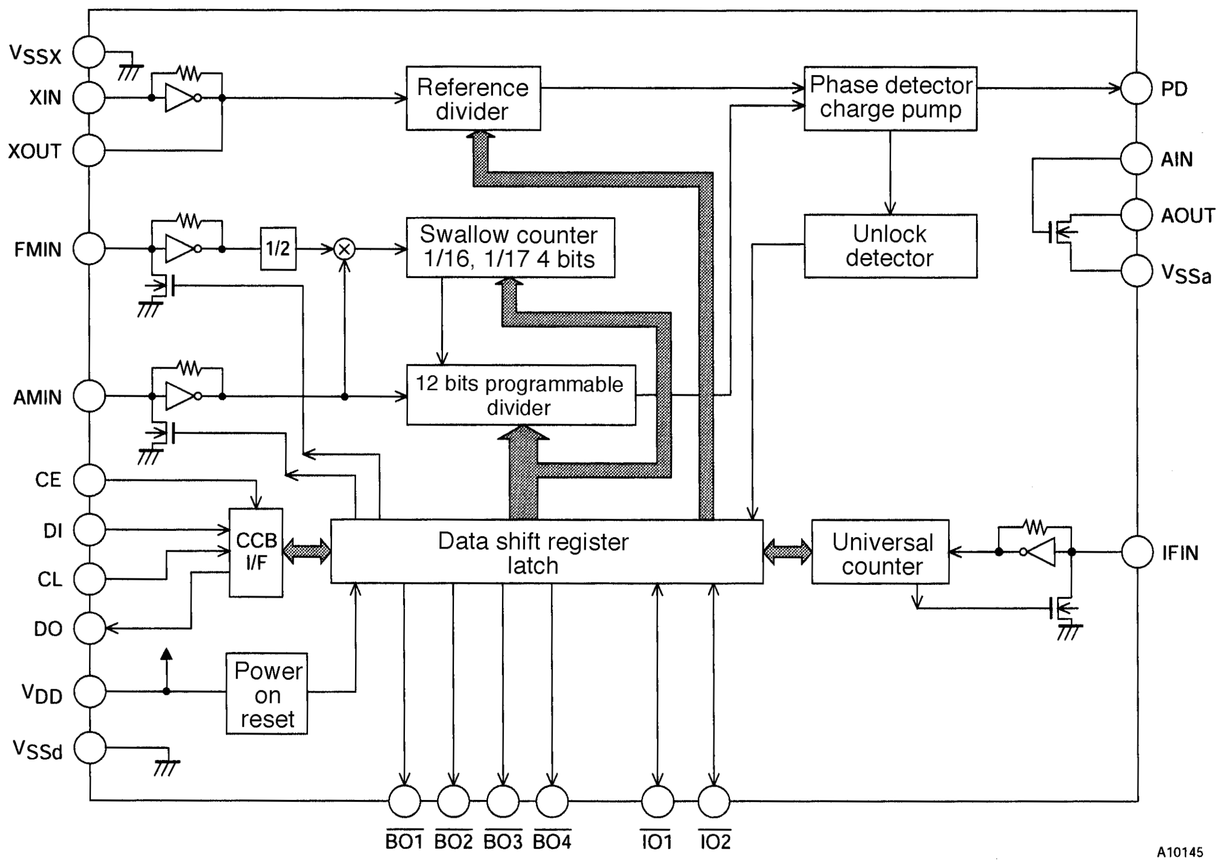
Pin Assignments





Top view

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, $V_{SSd} = V_{SSa} = V_{SSX} = 0$ V

Parameter	Symbol	Conditions		Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}		–0.3 to +7.0	V
Maximum input voltage	$V_{IN}1$ max	CE, DI, CL, AIN		–0.3 to +7.0	V
	$V_{IN}2$ max	XIN, FMIN, AMIN, IFIN		–0.3 to V_{DD} +0.3	V
	$V_{IN}3$ max	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$		–0.3 to +15	V
Maximum output voltage	V_O1 max	DO		–0.3 to +7.0	V
	V_O2 max	XOUT, PD		–0.3 to V_{DD} +0.3	V
	V_O3 max	$\overline{\text{BO1}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$, AOUT		–0.3 to +15	V
Maximum output current	I_O1 max	DO, AOUT		0 to +6.0	mA
	I_O2 max	$\overline{\text{BO1}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$		0 to +10.0	mA
Allowable power dissipation	Pd max	(Ta ≤ 85°C)	DIP22S:	350	mW
			MFP24S:	200	mW
			SSOP24:	150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

Allowable Operating Ranges at Ta = – 40 to +85°C, $V_{SSd} = V_{SSa} = V_{SSX} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		3.6	V
Input high-level voltage	$V_{IH}1$	CE, DI, CL	0.7 V_{DD}		6.5	V
	$V_{IH}2$	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$	0.7 V_{DD}		13	V
Input low-level voltage	V_{IL}	CE, DI, CL, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$	0		0.3 V_{DD}	V
Output voltage	V_O1	DO	0		6.5	V
	V_O2	$\overline{\text{BO1}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$, AOUT	0		13	V
Input frequency	$f_{IN}1$	XIN: $V_{IN}1$	1		8	MHz
	$f_{IN}2$	FMIN: $V_{IN}2$	10		160	MHz
	$f_{IN}3$	AMIN (SNS = 1): $V_{IN}3$	2		40	MHz
	$f_{IN}4$	AMIN (SNS = 0): $V_{IN}4$	0.5		10	MHz
	$f_{IN}5$	IFIN: $V_{IN}5$	0.4		12	MHz
Input amplitude	$V_{IN}1$	XIN: $f_{IN}1$	200		800	mVrms
	$V_{IN}2$-1	FMIN: f = 10 to 130 MHz	20		800	mVrms
	$V_{IN}2$-2	FMIN: f = 130 to 160 MHz	40		800	mVrms
	$V_{IN}3$	AMIN (SNS = 1): $f_{IN}3$	40		800	mVrms
	$V_{IN}4$	AMIN (SNS = 0): $f_{IN}4$	40		800	mVrms
	$V_{IN}5$-1	IFIN: $f_{IN}5$, IFS = 1	40		800	mVrms
	$V_{IN}5$-2	IFIN: $f_{IN}5$, IFS = 0	70		800	mVrms
Guaranteed crystal oscillator frequency	Xtal	XIN, XOUT: *1		4.5		MHz
		XIN, XOUT: *2		7.2		MHz

Notes: 1. Recommended value for CI for the crystal oscillator element: CI < 120Ω
2. Recommended value for CI for the crystal oscillator element: CI < 70Ω

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Internal feedback resistance	Rf1	XIN		1		MΩ
	Rf2	FMIN		500		kΩ
	Rf3	AMIN		500		kΩ
	Rf4	IFIN		250		kΩ
Internal pull-down resistance	Rpd1	FMIN	100	200	400	kΩ
	Rpd2	AMIN	100	200	400	kΩ
Hysteresis	V_{HIS}	CE, DI, CL		0.1 V_{DD}		V
Output high-level voltage	$V_{OH}1$	PD: I_O = –1 mA	V_{DD} – 1.0			V

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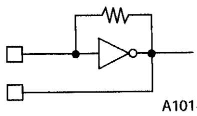
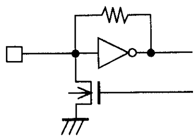
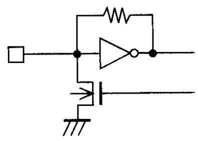
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output low-level voltage	$V_{OL}1$	PD: I_O = 1 mA			1.0	V
	$V_{OL}2$	$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$: I_O = 1 mA			0.2	V
		$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$: I_O = 8 mA			1.6	V
	$V_{OL}3$	DO: I_O = 5 mA			1.0	V
	$V_{OL}4$	AOUT: I_O = 1 mA, AIN = 1.3 V			0.5	V
Input high-level current	$I_{IH}1$	CE, DI, CL: V_I = 6.5 V			5.0	µA
	$I_{IH}2$	$\overline{IO1}$, $\overline{IO2}$: V_I = 13 V			5.0	µA
	$I_{IH}3$	XIN: V_I = V_{DD}	1.3		8	µA
	$I_{IH}4$	FMIN, AMIN: V_I = V_{DD}	2.5		15	µA
	$I_{IH}5$	IFIN: V_I = V_{DD}	5.0		30	µA
	$I_{IH}6$	AIN: V_I = 6.5 V			200	nA
Input low-level current	$I_{IL}1$	CE, DI, CL: V_I = 0 V			5.0	µA
	$I_{IL}2$	$\overline{IO1}$, $\overline{IO2}$: V_I = 0 V			5.0	µA
	$I_{IL}3$	XIN: V_I = 0 V	1.3		8	µA
	$I_{IL}4$	FMIN, AMIN: V_I = 0 V	2.5		15	µA
	$I_{IL}5$	IFIN: V_I = 0 V	5.0		30	µA
	$I_{IL}6$	AIN: V_I = 0 V			200	nA
Output off leakage current	$I_{OFF}1$	$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$, AOUT: V_O = 13 V			5.0	µA
	$I_{OFF}2$	DO: V_O = 6.5 V			5.0	µA
High-level 3-state off leakage current	I_{OFFH}	PD: V_O = V_{DD}		0.01	200	nA
Low-level 3-state off leakage current	I_{OFFL}	PD: V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMIN		6		pF
Supply current	$I_{DD}1$	V_{DD}: Xtal = 7.2 MHz, $f_{IN}2$ = 130 MHz, $V_{IN}2$ = 20 mVrms		2.5	6	mA
	$I_{DD}2$	V_{DD}: PLL block stopped (PLL inhibit mode) Crystal oscillator operating (crystal frequency: 7.2 MHz)		0.3		mA
	$I_{DD}3$	V_{DD}: PLL block stopped, crystal oscillator stopped			10	µA

Pin Descriptions

Pin name	Pin No.		Type	Function	Equivalent circuit
	LC72121	LC72121M LC72121V			
XIN XOUT	1 22	1 24	Xtal	• Crystal oscillator element connections (4.5 or 7.2 MHz)	 A10146
FMIN	16	17	Local oscillator signal input	• FMIN is selected when DVS in the serial data is set to 1. • Input frequency: 10 to 160 MHz • The signal is passed through an internal divide-by-two prescaler and then input to the swallow counter. • The divisor can be set to a value in the range 272 to 65535. Since the internal divide-by-two prescaler is used, the actual divisor will be twice the set value.	 A10147
AMIN	15	16	Local oscillator signal input	• AMIN is selected when DVS in the serial data is set to 0. • When SNS in the serial data is set to 1: • Input frequency: 2 to 40 MHz • The signal is input to the swallow counter directly. • The divisor can be set to a value in the range 272 to 65535. The set value becomes the actual divisor. • When SNS in the serial data is set to 0: • Input frequency: 0.5 to 10 MHz • The signal is input to a 12-bit programmable divider directly. • The divisor can be set to a value in the range 4 to 4095. The set value becomes the actual divisor.	 A10148

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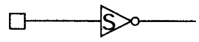
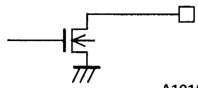
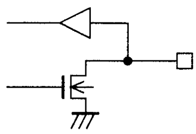
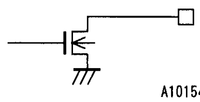
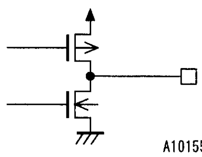
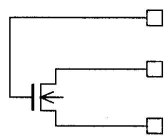
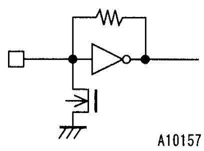
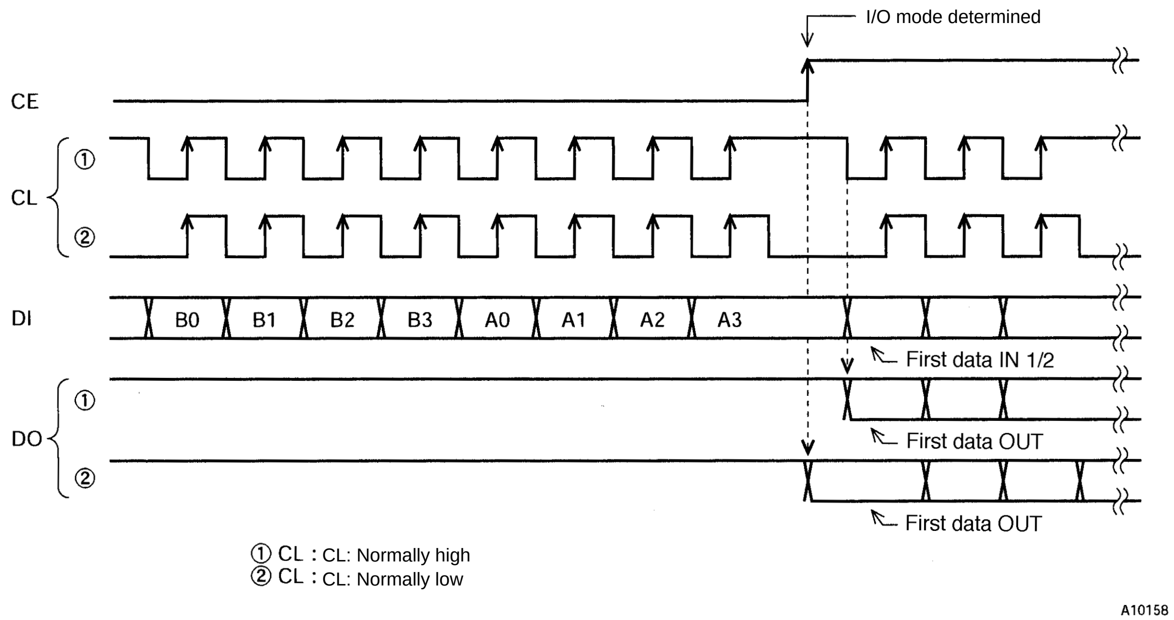
Pin name	Pin No. LC72121	Pin No. LC72121M LC72121V	Type	Function	Equivalent circuit
CE	3	3	Chip enable	• This pin must be set high to enable serial data input (DI) or serial data output (DO).	 A10149
DI	4	4	Input data	• Input for serial data transferred from the controller	 A10150
CL	5	5	Clock	• Clock used for data synchronization for serial data input (DI) and serial data output (DO).	 A10151
DO	6	6	Output data	• Output for serial data transmitted to the controller. The content of the data transmitted is determined by DOC0 through DOC2.	 A10152
V_{DD}	17	18	Power supply	• LC72121 power supply (V_{DD} 2.7 to 3.6 V) • The power on reset circuit operates when power is first applied.	——
V_{SSX}	2	2	Ground	• Ground for the crystal oscillator circuit	——
V_{SSa}	21	22	Ground	• Ground for the low-pass filter MOS transistor	——
V_{SSd}	14	15	Ground	• Ground for the LC72121 digital systems other than those that use V_{SSa} or V_{SSX}.	——
$\overline{IO1}$ $\overline{IO2}$	11 13	11 14	I/O port	• Shared function I/O ports • The pin function is determined by IOC1 and IOC2 in the serial data. When the data value 0: Input port When the data value 1: Output port • When specified to function as an input port: The input pin state is reported to the controller through the DO pin. When the input state is low: The data will be 0: When the input state is high: The data will be 1: • When specified to function as an output port: The output state is determined by IO1 and IO2 in the serial data. When the data value is 0: The output state will be the open circuit state. When the data value is 1: The output state will be a low level. • These pins are set to input mode after a power on reset.	 A10153
$\overline{BO1}$ $\overline{BO2}$ $\overline{BO3}$ $\overline{BO4}$	7 8 9 10	7 8 9 10	Output port	• Output-only ports • The output state is determined by BO1 through BO4 in the serial data. When the data value is 0: The output state will be the open circuit state. When the data value is 1: The output state will be a low level. • A time base signal (8 Hz) is output from $\overline{BO1}$ when TBC in the serial data is set to 1.	 A10154
PD	18	19	Charge pump output	• PLL charge pump output A high level is output when the frequency of the local oscillator signal divided by N is higher than the reference frequency, and a low level is output when that frequency is lower. This pin goes to the high-impedance state when the frequencies match.	 A10155
AIN AOUT	19 20	20 21	Low-pass filter amplifier transistor	• Connections for the MOS transistor used for the PLL active low-pass filter.	 A10156
IFIN	12	13	IF counter	• The input frequency range is 0.4 to 12 MHz • The signal is passed directly to the IF counter. • The result is output, MSB first, through the DO pin. • Four measurement periods are supported: 4, 8, 32, and 64 ms.	 A10157
NC	—	12 23	NC pin	• No connection	——

Procedures for Input and Output of Serial Data

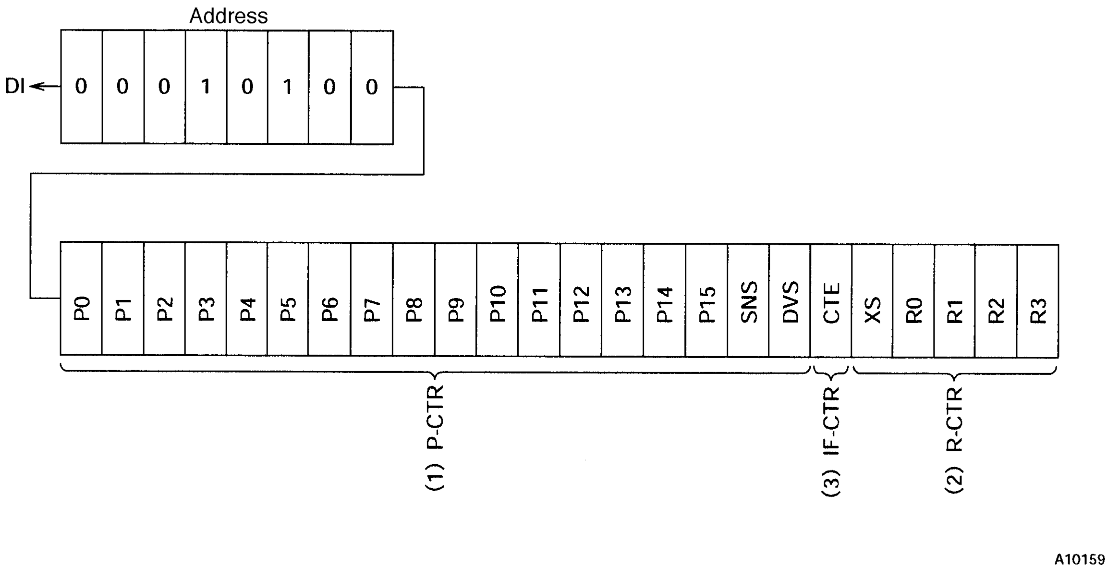
This product uses the CCB (Computer Control Bus), which is Sanyo’s audio product serial bus format, for data input and output. This product adopts an 8-bit address CCB format.

	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (82)	0	0	0	1	0	1	0	0	• Control data input (serial data input) mode • 24 bits of data are input. • See the “DI Control Data (serial data input)” section for details on the content of the input data.
2	IN2 (92)	1	0	0	1	0	1	0	0	• Control data input (serial data input) mode • 24 bits of data are input. • See the “DI Control Data (serial data input)” section for details on the content of the input data.
3	OUT (A2)	0	1	0	1	0	1	0	0	• Data output (serial data output) mode • The number of bits output is equal to the number of clock cycles. • See the “DO Control Data (serial data output)” section for details on the content of the output data.

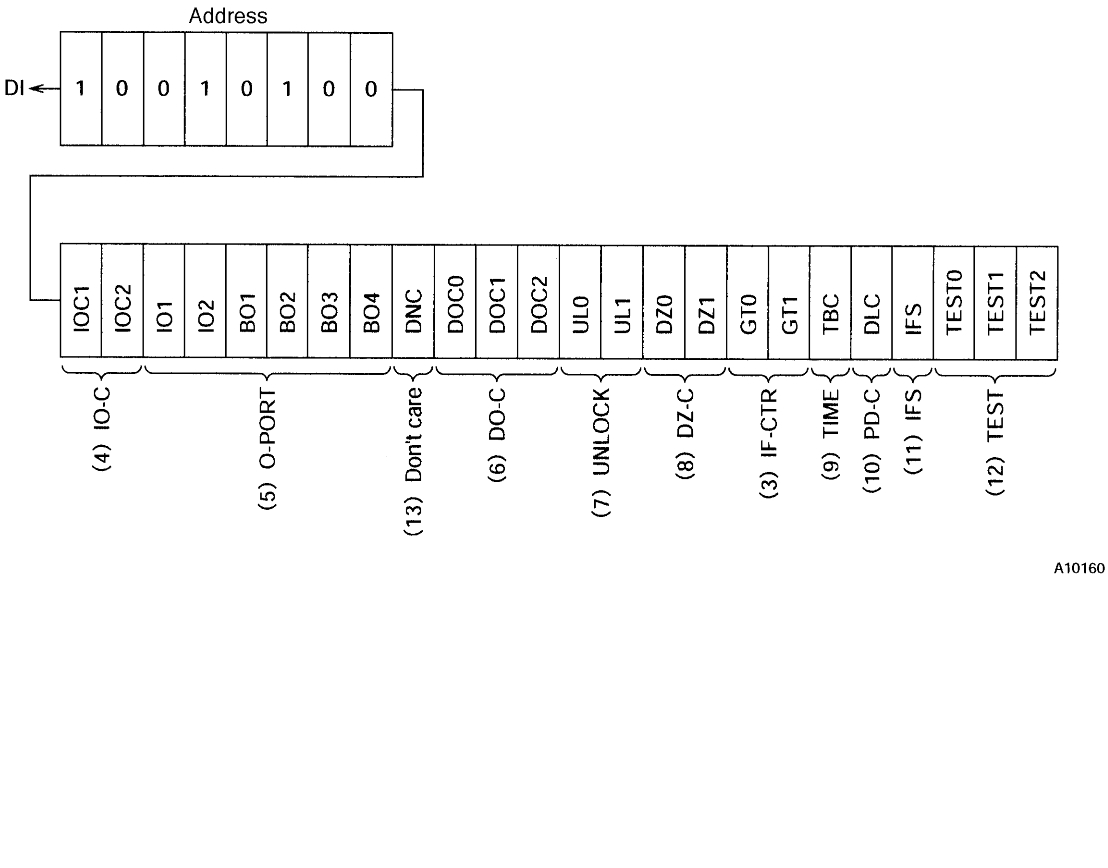


Structure of the DI Control Data (serial data input)

• IN1 mode



• IN2 mode



DI Control Data

<table>
<tr><th>No.</th><th>Control block/data</th><th>Function</th><th>Related data</th></tr>
<tr><td>1</td><td>Programmable divider data
P0 to P15
DVS, SNS</td><td>
• Specifies the divisor for the programmable divider.
This is a binary value in which P15 is the MSB. The LSB changes depending on DVS and SNS.
(* : don’t care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Set divisor (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The set value</td></tr>
</table>
* LSB: When P4 is the LSB, P0 to P3 are ignored.
• These pins select the signal input to the programmable divider (FMIN or AMIN) and switch the input frequency range.
(* : don’t care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Frequency range accepted by the input pin</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160 MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr>
</table>
* See the “Structure of the Programmable Divider” section for details.
</td><td></td></tr>
<tr><td>2</td><td>Reference divider data
R0 to R3
XS</td><td>
• Reference frequency selection
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + Xtal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT mode
In this mode, the programmable divider and the IF counter block are stopped, the FMIN, AMIN, and IFIN pins are pulled down to ground, and the charge pump output goes to the high-impedance state.
• Crystal oscillator element selection data
XS = 0: 4.5 MHz
XS = 1: 7.2 MHz
Note that 7.2 MHz is selected after a power on reset.
</td><td></td></tr>
<tr><td>3</td><td>IF counter control data
CTE
GT0, GT1</td><td>
• IF counter measurement start command data
CTE = 1: Starts the counter
CTE = 0: Resets the counter
• Determines the IF counter measurement time.
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td></tr>
</table>
* See the “Structure of the IF Counter” section for details.
</td><td>IFS</td></tr>
</table>

Continued on next page.

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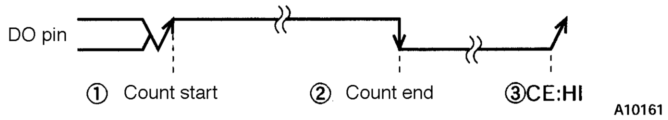
<table>
<tr><th>No.</th><th>Control block/data</th><th>Function</th><th>Related data</th></tr>
<tr><td>4</td><td>I/O port setup data
IOC1,IOC2</td><td>• Specifies input or output for the shared function I/O pins ($\overline{\text{IO1}}$ and $\overline{\text{IO2}}$).
Data = 0: Input port
Data = 1: Output port</td><td></td></tr>
<tr><td>5</td><td>Output port data
BO1 to BO4
IO1,IO2</td><td>• Determines the output state of the $\overline{\text{BO1}}$ through $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, and $\overline{\text{IO2}}$ output ports.
Data = 0: Open
Data = 1: Low level
• The data is reset to 0, setting the pins to the open state, after a power on reset.</td><td>IOC1
IOC2</td></tr>
<tr><td>6</td><td>DO pin control data
DOC0
DOC1
DOC2</td><td>• Determines the DO pin output.
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the PLL is unlocked</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC *1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>The IO1 pin state *2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The IO2 pin state *2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
The open state is selected after a power on reset.
*1. end-UC: IF counter measurement end check


(1)When end-UC is selected and an IF count is started (by switching CTE from 0 to 1), the DO pin automatically goes to the open state.
(2)When the IF counter measurement period completes, the DO pin goes to the low level, allowing applications to test for the completion of the count period.
(3)The DO pin is set to the open state by performing a serial data input or output operation (when the CE pin is set high).
*2. The DO pin will go to the open state if the corresponding IO pin is set up to be an output port.
Note: During the data input period (the period that CE is high in IN1 or IN2 mode), the DO pin goes to the open state regardless of the DO pin control data (DOC0 to DOC2). During the data output period (the period that CE is high in OUT mode) the DO pin state reflects the internal DO serial data in synchronization with the CL clock, regardless of the DO pin control data (DOC0 to DOC2).</td><td>UL0, UL1
CTE

IOC1
IOC2</td></tr>
<tr><td>7</td><td>Unlocked state detection data
UL0, UL1</td><td>• Selects the width of the phase error (øE) detected for PLL lock state discrimination. The state is taken to be unlocked if a phase error in excess of the detection width occurs.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detection output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE is output directly</td></tr>
<tr><td>1</td><td>0</td><td>±0.55 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
<tr><td>1</td><td>1</td><td>±1.11 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
</table>
* When the PLL is unlocked, the DO pin goes low and UL in the serial data output is set to 0.</td><td>DOC0
DOC1
DOC2</td></tr>
<tr><td>8</td><td>Phase comparator control data
DZ0, DZ1</td><td>• Controls the phase comparator dead zone
<table>
<tr><th>DZ1</th><th>DZ</th><th>Dead zone mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Dead zone width: DZA < DZB < DZC < DZD</td><td></td></tr>
</table>

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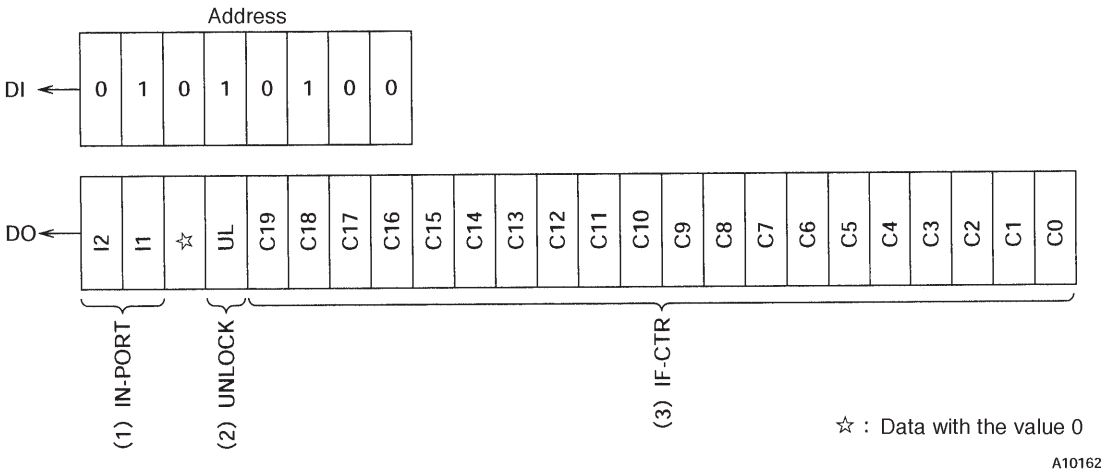
No.	Control block/data	Function	Related data
9	Clock time base TBC	• Setting the TBC bit to 1 causes an 8-Hz clock time base signal with a 40% duty to be output from the BO1 pin. (The BO1 data will be ignored.)	BO1
10	Charge pump control data DLC	• Forcibly controls the charge pump output. DLC / Charge pump output 0 / Normal operation 1 / Forced to low * If the circuit deadlocks due to the VCO control voltage (Vtune) being 0 and the VCO being stopped, applications can get out of the deadlocked state by setting the charge pump output to low and setting Vtune to V_{CC}. (Deadlock clear circuit)	
11	IF counter control data IFS	• This data is normally set to 1. Setting this data to 0 sets the circuit to reduced input sensitivity mode, in which the sensitivity is reduced by about 10 to 30 mV rms. * See the "IF Counter Operation" section for details.	
12	Test data TEST0 to 2	• Test data TEST0, TEST1, TEST2: All these bits must be set to 0. All these bits are set to 0 after a power on reset.	
13	DNC	• This bit must be set to 0.	

Structure of the DO Output Data (serial data output)

• OUT mode

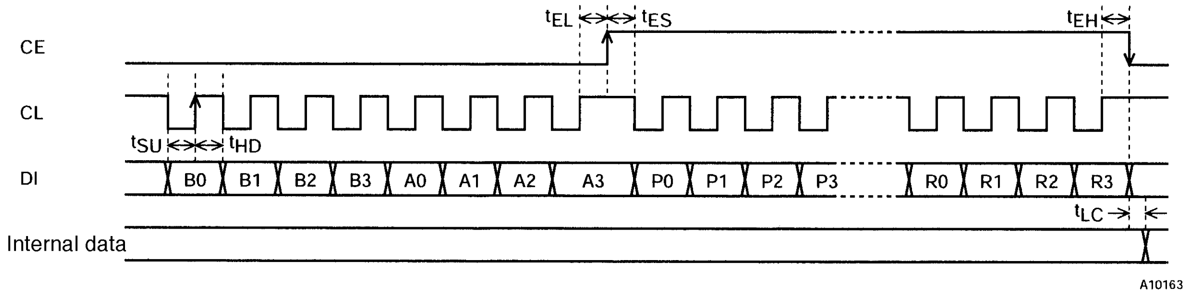


DO Output Data

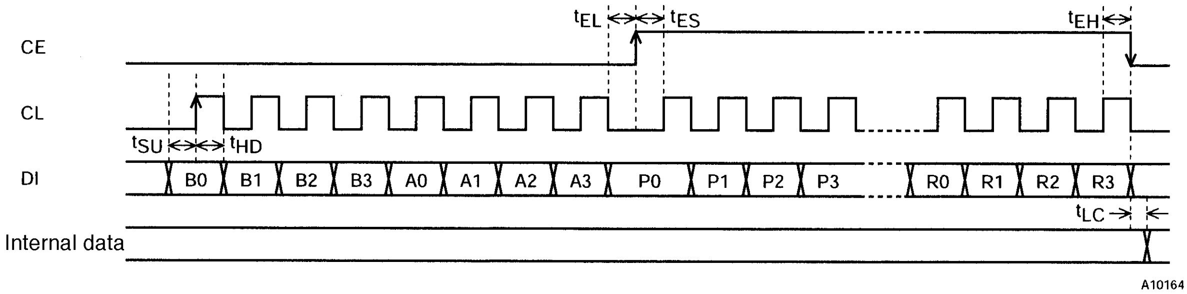
No.	Control block/data	Function	Related data
1	I/O port data I2, I1	• Data latched from the I/O port IO pin states. • These bits reflect the pin states regardless of the I/O port mode (input or output). The data is latched at the point the circuit enters data output mode (OUT mode). I1 ← The $\overline{IO1}$ pin state, I2 ← The $\overline{IO2}$ pin state: H : 1, L : 0	IOC1 IOC2
2	PLL unlocked state data UL	• Indicates the state of the unlocked state detection circuit. UL ← 0: When the PLL is unlocked. UL ← 1: When the PLL is locked or in the detection disabled mode.	UL0 UL1
3	IF counter binary data C19 to C0	• Indicates the value of the IF counter (20-bit binary counter). C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE GT0 GT1

Serial Data Input (IN1/IN2) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} ≥ 0.75 µs t_{LC} < 0.75 µs

- CL: Normal (high)

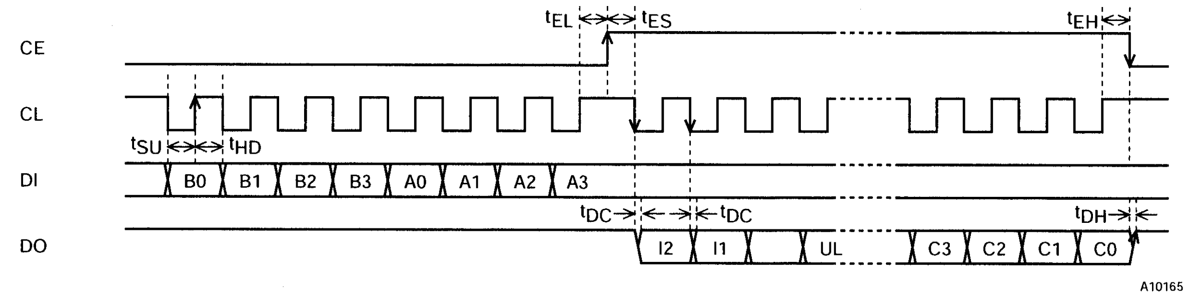


- CL: Normal (low)

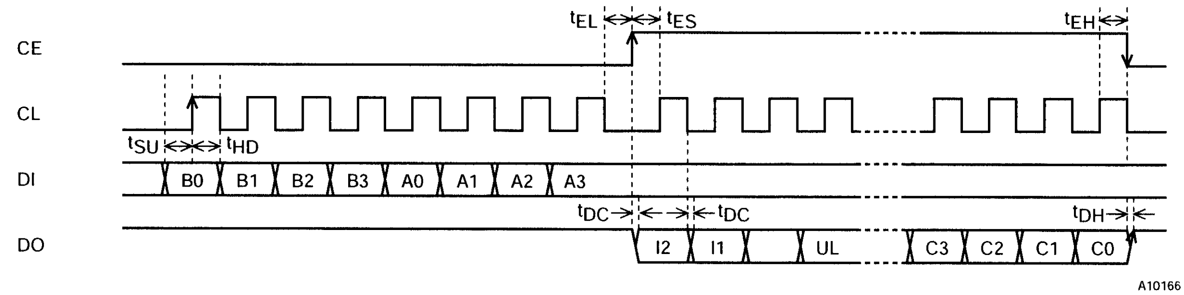


Serial Data Output (Out) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} ≥ 0.75 µs t_{DC}, t_{DH} < 0.35 µs

- CL: Normal (high)

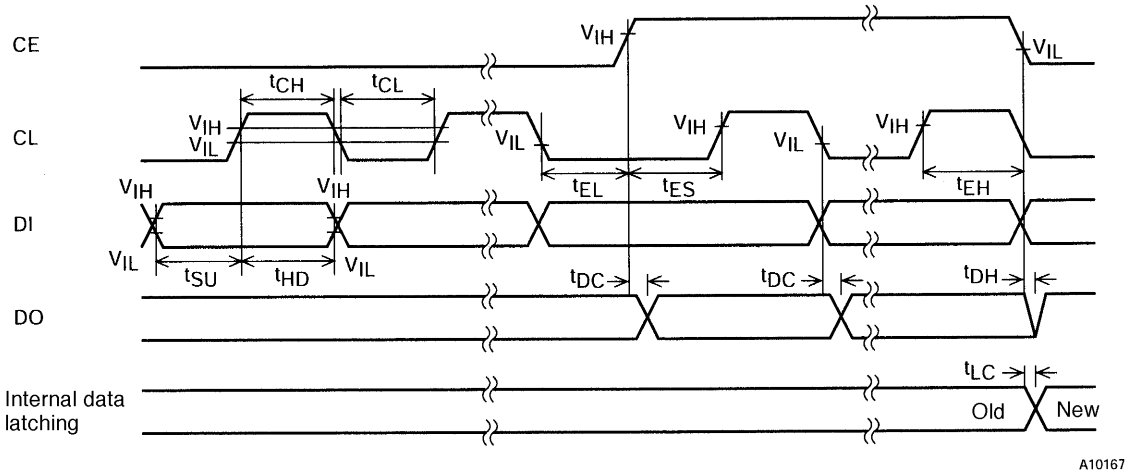


- CL: Normal (low)

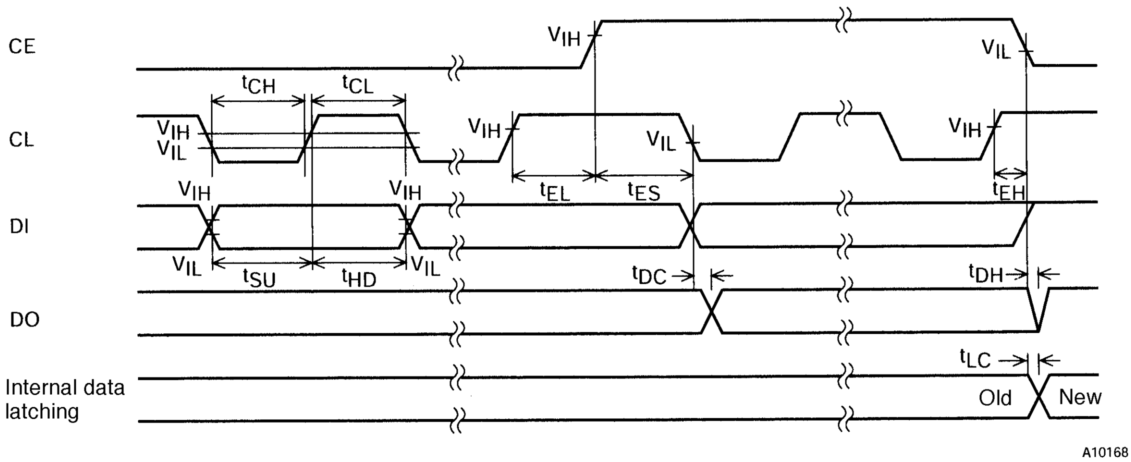


Note: The data conversion times (t_{DC} and t_{DH}) depend on the value of the pull-up resistor and the printed circuit board capacitance since the DO pin is an n-channel open-drain circuit.

Serial Data Timing



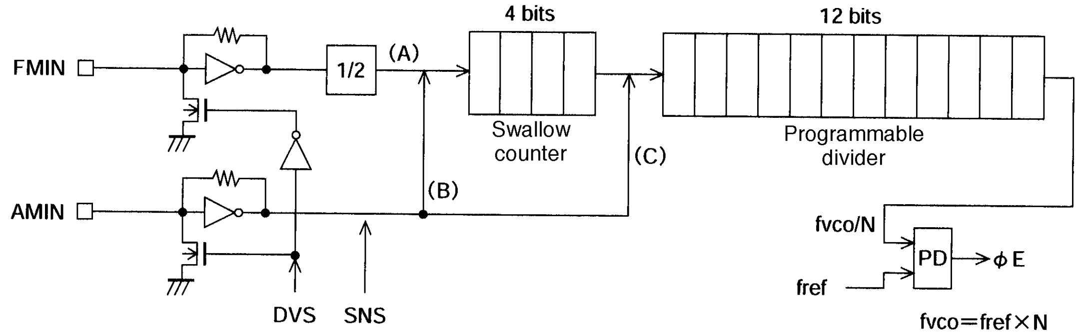
When CL is Stopped at the Low Level



When CL is Stopped at the High Level

Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Data setup time	t_{SU}	DI, CL		0.75			µs
Data hold time	t_{HD}	DI, CL		0.75			µs
Clock low level time	t_{CL}	CL		0.75			µs
Clock high level time	t_{CH}	CL		0.75			µs
CE wait time	t_{EL}	CE, CL		0.75			µs
CE setup time	t_{ES}	CE, CL		0.75			µs
CE hold time	t_{EH}	CE, CL		0.75			µs
Data latch change time	t_{LC}					0.75	µs
Data output time	t_{DC}	DO, CL	These values differ depending on the value of the pull-up resistor used and the printed circuit board capacitance.			0.35	µs
	t_{DH}	DO, CE				0.35	µs

Structure of the Programmable Divider



A10169

	DVS	SNS	Input pin	Set divisor	Actual divisor	Input frequency range
A	1	*	FMIN	272 to 65535	Twice the set value	10 to 160 MHz
B	0	1	AMIN	272 to 65535	The set value	2 to 40 MHz
C	0	0	AMIN	4 to 4095	The set value	0.5 to 10 MHz

*: Don't care

Sample Programmable Divider Divisor Calculations

- For FM with a step size of 50 kHz (DVS = 1, SNS = *: FMIN selected)
  FM RF = 90.0 MHz (IF +10.7 MHz)
  FM VCO = 100.7 MHz
  PLL fref = 25 kHz (R0 = 0, R1 = 1, R2 = 0, R3 = 0)
  100.7 MHz (FM VCO) ÷ 25 kHz (fref) ÷ 2 (for the FMIN 1/2 prescaler) 2014 → 07DE (hexadecimal)

E				D				7				0											
0	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	*	1			0	1	0	0
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A10170

- For SW with a step size of 5 kHz (DVS = 0, SNS = 1: AMIN high-speed operation selected)
  SW RF = 21.75 MHz (IF +450 kHz)
  SW VCO = 22.20 MHz
  PLL fref = 5 kHz (R0 = 0, R1 = 1, R2 = 0, R3 = 1)
  22.2 MHz (SW VCO) ÷ 5 kHz (fref) = 4440 → 1158 (hexadecimal)

8				5				1				1											
0	0	0	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0			0	1	0	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A10171

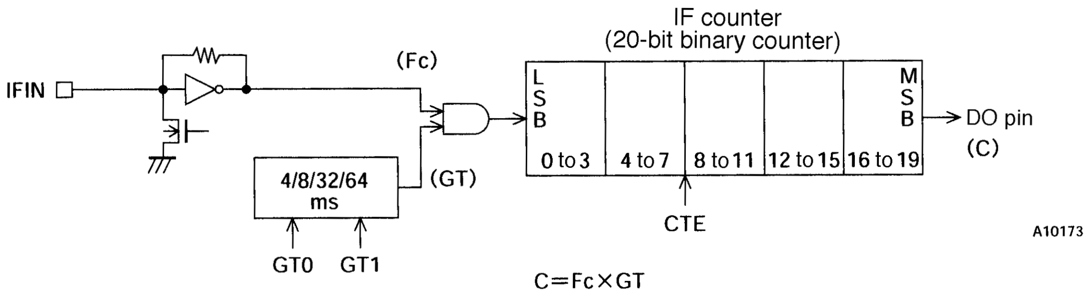
- For MW with a step size of 9 kHz (DVS = 0, SNS = 0: AMIN low-speed operation selected)
  MW RF = 1008 kHz (IF +450 kHz)
  WM VCO = 1458 kHz
  PLL fref =9 kHz (R0 = 1, R1 = 0, R2 = 0, R3 = 1)
  1458 (MW VCO) ÷ 9 kHz (fref) = 162 → 0A2 (hexadecimal)

				2				A				0											
*	*	*	*	0	1	0	0	0	1	0	1	0	0	0	0	0	0			1	0	0	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A10172

Structure of the IF Counter

The LC72121 IF counter is a 20-bit binary counter, and takes the IF signal from the IFIN pin as its input. The result of the count can be read out serially, MSB first, from the DO pin.



GT1	GT0	Measurement time	
		Measurement time (GT)	Wait time (t_{WU})
0	0	4 ms	3 to 4 ms
0	1	8	3 to 4 ms
1	0	32	7 to 8 ms
1	1	64	7 to 8 ms

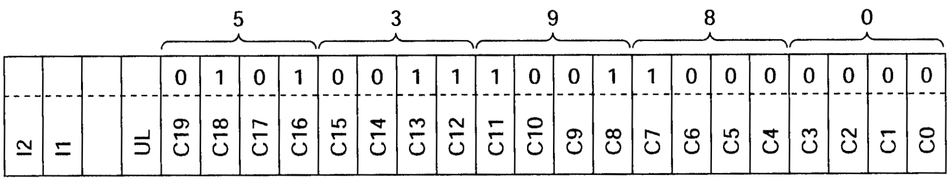
The IF frequency (Fc) is measured by determining how many pulses were input to the IF counter in the stipulated measurement time, GT.

$$Fc = \frac{C}{GT} \quad (C = Fc \times GT)$$

C: Counted value (the number of pulses)

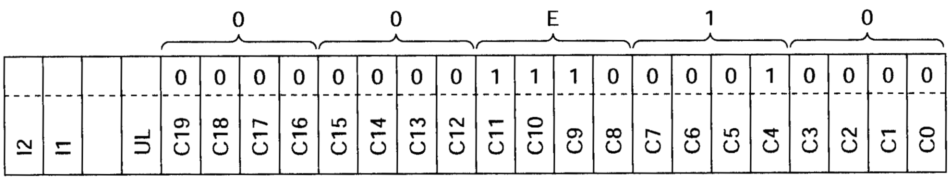
IF Counter Frequency Measurement Examples

- When the measurement time (GT) is 32 ms and the counted value (C) is 53980 (hexadecimal) or 342,400 decimal.
  IF frequency (F_C) = 342400 ÷ 32 ms = 10.7 MHz



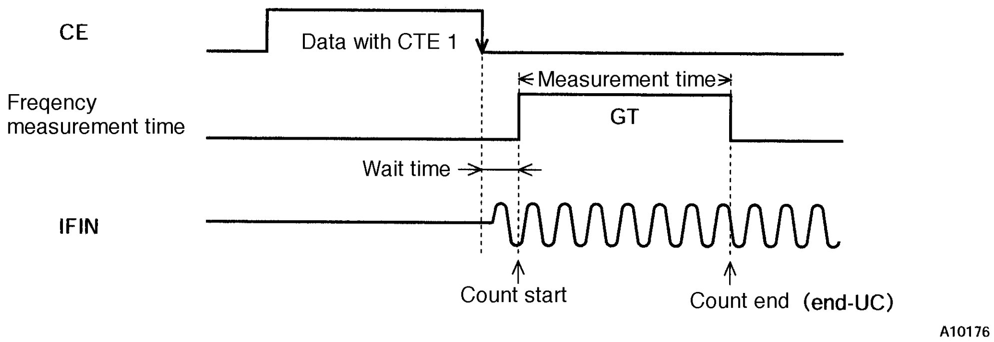
A10174

- When the measurement time (GT) is 8 ms and the counted value (C) is E10 (hexadecimal) or 3600 decimal.
  IF frequency (F_C) = 3600 ÷ 8 ms = 450 kHz



A10175

IF Counter Operation



Applications must first, before starting an IF count operation reset the IF counter by setting CTE in the serial data to 0. The IF counter operation is started setting CTE in the serial data from 0 to 1. Although the serial data is latched by dropping the CE pin from high to low, the IF signal input to the IFIN pin must be provided within the wait time from the point CE goes low. Next, the readout of the IF counter after measurement is complete must be performed while CTE is still 1, since the counter will be reset if CTE is set to 0.

Note: If IF counting is used, applications must determine whether or not the IF IC SD (station detect) signal is present in the microcontroller software, and perform the IF count only if that signal is asserted. This is because auto-search techniques that use IF counting only are subject to incorrect stopping at points where there is no station due to IF buffer leakage.
Note that the LC72121 input sensitivity can be controlled with the IFS bit in the serial data.
Reduced sensitivity mode (IFS = 0) must be selected when this IC is used in conjunction with an IF IC that does not provide an SD output and auto-search is implemented using only IF counting.

IFIN Minimum Sensitivity Standard

Input frequency : f [MHz]

IFS data	0.4 ≤ f < 0.5	0.5 ≤ f < 0.8	8 ≤ f ≤ 12
1(Normal mode)	40 mVrms (0.1 to 3 mVrms)	40 mVrms	40 mVrms (1 to 10 mVrms)
0 (Degraded sensitivity mode)	70 mVrms (10 to 15 mVrms)	70 mVrms	70 Vrms (30 to 40 mVrms)

Note: Values in parentheses are actual performance values that are provided for reference purposes.

Unlocked State Detection Timing

- Unlocked state detection timing

  Unlocked state detection is performed during the reference frequency (fref) period (interval). This means that a period at least as long as the period of the reference frequency is required to recognize the locked/unlocked state. However, applications must wait at least twice the period of the reference frequency immediately after changing the divisor (N) before checking the locked/unlocked state.

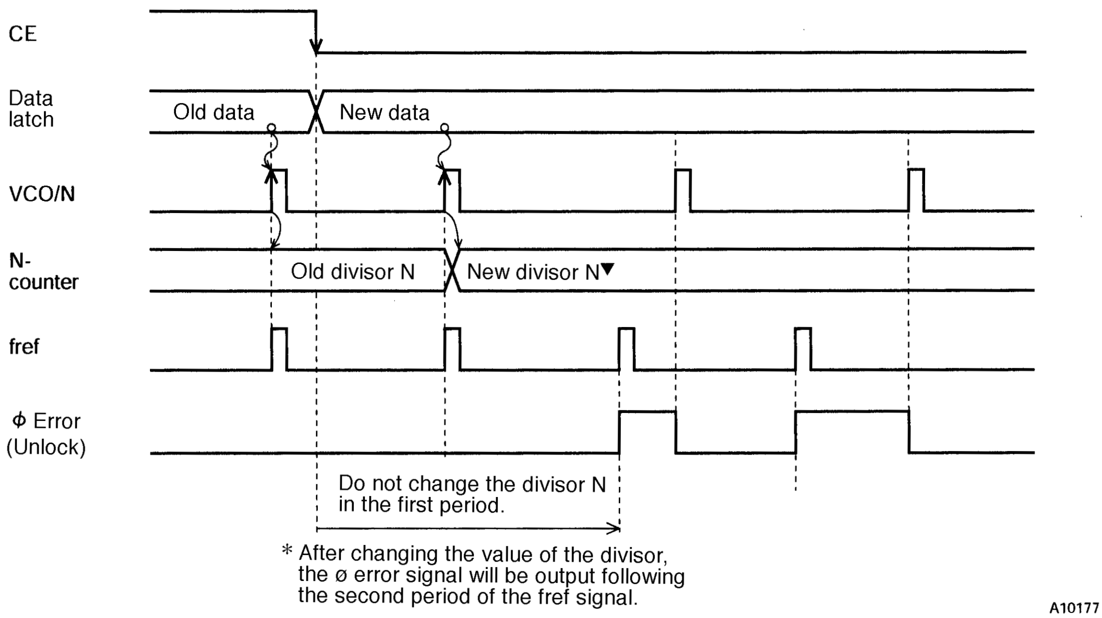


Figure 1 Unlocked State Detection Timing

For example, if fref is 1 kHz (a period of 1 ms) applications must wait at least 2 ms after the divisor N is changed before performing a locked/unlocked check.

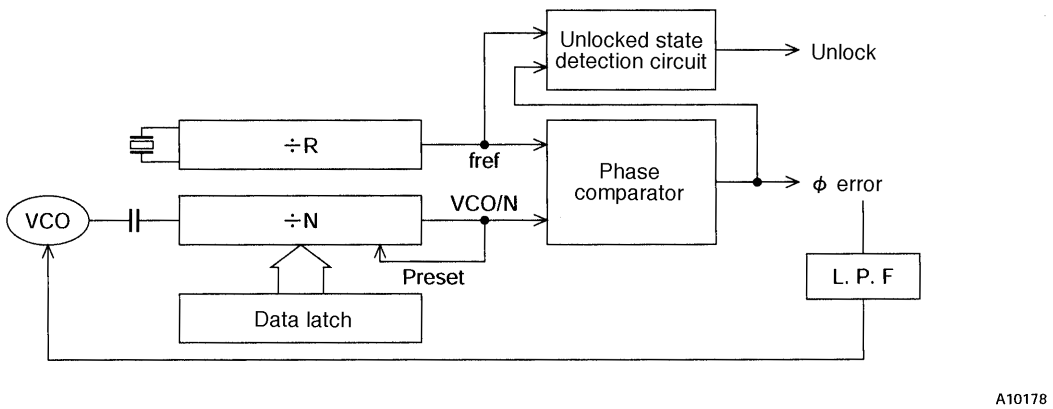


Figure 2 Circuit Structure

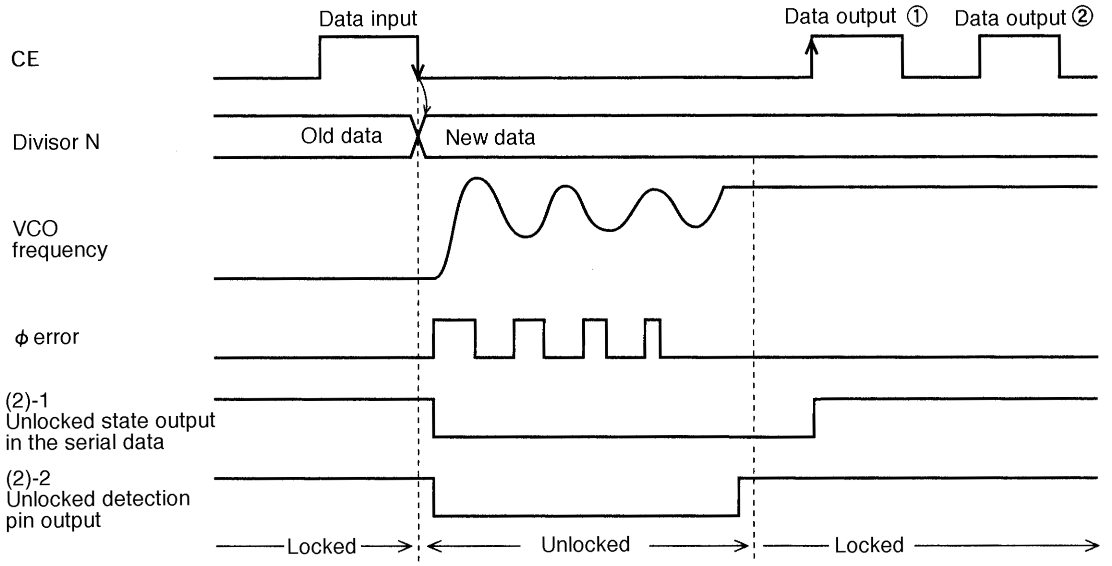
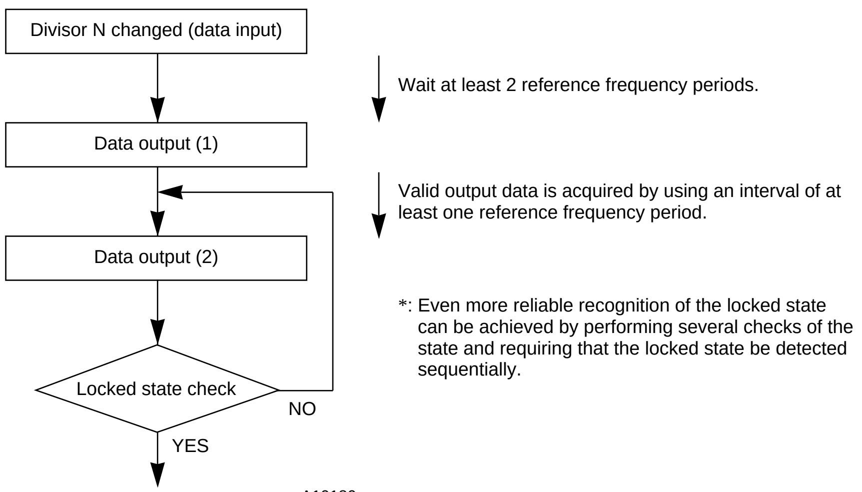


Figure 3 Combining with Software

- Outputting the unlocked state data in the serial data
  At the point of data output 1 in figure 3, the unlocked state data will indicate the unlocked state, since the VCO frequency is not stable (locked) yet. In cases such as this, the application should wait at least one whole period and then check again whether or not the frequency has stabilized with the data output 2 operation in the figure. Applications can implement even more reliable recognition of the locked state by performing several more checks of the state and requiring that the locked state be detected sequentially.

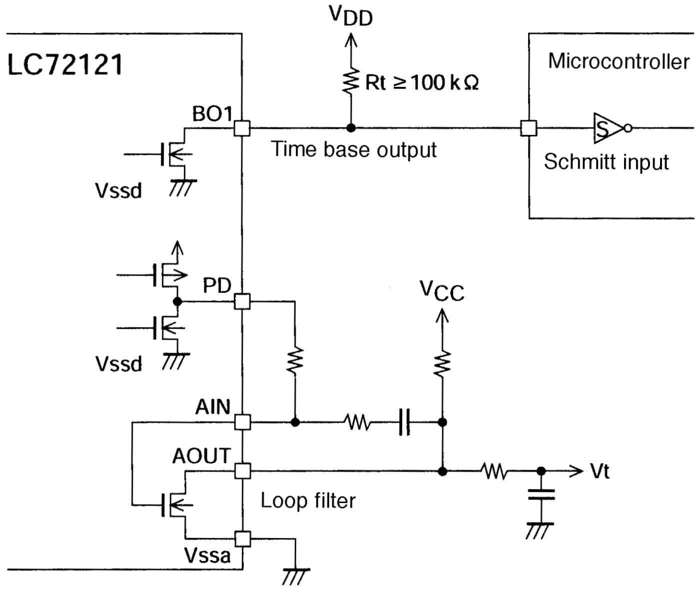
<Flowchart for Lock Detection>



- Directly outputting the unlocked state to the DO pin
  Since the unlocked state (high level when locked, low when unlocked) is output from the DO pin, applications can check for the locked state by waiting at least two reference frequency periods after changing the divisor N. However, in this case also, even more reliable recognition of the locked state can be achieved by performing several checks of the state and requiring that the locked state be detected sequentially.

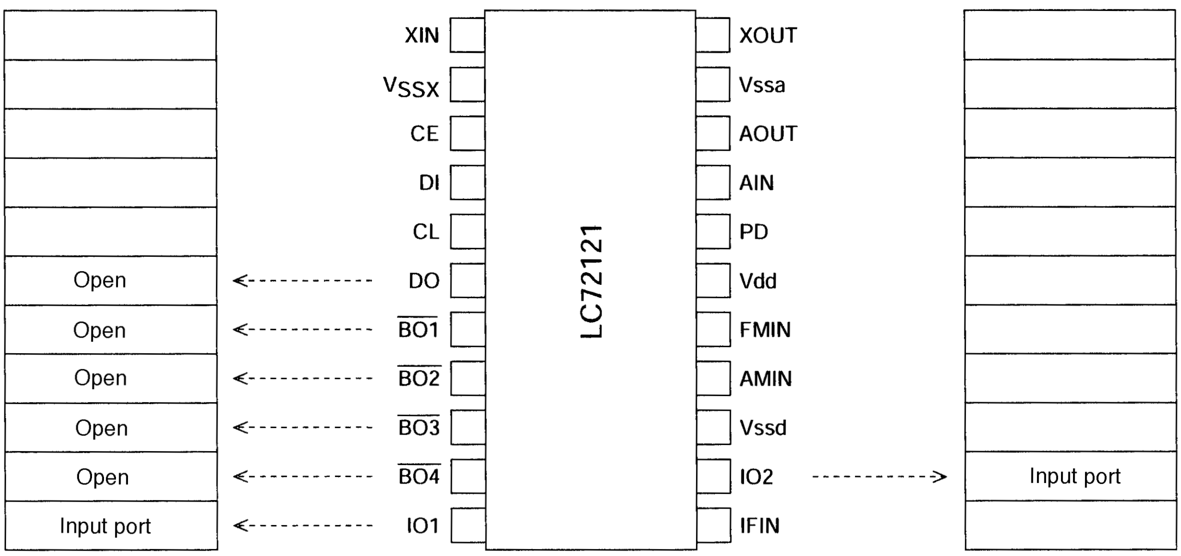
Clock Time Base Usage Notes

When using the clock time base output function, the output pin (BO1) pull-up resistor must have a value of over 100 kΩ. The use of a Schmitt input in the microcontroller that accepts this signal is recommended to reduce chattering. This is to prevent degradation of the VCO C/N characteristics when combining with a loop filter that uses the internal transistor provided to form a low-pass filter. Although the ground for the clock time base output pin (V_{SSd}) and the ground for the transistor (V_{SSa}) are isolated internally on the chip, applications must take care to avoid ground loops and minimize current fluctuations in the time base pin to prevent degradation of the low-pass filter characteristics.



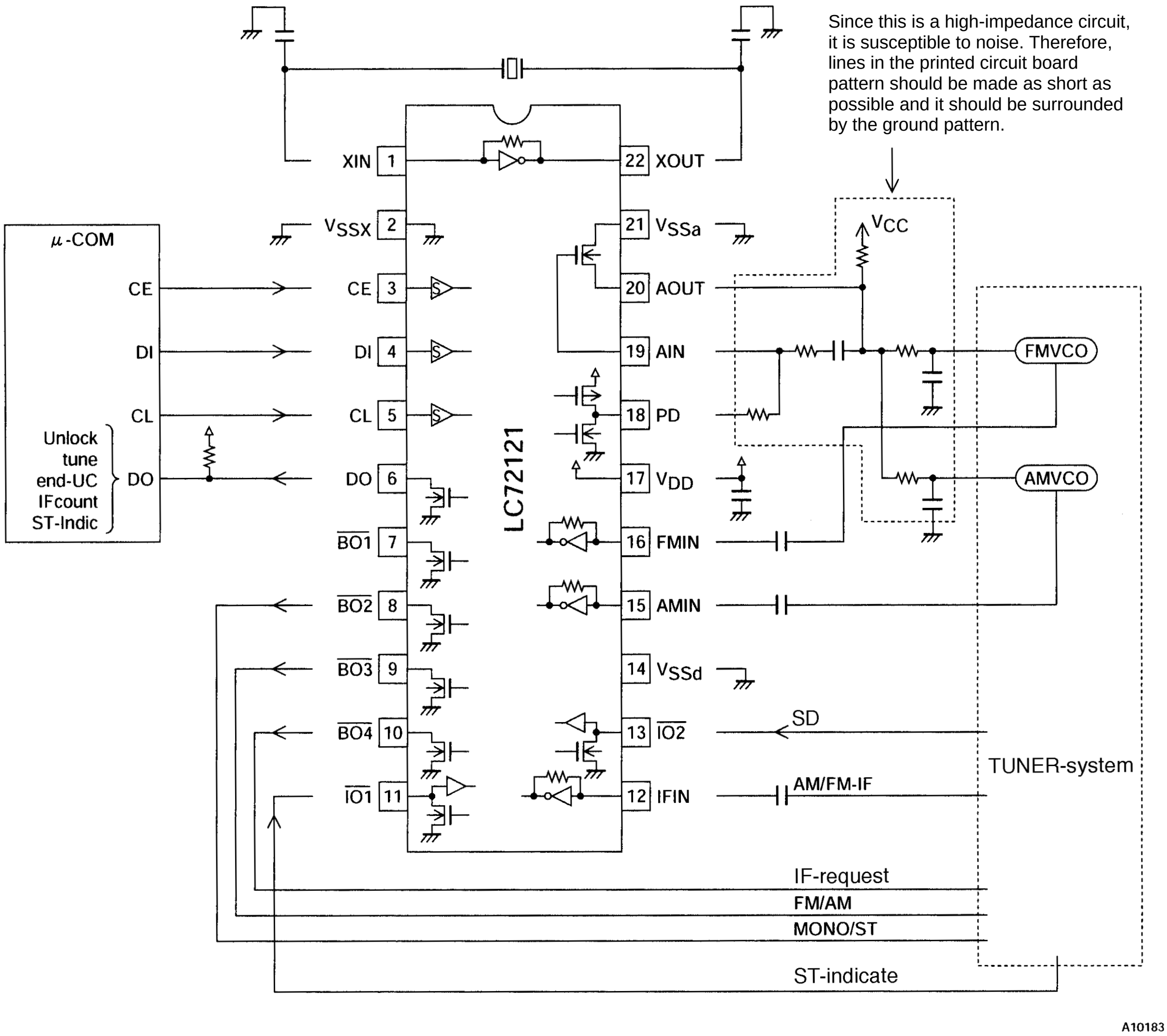
A10181

Pin States after a Power on Reset



A10182

Sample Application Circuit
(Using the DIP22S package)



Other Items

- Notes on the phase comparator dead zone

DZ1	DZ0	Dead zone mode	Charge pump	Dead zone
0	0	DZA	ON/ON	– –0s
0	1	DZB	ON/ON	–0s
1	0	DZC	OFF/OFF	+0s
1	1	DZD	OFF/OFF	+ +0s

When the charge pump is used with one of the ON/ON modes, correction pulses are generated from the charge pump even if the PLL is locked. As a result, it is easy for the loop to become unstable, and special care is required in application design. The following problems can occur if an ON/ON mode is used.

— Sidebands may be created by reference frequency leakage.

— Sidebands may be created by low-frequency leakage due to the correction pulse envelope.

Although the loop is more stable when a dead zone is present (i.e. when an OFF/OFF mode is used), a dead zone makes it more difficult to achieve excellent C/N characteristics. On the other hand, while it is easy to achieve good C/N characteristics when there is no dead zone, achieving good loop stability is difficult. Accordingly, the DZA and DZB settings, in which there is no dead zone, can be effective in situations where a signal-to-noise ratio of 90 to 100 dB or higher is required in FM reception, or where it is desirable to increase the pilot margin in AM stereo reception. However, if such a high signal-to-noise ratio is not required for FM reception, if an adequate pilot margin can be acquired in AM stereo reception, or if AM stereo is not required, then either DZC or DZD, in which there is a dead zone, should be chosen.

Dead Zone

As shown in figure 1, the phase comparator compares a reference frequency (fr) with fp. As shown in figure 2, the phase comparator's characteristics consist of an output voltage (V) that is proportional to the phase difference ø. However, due to internal circuit delay and other factors, an actual circuit has a region (the dead zone, B) where the circuit cannot actually compare the phases. To implement a receiver with a high S/N ratio, it is desirable that this region be as small as possible. However, it is often desirable to have the dead zone be slightly wider in popularly-priced models. This is because in certain cases, such as when there is a strong RF input, popularly-priced models can suffer from mixer to VCO RF leakage that modulates the VCO. When the dead zone is small, the circuit outputs signals to correct this modulation and this output further modulates the VCO. This further modulation may then generate beats and the RF signal.

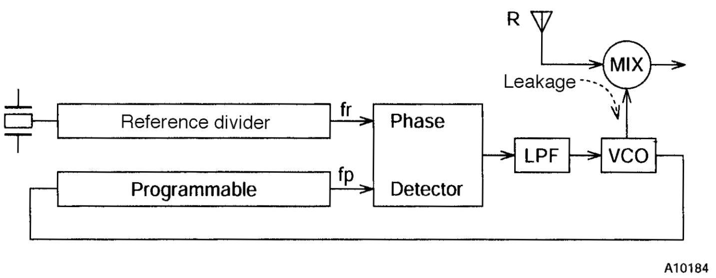


Figure 1

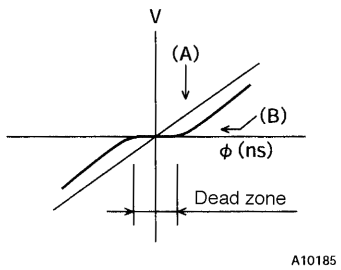


Figure 2

- Notes on the FMIN, AMIN, and IFIN pins

  Coupling capacitors should be placed as close to their pin as possible. A capacitance of about 100 pF is desirable for these capacitors. In particular, if the IFIN pin coupling capacitor is not held under 1000 pF, the time to reach the bias level may become excessive and incorrect counts may result due to the relationship with the wait time.

- Notes on IF counting → Use the SD signal in conjunction with IF counting

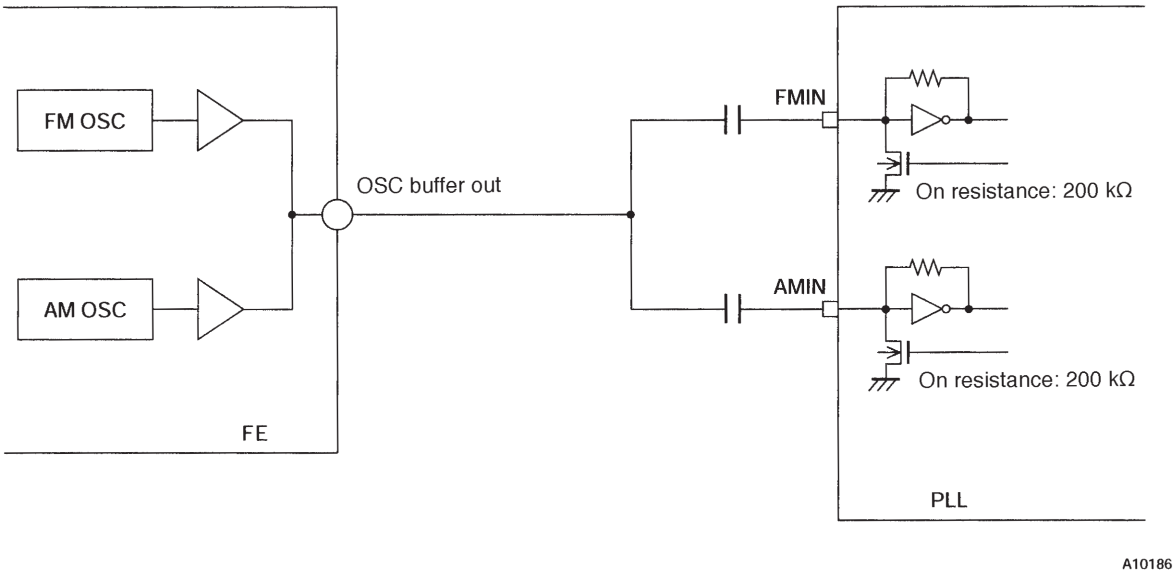
  When counting the IF frequency, the microcontroller must determine the presence or absence of the IF IC SD (station detect) signal and turn on the IF counter buffer output and execute the IF count only if there is an SD signal. Auto-search techniques that only use the IF counter are subject to incorrect stopping at points where there is no station due to IF buffer leakage.

- DO pin usage
  The DO pin can be used for IF counter count completion checking and as an unlock detection output in addition to its use in data output mode. It is also possible to have the DO pin reflect the state of an input pin to input that state to the microcontroller.

- Power supply pins
  Capacitors must be inserted between the power supply V_{DD} and V_{SS} pins for noise exclusion. These capacitors must be placed as close as possible to the V_{DD} and V_{SS} pins.

- VCO setup
  Applications must be designed so that the VCO (local oscillator) does not stop, even if the control voltage (Vtune) goes to 0 V. If it is possible for the oscillator to stop, the application must use the control data (DLC) to temporarily force Vtune to V_{CC} to prevent deadlock from occurring. (Deadlock clear circuit)

- Front end connection example
  Since this product (and the LC72131 as well) is designed with the relatively high resistance of 200 kΩ for the pull-down (on) resistors built in to the FMIN and AMIN pins, a common AM/FM local oscillator buffer can be used as shown in the following circuit.



- PD pin
  Note that the charge pump output voltage is reduced when this IC, which is a 3-V system, is used to replace the LC72131, which is a 5-V system. This means that since the loop gain is reduced, the loop filter constants, the lock time (SD wait time), and other related parameters must be reevaluated in the end product design.