GALVANTECH, INC.

GVT71256T18
256K X 18 SYNCHRONOUS TAG SRAM

SYNCHRONOUS CACHE TAG SRAM PIPELINED OUTPUT

256K x 18 SRAM

+3.3V SUPPLY WITH CLOCKED REGISTERED INPUTS

FEATURES

- Fast match times: 3.5, 3.8, 4.0 and 4.5ns
- Fast clock speed: 166, 150, 133, and 100MHz
- Fast OE# access times: 3.5, 3.8, 4.0 and 5.0ns
- Pipelined data comparator
- Data input register load control by DEN#
- Optimal for depth expansion (one cycle chip deselect to eliminate bus contention)
- 3.3V -5% and +10% core power supply
- 2.5V or 3.3V I/O supply
- 5V tolerant inputs except I/O's
- Clamp diodes to VSS at all inputs and outputs
- Common data inputs and data outputs
- JTAG boundary scan
- BYTE WRITE ENABLE and GLOBAL WRITE control
- Three chip enables for depth expansion and address pipeline
- Address, data and control registers
- Internally self-timed WRITE CYCLE
- Burst control pins (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- Low profile 119 lead, 14mm x 22mm BGA (Ball Grid Array) and JEDEC standard 100 pin TQFP packages

OPTIONS — MARKING

- Timing

3.5ns access/6.0ns cycle	-6
3.8ns access/6.7ns cycle	-6.7
4.0ns access/7.5ns cycle	-7.5
4.5ns access/10ns cycle	-10

- Packages

119-lead BGA	B
100-pin TQFP	T

GENERAL DESCRIPTION

The Galvantech Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable (CE#), depth-expansion chip enables (CE2# and CE2), burst control inputs (ADSC#, ADSP#, and ADV#), write enables (WEL#, WEH#, and BWE#), global write (GW#), and data input enable (DEN#).

Asynchronous inputs include the burst mode control (MODE), the output enable (OE#) and the match output enable (MOE#). The data outputs (Q) and match output (MATCH), enabled by OE# and MOE# respectively, are also asynchronous.

Addresses and chip enables are registered with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Data inputs are registered with data input enable (DEN#) and chip enable pins (CE#, CE2 and CE2#). The outputs of the data input registers are compared with data in the memory array and a match signal is generated. The match output is gated into a pipeline register and released to the match output pin at the next rising edge of clock (CLK).

Address, data inputs, and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to two bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. WEL# controls DQ1-DQ9. WEH# controls DQ10-DQ18. WEL#, and WEH# can be active only with BWE# being LOW. GW# being LOW causes all bytes to be written.

The GVT71256T18 operates from a +3.3V power supply with output power supply being +2.5V or +3.3V. All inputs and outputs are LVTTL compatible. The device is ideally suited for address tag RAM for up to 8MB secondary cache.

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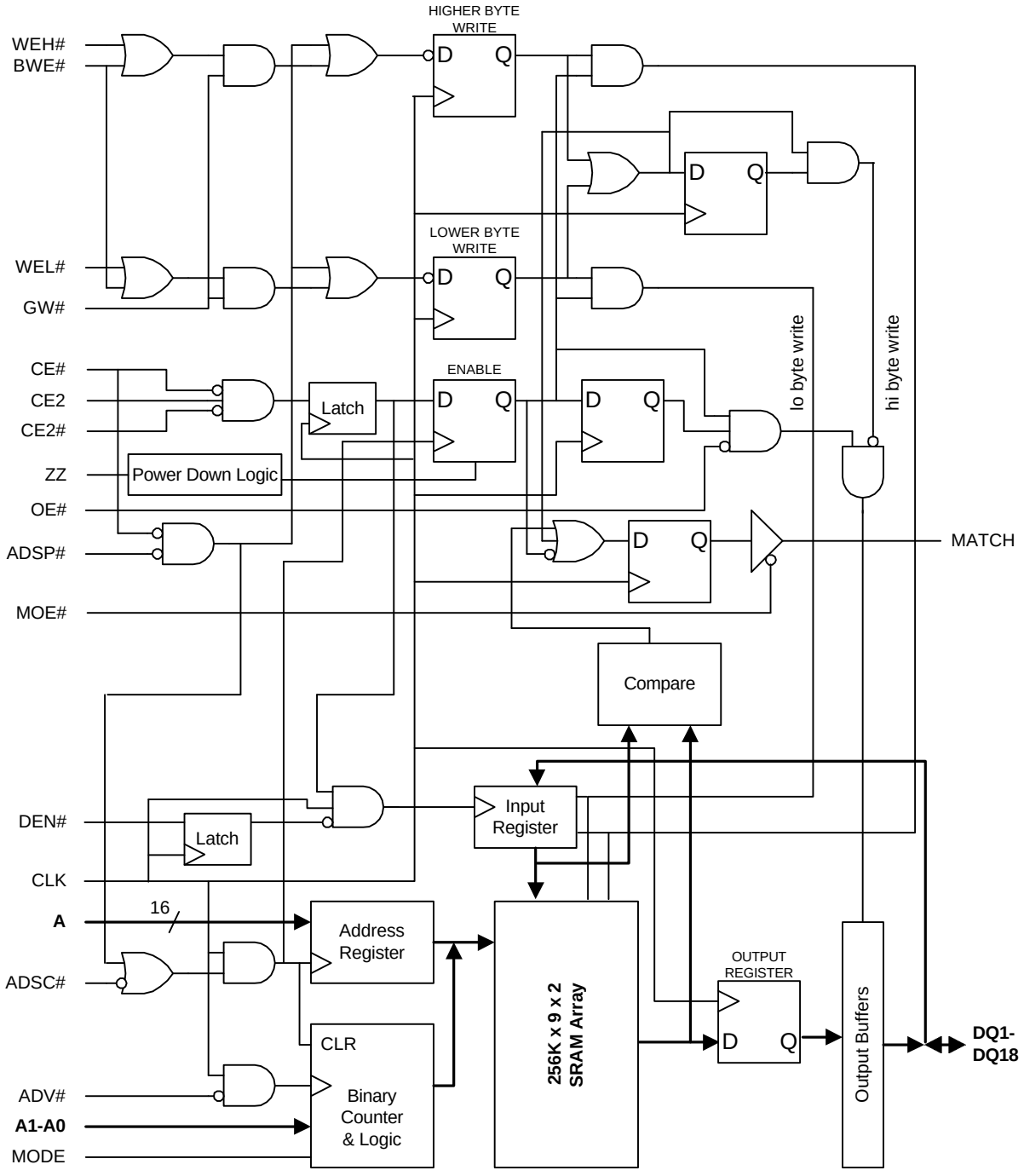
Rev. 8/98

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

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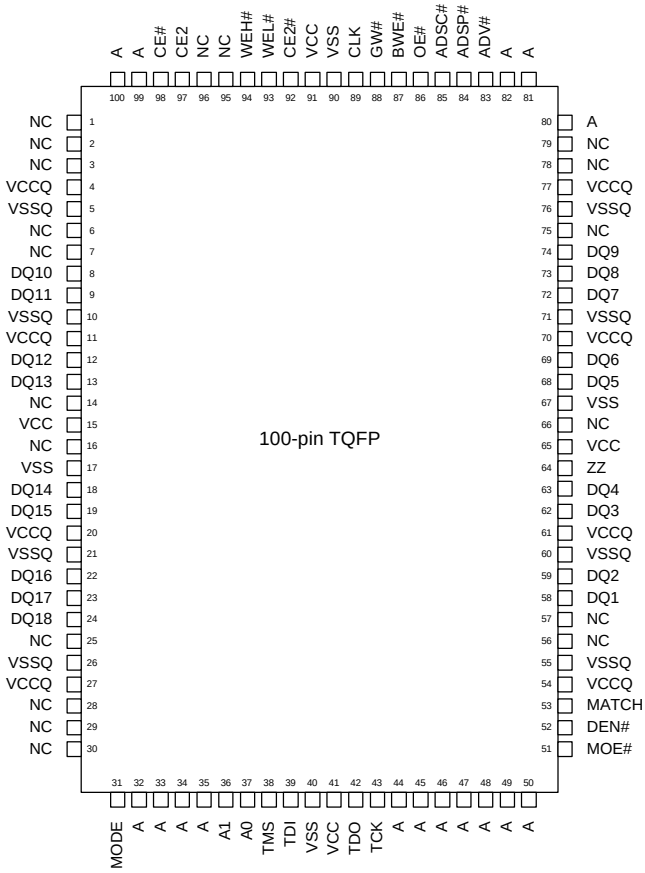
256K X 18 SYNCHRONOUS TAG SRAM

PIN ASSIGNMENTS (TOP VIEW)

	1	2	3	4	5	6	7
A	VCCQ	A	A	ADSP#	A	A	VCCQ
B	NC	CE2	A	ADSC#	A	CE2#	NC
C	NC	A	A	VCC	A	A	NC
D	DQ10	NC	VSS	NC	VSS	DQ9	NC
E	NC	DQ11	VSS	CE#	VSS	NC	DQ8
F	VCCQ	NC	VSS	OE#	VSS	DQ7	VCCQ
G	NC	DQ12	WEH#	ADV#	VSS	NC	DQ6
H	DQ13	NC	VSS	GW#	VSS	DQ5	NC
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	NC	DQ14	VSS	CLK	VSS	NC	DQ4
L	DQ15	NC	VSS	NC	WEL#	DQ3	NC
M	VCCQ	DQ16	VSS	BWE#	VSS	MATCH	VCCQ
N	DQ17	NC	VSS	A1	VSS	DQ2	DEN#
P	NC	DQ18	VSS	A0	VSS	MOE#	DQ1
R	NC	A	MODE	VCC	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VCCQ	TMS	TDI	TCK	TDO	NC	VCCQ

TOP VIEW 119 LEAD BGA



PIN DESCRIPTIONS

BGA PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	37 36 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44, 49, 50	A0 A1 A	Input-Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
5L 3G	93 94	WEL# WEH#	Input-Synchronous	Byte Write Enables: A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. WEL# controls DQ1-DQ9. WEH# controls DQ10-DQ18. Data I/O are high impedance if either of these inputs are LOW, conditioned by BWE# being LOW.
4M	87	BWE#	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.
4H	88	GW#	Input-Synchronous	Global Write: This active LOW input allows a full 18-bit WRITE to occur independent of the BWE# and WEn# lines and must meet the setup and hold times around the rising edge of CLK.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and data input enable control input on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	98	CE#	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate ADSP#.
6B	92	CE2#	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
2B	97	CE2	input-Synchronous	Chip enable: This active HIGH input is used to enable the device.
4F	86	OE#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
4G	83	ADV#	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
4A	84	ADSP#	Input-Synchronous	Address Status Processor: This active LOW input, along with CE# being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
4B	85	ADSC#	Input-Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
3R	31	MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
7T	64	ZZ	Input-Asynchronous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
7N	52	DEN#	Input-Synchronous	Data Input Enable: This active LOW input is used to control the update of data input registers.
6M	53	MATCH	Output	Match Output: MATCH will be HIGH if data in the data input registers match the data stored in the memory array, assuming MOE# being LOW. MATCH will be LOW if data do not match.
6P	51	MOE#	Input	Match Output Enable: This active LOW asynchronous input enables the MATCH output drivers.
7P, 6N, 6L, 7K, 6H, 7G, 6F, 7E, 6D, 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	58, 59, 62, 63, 68, 69, 72, 73, 74, 8, 9, 12, 13, 18, 19, 22, 23, 24	DQ1-DQ18	Input/ Output	Data Inputs/Outputs: Input data must meet setup and hold times around the rising edge of CLK.
5U	42	TDO	Output	IEEE 1149.1 test output. LVTTL-level output.

PIN DESCRIPTIONS (continued)

BGA PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
2U 3U 4U	38 39 43	TMS TDI TCK	Input	IEEE 1149.1 test inputs. LVTTL-level inputs.
4C, 2J, 4J, 6J, 4R	15, 41,65, 91	VCC	Supply	Power Supply: +3.3V -5% and +10%
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	VSS	Ground	Ground: GND.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	4, 11, 20, 27, 54, 61, 70, 77	VCCQ	I/O Supply	Output Buffer Supply: +2.5V (from 2.375V to VCC)
1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 2N, 1P, 1R, 5R, 7R, 1T, 4T, 6U	1-3, 6, 7, 14, 16, 25, 28-30, 56, 57, 66, 75, 78, 79, 95, 96	NC	-	No Connect: These signals are not internally connected.

BURST ADDRESS TABLE (MODE = NC/VCC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

BURST ADDRESS TABLE (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

PARTIAL TRUTH TABLE FOR MATCH

OPERATION	E#	WE#	DEN#	MOE##	OE#	MATCH	DQ
READ Cycle	L	H	X	X	L	-	Q
WRITE Cycle	L	L	L	X	H	-	D
Fill WRITE Cycle	L	L	H	X	H	-	High-Z
COMPARE Cycle	L	H	L	L	H	Output	D
Deselected Cycle (MATCH Out)	H	X	X	L	X	H	High-Z
Deselected Cycle	H	X	X	H	X	High-Z	High-Z

Note:
1. X means “don’t care.” H means logic HIGH. L means logic LOW. It is assumed in this table that ADSP# is HIGH and ADSC# is LOW.
2. E# =L is defined as CE#=LOW and CE2#=LOW and CE2=HIGH. E# =H is defined as CE#=HIGH or CE2#=HIGH or CE2=LOW. WE# is defined as [BWE# + WEL#*WEH#]*GW#.
3. All inputs except OE# and MOE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. For a write operation following a read operation, OE# must be HIGH before the input data required setup time plus High-Z time for OE# and staying HIGH throughout the input data hold time.
5. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

TRUTH TABLE

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Note: 1. X means “don’t care.” H means logic HIGH. L means logic LOW. WRITE# = L means [BWE# + WEL#*WEH#]*GW# equals LOW. WRITE# = H means [BWE# + WEL#*WEH#]*GW# equals HIGH. It is assumed in this truth table that DEN# is LOW.
2. WEL# enables write to DQ1-DQ9. WEH# enables write to DQ10-DQ18.
3. All inputs except OE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Suspending burst generates wait cycle.
5. For a write operation following a read operation, OE# must be HIGH before the input data required setup time plus High-Z time for OE# and staying HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. ADSP# LOW along with chip being selected always initiates an READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting WRITE# LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR READ/WRITE

FUNCTION	GW#	BWE#	WEH#	WEL#
READ	H	H	X	X
READ	H	L	H	H
WRITE one byte	H	L	L	H
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

Note: 1. X means “don’t care.” H means logic HIGH. L means logic LOW. It is assumed in this truth table that chip is selected and ADSP# is HIGH along with DEN# being LOW.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +150°
Junction Temperature .....+150°
Power Dissipation 1.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed uunder "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_a ≤ 70°C; VCC = 3.3V -5% and +10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage	Data Inputs (DQxx)	V_{IHD}	1.7	VCC+0.3	V	1,2
	All Other Inputs	V_{IH}	1.7	4.6	V	1,2
Input Low (Logic 0) Voltage		V_{II}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-2	2	uA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-2	2	uA	
Output High Voltage	I_{OH} = -4.0mA at VCCQ=3.135V	V_{OH}	2.4		V	1, 11
	I_{OH} = -4.0mA at VCCQ=2.375V	V_{OH}	1.7		V	1, 11
Output Low Voltage	I_{OL} =8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		VCC	3.135	3.6	V	1
I/O Supply Voltage		VCCQ	2.375	VCC	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	- 6	- 6.7	- 7.5	- 10	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL}or ≥ V_{IH};cycle time ≥ ^tKC MIN; VCC =MAX; outputs open	Icc	100	310	275	250	190	mA	3, 12, 13
CMOS Standby	Device deselected; VCC = MAX; all inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; CLK frequency = 0	I_{SB2}	5	10	10	10	10	mA	12,13
TTL Standby	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; VCC = MAX; CLK frequency = 0	I_{SB3}	10	20	20	20	20	mA	12,13
Clock Running	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; VCC = MAX; CLK cycle time ≥ ^tKC MIN	I_{SB4}	40	80	70	60	50	mA	12,13

THERMAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	BGA TYP	TQFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	Θ_{JA}	19	25	°C/W	
Thermal Resistance - Junction to Case		Θ_{JC}	9	9	°C/W	

AC ELECTRICAL CHARACTERISTICS

(Note 5) ($0^oC \leq T_A \leq 70^oC$; VCC = 3.3V -5% and +10%)

DESCRIPTION		- 6 166MHz		- 6.7 150MHz		- 7.5 133MHz		- 10 100MHz			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	6.0		6.7		7.5		10		ns	
Clock frequency	^fKF		166		150		133		100	MHz	
Clock HIGH time	^tKH	1.5		1.5		2.0		2.0		ns	
Clock LOW time	^tKL	1.5		1.5		2.0		2.0		ns	
Output Times											
Clock to output valid	^tKQ		3.5		3.8		4.0		4.5	ns	
Clock to MATCH valid	^tKM		3.5		3.8		4.0		4.5	ns	
Clock to output invalid	^tKQX	1.5		1.5		1.5		1.5		ns	
Clock to MATCH invalid	^tKMX	1.5		1.5		1.5		1.5		ns	
Clock to output in Low-Z	^tKQLZ	1.5		1.5		1.5		1.5		ns	4, 6,7
Clock to output in High-Z	^tKQHZ	1.5	3.5	1.5	3.8	1.5	4.0	1.5	5.0	ns	4, 6,7
OE to output valid	^tOEQ		3.5		3.8		4.0		5.0	ns	9
MOE to MATCH valid	^tMOEM		3.5		3.8		4.0		5.0	ns	9
OE to output in Low-Z	^tOELZ	0		0		0		0		ns	4, 6,7
MOE to MATCH in Low-Z	^tMOELZ	0		0		0		0		ns	4, 6,7
OE to output in High-Z	^tOEHZ		3.5		3.8		4.0		5.0	ns	4, 6,7
MOE to MATCH in High-Z	^tMOEHZ		3.5		3.8		4.0		5.0	ns	4, 6,7
Setup Times											
Address, Controls and Data In	^tS	1.5		1.5		2.0		2.0		ns	10
Hold Times											
Address, Controls and Data In	^tH	0.5		0.5		0.5		0.5		ns	10

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$; f = 1 MHz VCC = 3.3V	C_I	4	5	pF	4
Input/Output Capacitance (DQ)		C_O	7	8	pF	4

TYPICAL OUTPUT BUFFER CHARACTERISTICS

OUTPUT HIGH VOLTAGE	PULL-UP CURRENT			OUTPUT LOW VOLTAGE	PULL-DOWN CURRENT	
VOH (V)	IOH(mA) Min	IOH(mA) Max		VOL (V)	IOL(mA) Min	IOL(mA) Max
-0.5	-38	-105		-0.5	0	0
0	-38	-105		0	0	0
0.8	-38	-105		0.4	10	20
1.25	-26	-83		0.8	20	40
1.5	-20	-70		1.25	31	63
2.3	0	-30		1.6	40	80
2.7	0	-10		2.8	40	80
2.9	0	0		3.2	40	80
3.4	0	0		3.4	40	80

AC TEST CONDITIONS

Input pulse levels	0V to 2.5V
Input slew rate	1.0V/ns
Output rise and fall times(max)	1.8ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Output load	See Figures 1and 2

OUTPUT LOADS

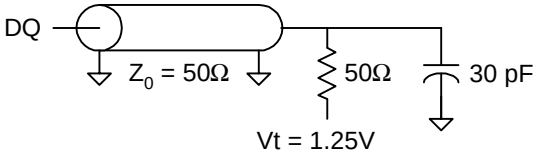


Fig. 1 OUTPUT LOAD EQUIVALENT

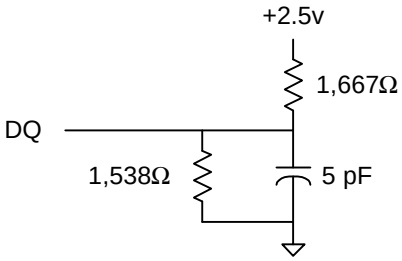
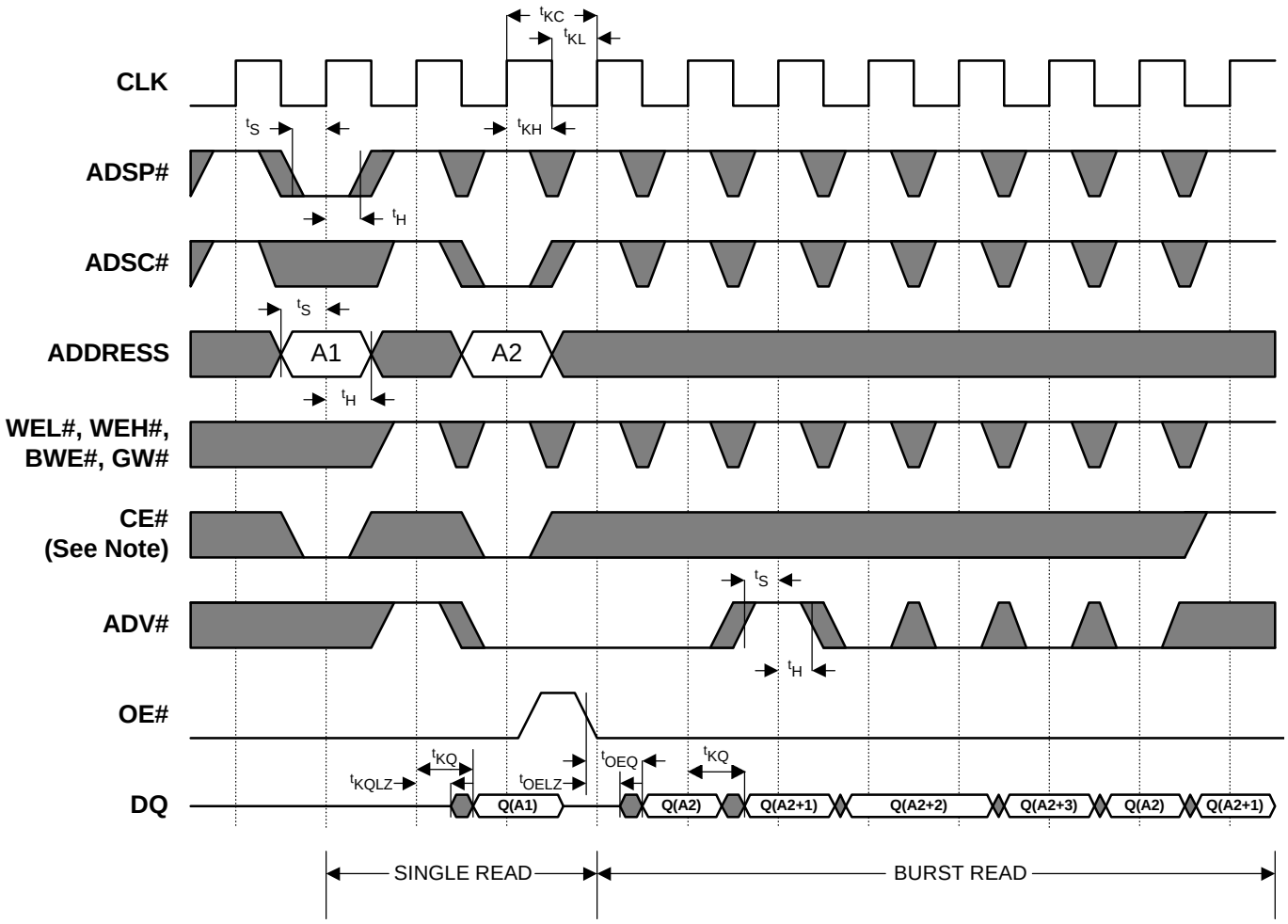


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

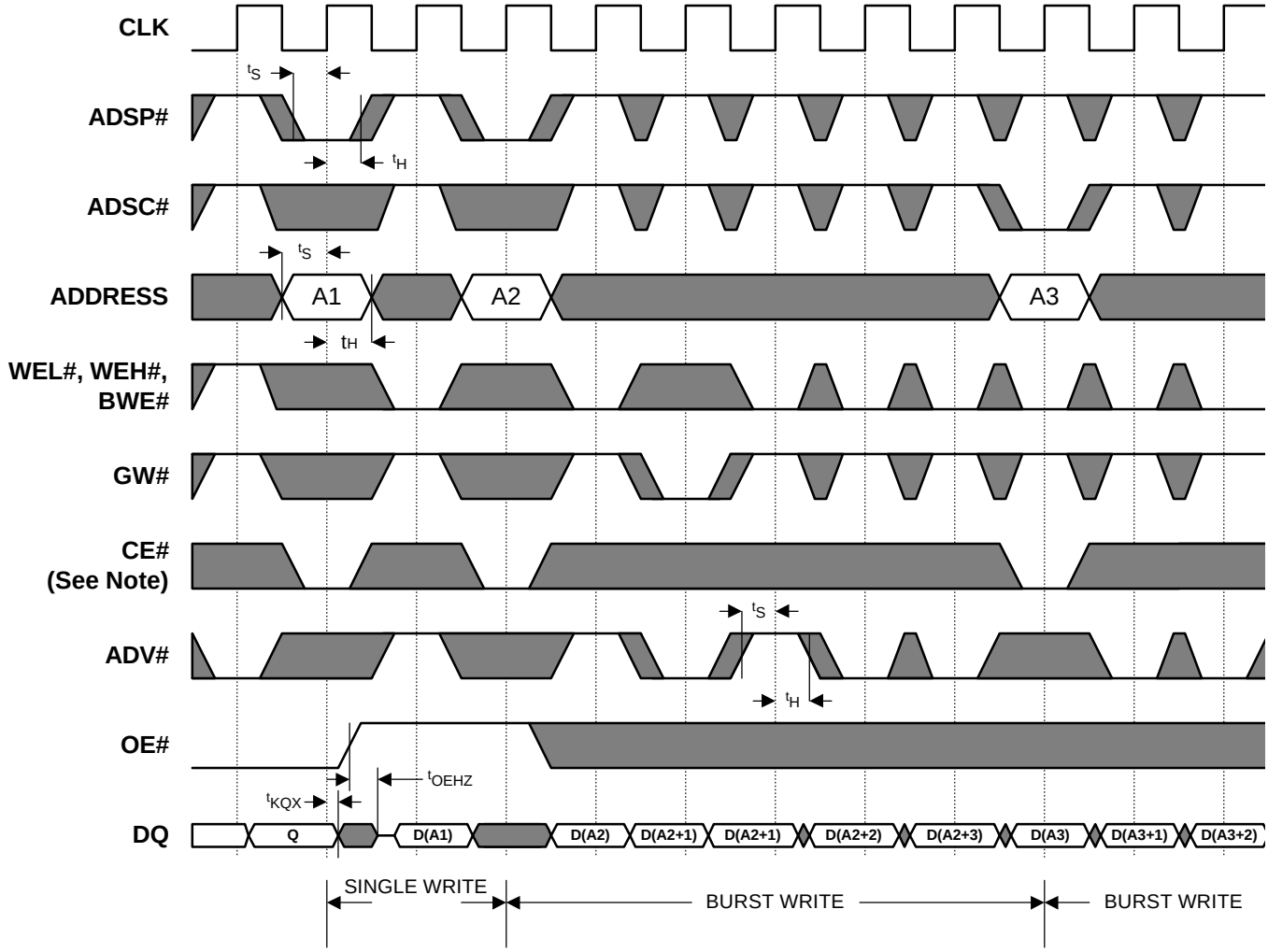
1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tKC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL=5pF as in Fig. 2.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$, ${}^tOEHZ$ is less than ${}^tOELZ$ and ${}^tMOEHZ$ is less than ${}^tMOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or ADSP# LOW along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by at one byte or all byte WRITE per READ/WRITE TRUTH TABLE.
9. OE# is a “don’t care” after a write cycle begins To prevent bus contention, OE# should be negated prior before the start of write cycle.
10. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for “don’t care” as defined in the truth table.
11. AC I/O curves are available upon request.
12. “Device Deselected” means the device is in POWER -DOWN mode as defined in the truth table. “Device Selected” means the device is active.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
15. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

READ TIMING WITH BURST FEATURE



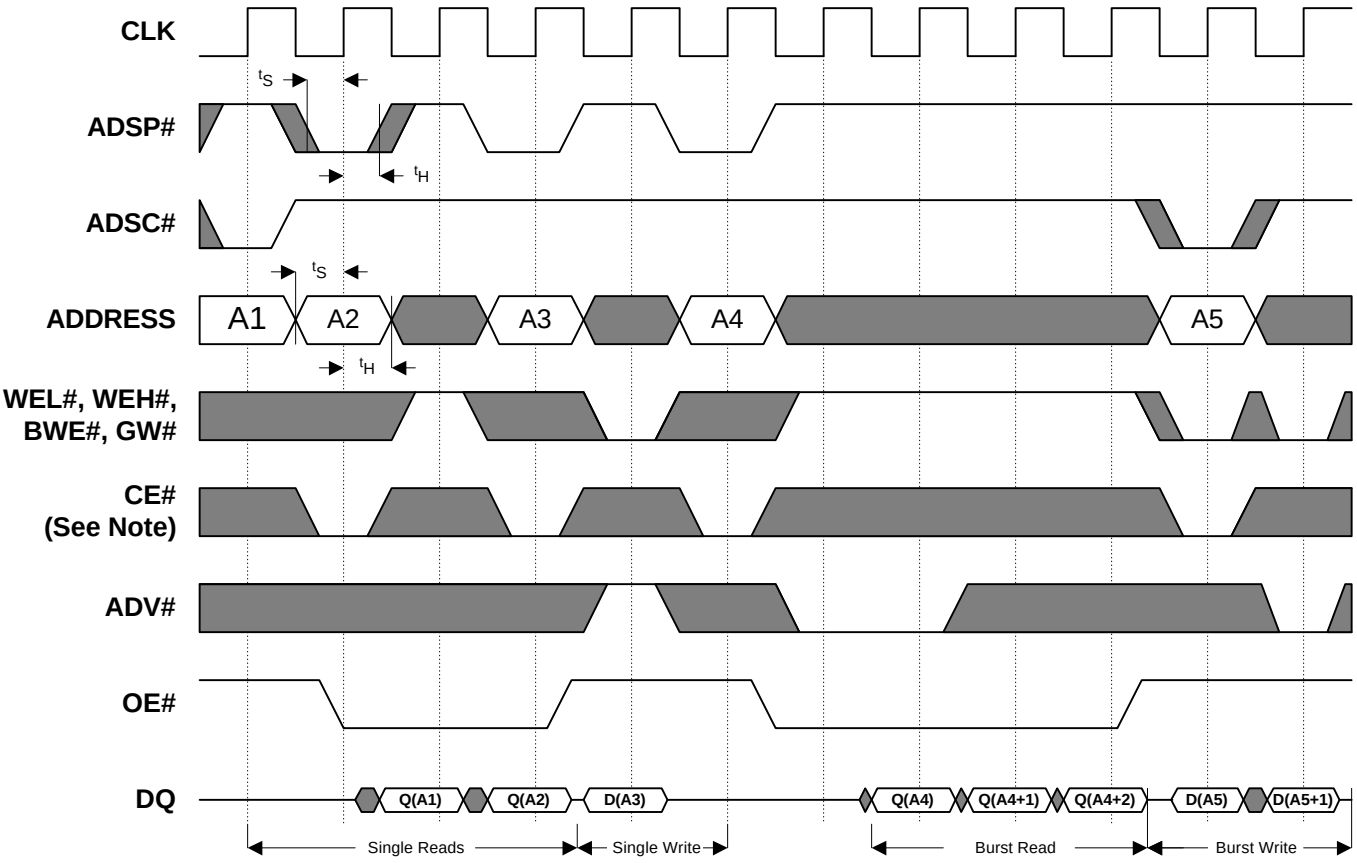
Note: (1) CE# active in this timing diagram means that all chip enables CE#, CE2# and CE2 are active.
(2) In this timing diagram, it is assumed that DEN# is tied to LOW (VSS).

WRITE TIMING WITH BURST FEATURE



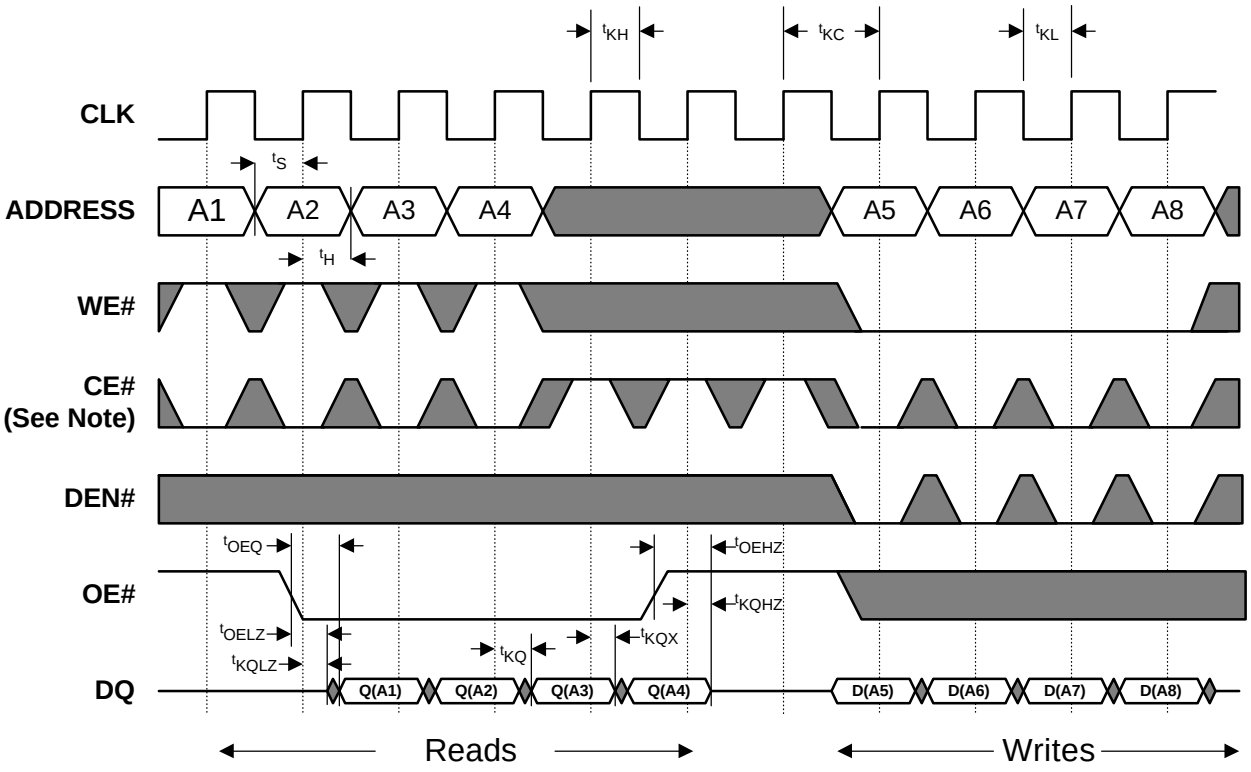
Note: (1) CE# active in this timing diagram means that all chip enables CE#, CE2# and CE2 are active.
(2) In this timing diagram, it is assumed that DEN# is tied to LOW (VSS).

READ/WRITE TIMING WITH BURST FEATURE



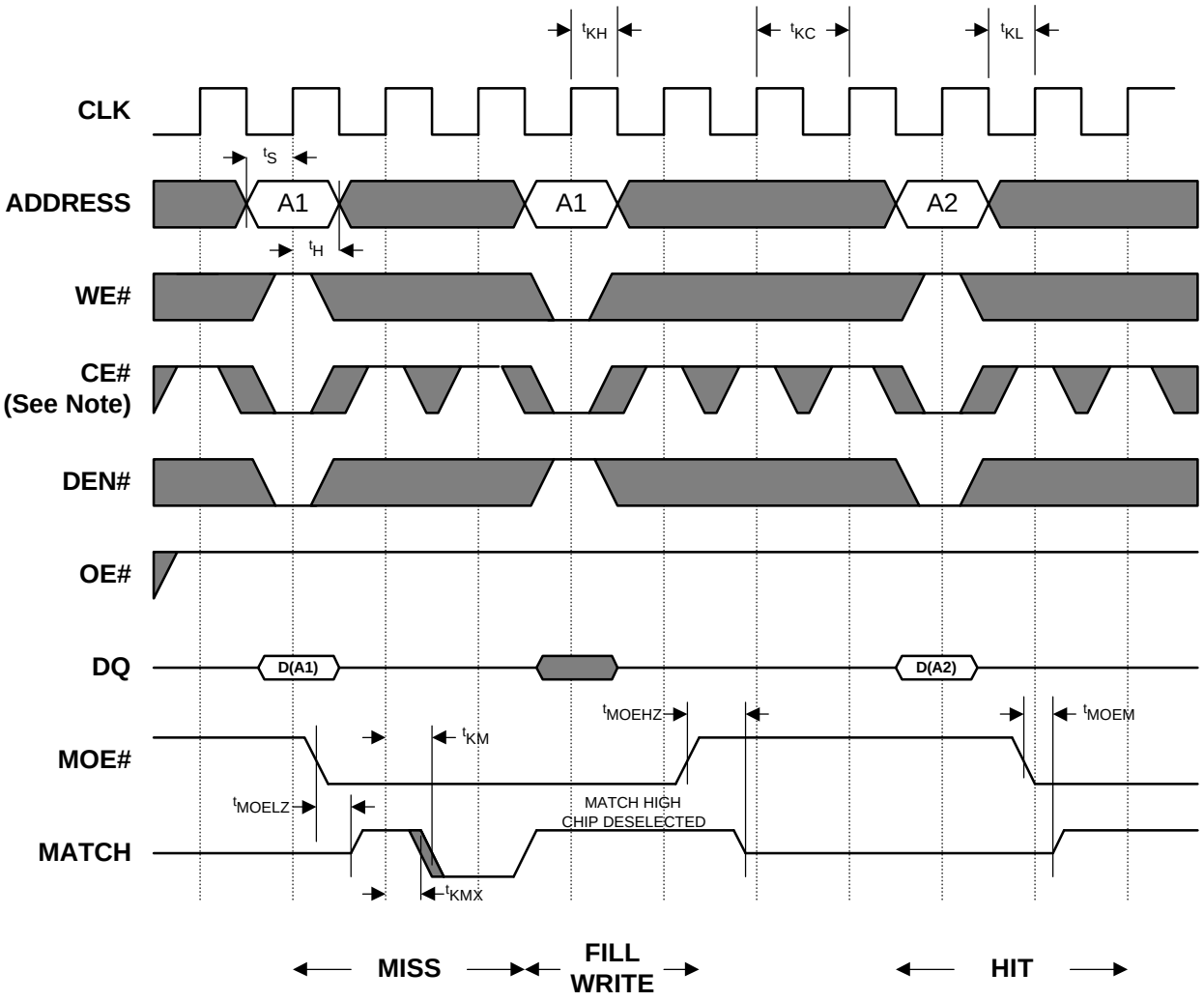
Note: (1) CE# active in this timing diagram means that all chip enables CE#, CE2# and CE2 are active.
(2) In this timing diagram, it is assumed that DEN# is tied to LOW (VSS).

READ/WRITE TIMING WITHOUT BURST FEATURE



Note: (1) CE# active in this timing diagram means that all chip enables CE#, CE2# and CE2 are active.
(2) In this timing diagram, it is assumed that burst feature is not used and therefore ADSP# is tied to HIGH (VCC) and ADSC# is tied to LOW (VSS). The logic state of ADV# is a “Don’t Care”.
(3) In this timing diagram, it is assumed that WE# = [BWE# + WEL#*WEH#]*GW#.

COMPARE/FILL WRITE TIMING



Note: (1) CE# active in this timing diagram means that all chip enables CE#, CE2# and CE2 are active.
(2) In this timing diagram, it is assumed that burst feature is not used and therefore ADSP# is tied to HIGH (VCC) and ADSC# is tied to LOW (VSS). The logic state of ADV# is a “Don’t Care”.
(3) In this timing diagram, it is assumed that WE# = [BWE# + WEL#*WEH#]*GW#.

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

OVERVIEW

This device incorporates a serial boundary scan access port (TAP). This port is designed to operate in a manner consistent with IEEE Standard 1149.1-1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the critical speed path of the device. Nevertheless, the device supports the standard TAP controller architecture (the TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE Standard 1149.1 compliant TAPs. The TAP operates using LVTTL/LVCMOS logic level signaling.

DISABLING THE JTAG FEATURE

It is possible to use this device without using the JTAG feature. To disable the TAP controller without interfering with normal operation of the device, TCK should be tied LOW (VSS) to prevent clocking the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be pulled up to VCC through a resistor. TDO should be left unconnected. Upon power-up the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TCK - TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS - TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TDI - TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 3, TAP Controller State Diagram). It is allowable to leave this pin unconnected if it is not used in an application. The pin is pulled up internally, resulting in a logic HIGH level. TDI is connected to the most significant bit (MSB) of any register. (See Figure 4.)

TDO - TEST DATA OUT (OUTPUT)

The TDO output pin is used to serially clock data-out from the registers. The output that is active depending on the state of the TAP state machine (refer to Figure 3, TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO. TDO is connected to the least significant bit (LSB) of any register. (See Figure 4.)

PERFORMING A TAP RESET

The TAP circuitry does not have a reset pin (TRST#, which is optional in the IEEE 1149.1 specification). A RESET can be performed for the TAP controller by forcing TMS HIGH (VCC) for five rising edges of TCK and pre-loads the instruction register with the IDCODE command. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

At power-up, the TAP is reset internally to ensure that TDO is in a High-Z state.

TEST ACCESS PORT (TAP) REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected, it is connected between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The parallel outputs of the instruction register are automatically preloaded with the IDCODE instruction upon power-up or whenever the

controller is placed in the test-logic reset state. When the TAP controller is in the Capture-IR state, the two least significant bits of the serial instruction register are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

The bypass register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the device TAP to another device in the scan chain with minimum delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

BOUNDARY SCAN REGISTER

The Boundary scan register is connected to all the input and bidirectional I/O pins (not counting the TAP pins) on the device. This also includes a number of NC pins that are reserved for future needs. There are a total of 54 bits in the case of the TAG device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the device I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table describes the order in which the bits are connected. The first column defines the bit's position in the boundary scan register. The MSB of the register is connected to TDI, and LSB is connected to TDO. The second column is the signal name and the third column is the bump number. The third column is the TQFP pin number and the fourth column is the BGA bump number.

INDENTIFICATION (ID) REGISTER

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the device as described in the Identification Register Definitions table.

TAP CONTROLLER INSTRUCTION SET

OVERWIEW

There are two classes of instructions defined in the IEEE Standard 1149.1-1990; the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the device or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction sets for this device are listed in the following tables.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this device.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the device responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between two instructions. Unlike SAMPLE/PRELOAD instruction, EXTEST places the device outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in the instruction upon power-up and at any time the TAP controller is placed in the test-logic reset state.

SAMPLE-Z

If the High-Z instruction is loaded in the instruction register, all output pins are forced to a High-Z state and the boundary scan register is connected between TDI and TDO pins when the TAP controller is in a Shift-DR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory instruction. The PRELOAD portion of the command is not implemented in this device, so the device TAP controller is not fully IEEE 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded in the instruction register and the TAP controller is in the Capture-DR state, a snap shot of the data in the device's input and I/O buffers is loaded into the boundary scan register. Because the device system clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the input and I/O ring contents while the buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. To guarantee that the boundary scan register will capture the correct value of a signal, the device input signals must be stabilized long enough to meet the TAP controller's capture setup plus hold time (tCS plus tCH). The device clock input(s) need not be paused for any other TAP operation except capturing the input and I/O ring contents into the boundary scan register.

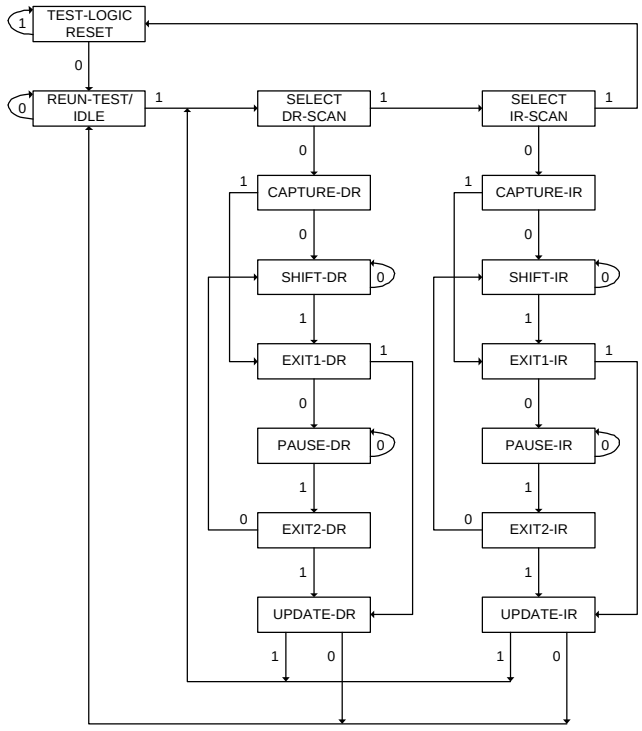
Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP controller is in the Shift-DR state, the bypass register is placed between TDI and TDO. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

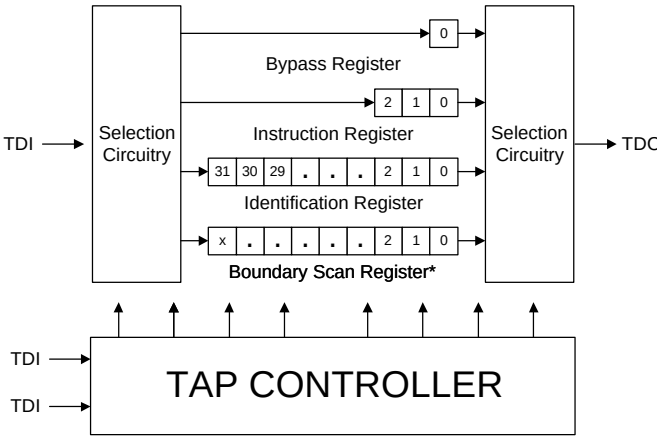
RESERVED

Do not use these instructions. They are reserved for future use.



Note: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Figure 3
TAP CONTROLLER STATE DIAGRAM



*X = 53 for this device.

Figure 4
TAP CONTROLLER BLOCK DIAGRAM

TAP AC TEST CONDITIONS

Input pulse levels	VSS to 3.0V
Iutput rise and fall times	1ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load termination supply voltage	1.5V

TAP OUTPUT LOADS

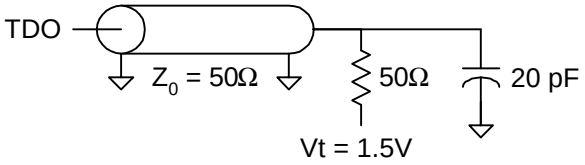


Figure 5
TAP AC OUTPUT LOAD EQUIVALENT

TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

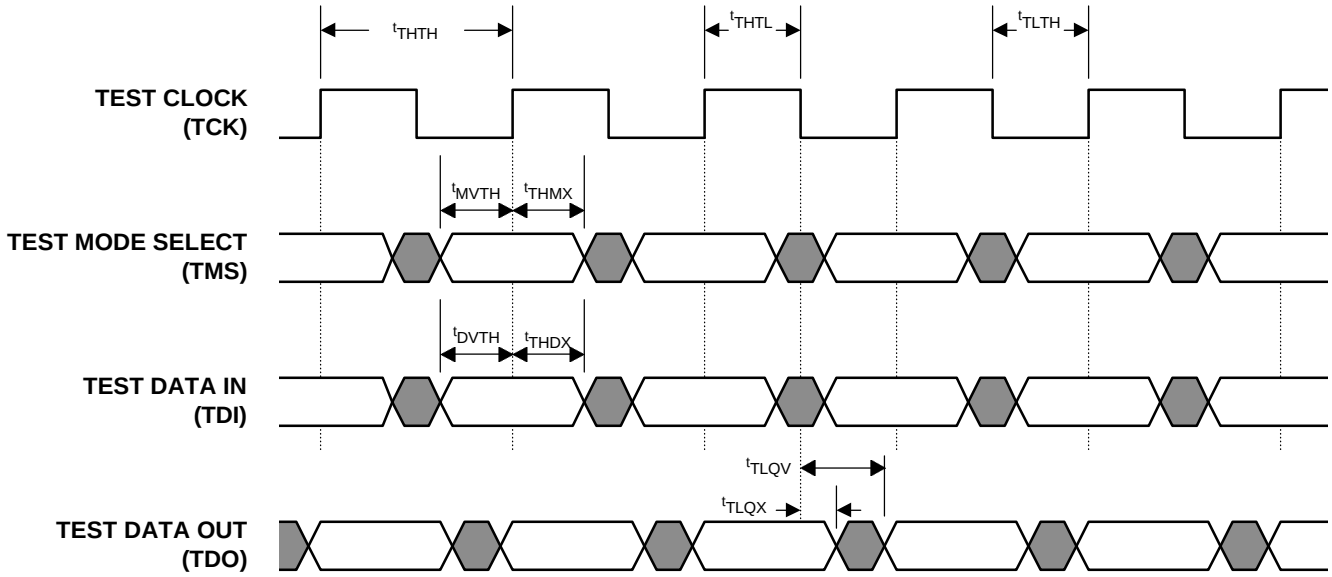
($20^oC \le T_j \le 110°C$; VCC = 3.3V -0.2V and +0.3V unless otherwise noted)

DESCRIPTIOPN	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage		V_{IH}	2.0	VCC + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{Il}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le VCC$	IL_I	-5.0	5.0	uA	
Output Leakage Current	Output disabled, $0V \le V_{IN} \le VCCQ$	IL_O	-5.0	5.0	uA	
LVCMOS Output Low Voltage	I_{OLC} = 100uA	V_{OLC}		0.2		1, 3
LVCMOS Output High Voltage	I_{OHC} = 100uA	V_{OHC}	VCC - 0.2			1, 3
LVTTL Output Low Voltage	I_{OLT} = 8.0mA	V_{OLT}		0.4		1
LVTTL Output High Voltage	I_{OHT} = 8.0mA	V_{OHT}	2.4			1

NOTE:

1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH}(AC) \le VCC + 1.5V$ for $t \le {}^tKHKH/2$.
   Undershoot: $V_{IL}(AC) \le -0.5V$ for $t \le {}^tKHKH/2$
   Power-up: $V_{IH} \le +3.6V$ and $VCC \le 3.135V$ and $VCCQ \le 1.4V$ for $t \le 200ms$
   During normal operation, VCCQ must not exceed VCC. Control input signals (such as GW#, ADSC#, etc.) may not have pulse widths less than ${}^tKHKL$ (MIN).
3. This parameter is sampled.

TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) ($20^oC \leq T_j \leq 110°C$; VCC = 3.3V -0.2V and +0.3V)

DESCRIPTION	SYM	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	20		ns
Clock frequency	^fTF		50	MHz
Clock HIGH time	^tTHTL	8		ns
Clock LOW time	^tTLTH	8		ns
Output Times				
TCK LOW to TDO unknown	^tTLQX	0		ns
TCK LOW to TDO valid	^tTLQV		10	ns
TDI valid to TCK HIGH	^tDVTH	5		ns
TCK HIGH to TDI invalid	^tTHDX	5		ns
Setup Times				
TMS setup	^tMVTH	5		ns
Capture setup	^tCS	5		ns
Hold Times				
TMS hold	^tTHMX	5		ns
Capture hold	^tCH	5		ns

NOTE:

1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 5.

IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	BIT PATTERN	DESCRIPTION
REVISION NUMBER (31:28)	XXXX	Reserved for revision number.
DEVICE DEPTH (27:23)	00110	Defines depth of 256K words.
DEVICE WIDTH (22:18)	00011	Defines width of x18 bits.
RESERVED (17:12)	XXXXXX	Reserved for future use.
GALVANTECH JEDEC ID CODE (11:1)	00011100100	Allows unique identification of DEVICE vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE
Instruction	3
Bypass	1
ID	32
Boundary Scan	54

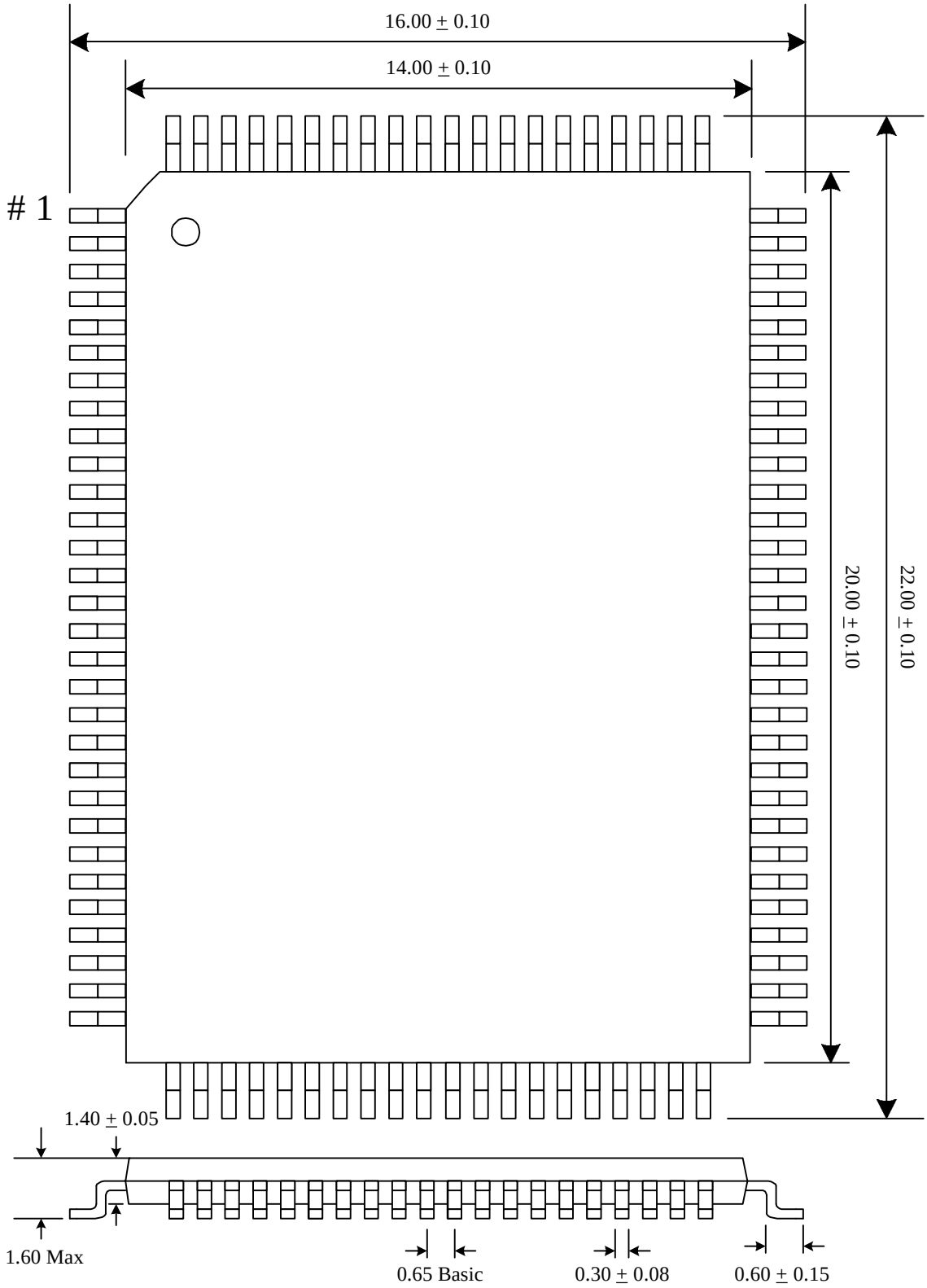
INSTRUCTION CODES

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state. This instruction is not IEEE 1149.1-compliant.
IDCODE	001	Preloads ID register with vendor ID code and places it between TDI and TDO. This instruction does not affect device operations.
SAMPLE-Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state.
RESERVED	011	Do not use these instructions; they are reserved for future use.
SAMPLE/PRE-LOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not affect device operations. This instruction does not implement IEEE 1149.1 PRELOAD function and is therefore not 1149.1-compliant.
RESERVED	101	Do not use these instructions; they are reserved for future use.
RESERVED	110	Do not use these instructions; they are reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This instruction does not affect device operations.

BOUNDARY SCAN ORDER

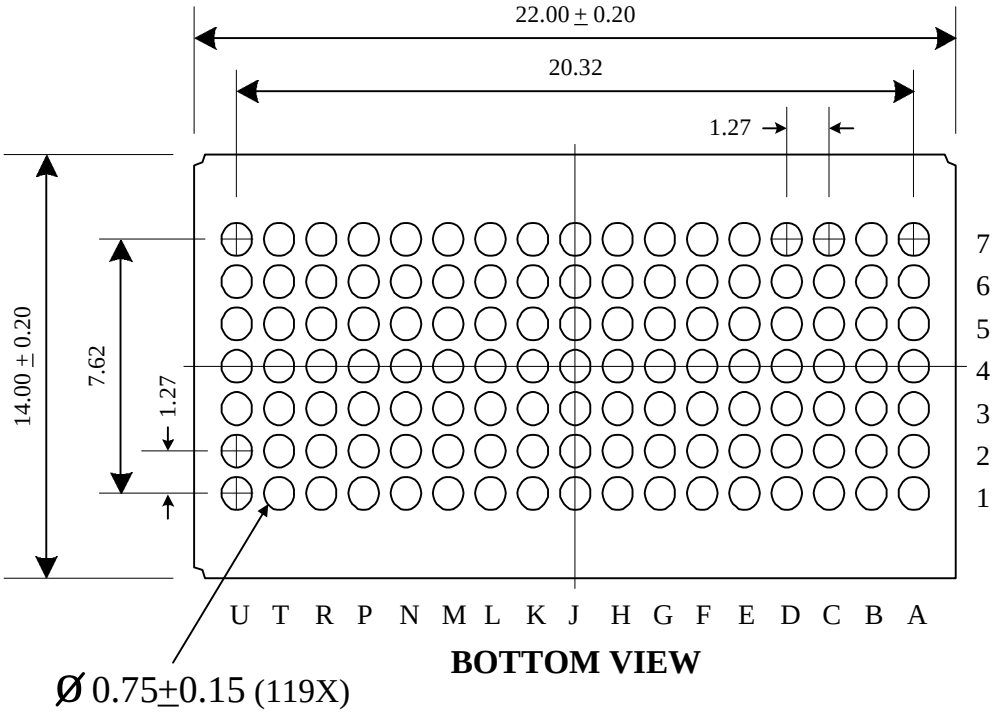
BIT#	SINGAL NAME	TQFP	BUMP ID
1	A	44	2R
2	A	45	2T
3	A	46	3T
4	A	47	5T
5	A	48	6R
6	A	49	3B
7	A	50	5B
8	MOE#	51	6P
9	DEN#	52	7N
10	MATCH	53	6M
11	DQ1	58	7P
12	DQ2	59	6N
13	DQ3	62	6L
14	DQ4	63	7K
15	ZZ	64	7T
16	DQ5	68	6H
17	DQ6	69	7G
18	DQ7	72	6F
19	DQ8	73	7E
20	DQ9	74	6D
21	A	80	6T
22	A	81	6A
23	A	82	5A
24	ADV#	83	4G
25	ADSP#	84	4A
26	ADSC#	85	4B
27	OE#	86	4F
28	BWE#	87	4M
29	GW#	88	4H
30	CLK	89	4K
31	CE2#	92	6B
32	WEL#	93	5L
33	WEH#	94	3G
34	CE2	97	2B
35	CE#	98	4E
36	A	99	3A
37	A	100	2A
38	DQ10	8	ID
39	DQ11	9	2E
40	DQ12	12	2G
41	DQ13	13	1H
42	NC	14	5R
43	DQ14	18	2K
44	DQ15	19	1L
45	DQ16	22	2M
46	DQ17	23	1N
47	DQ18	24	2P
48	MODE	31	3R
49	A	32	2C
50	A	33	3C
51	A	34	5C
52	A	35	6C
53	A1	36	4N
54	A0	37	4P

100 Pin TQFP Package Dimensions

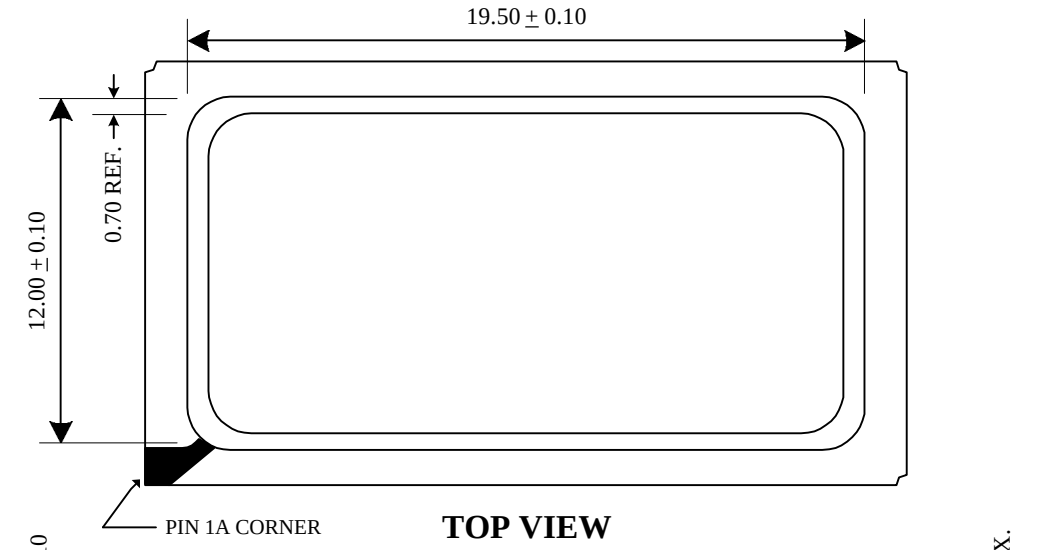


Note: All dimensions in Millimeters

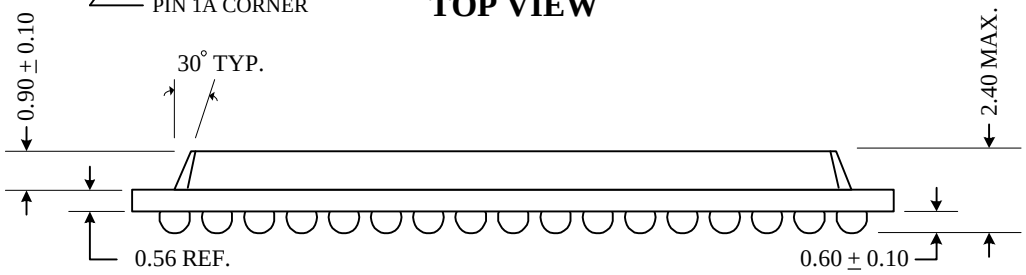
7 x 17 (119-lead) BGA Dimensions



BOTTOM VIEW



TOP VIEW



SIDE VIEW

Note: All dimensions in Millimeters

Ordering Information