Am2716B/Am2732B

2048 x 8-Bit/4096 x 8-Bit EPROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access times — as low as 100 ns
- Low-power dissipation
- Programming voltage — 12.5 V
- Single +5-V power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available

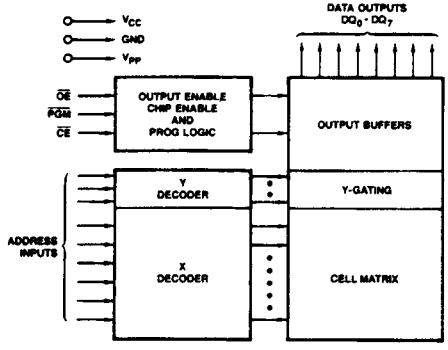
GENERAL DESCRIPTION

The Am2716B and Am2732B are ultraviolet Erasable Programmable Read-Only Memories (EPROMs) and are organized as 2048 x 8 bits, and 4096 x 8 bits, respectively. All standard EPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any Wait states. Some of AMD's EPROMs have access times of as fast as 100 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD EPROMs offer separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's EPROMs may be programmed using 1-ms pulses.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

Family Part No.	Am2716B/Am2732B					
Ordering Part No.:						
±5% V_{CC} Tolerance	2716B-105 2732B-105	2716B-155 2732B-155	2716B-205 2732B-205	2716B 2732B	2716B-305 2732B-305	2716B-455 2732B-455
±10% V_{CC} Tolerance	2716B-100 2732B-100	2716B-150 2732B-150	2716B-200 2732B-200	2716B-250 2732B-250	2716B-300 2732B-300	2716B-450 2732B-450
t_{ACC} (ns)	100	150	200	250	300	450
t_{CE} (ns)	100	150	200	250	300	450
t_{OE} (ns)	75	75	75	100	110	150

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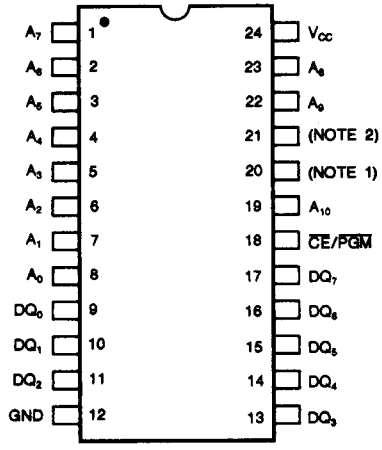
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



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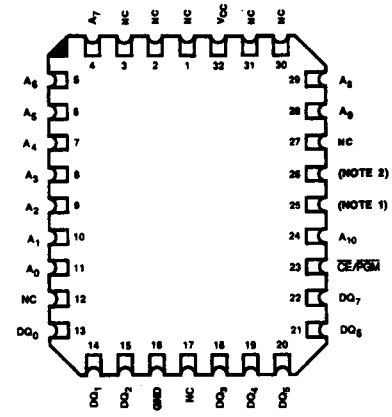

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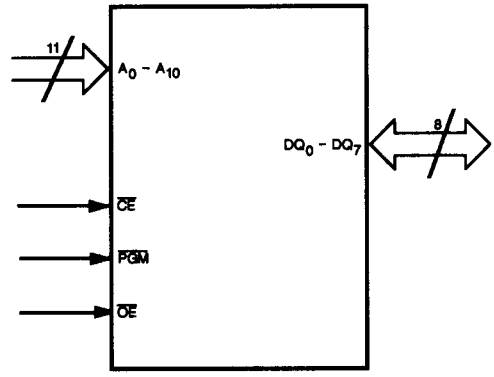
Notes:		Am2716B	Am2732B
	1	$\overline{OE}$	$\overline{OE}/V_{PP}$
	2	V_{PP}	A_{11}

LOGIC SYMBOLS

Am2716B



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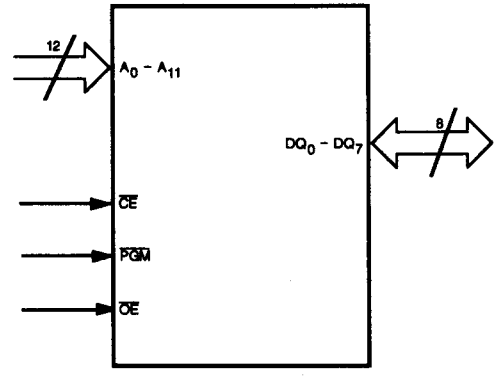
Am2764B



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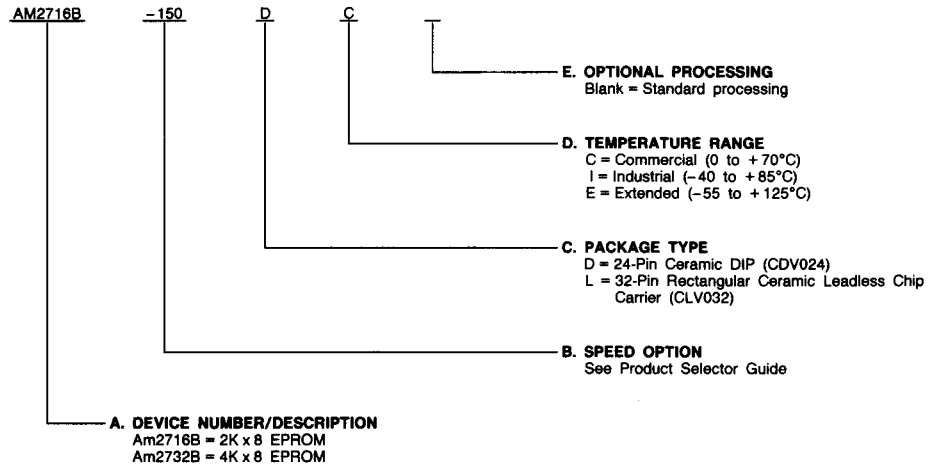
ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
±5% V_{CC} Tolerance	
AM2716B-105	DC, DI, LC, LI
AM2716B-155	
AM2716B-205	
AM2716B	
AM2716B-305	
AM2716B-455	
AM2732B-105	
AM2732B-155	
AM2732B-205	
AM2732B	
AM2732B-305	
AM2732B-455	
±10% V_{CC} Tolerance	
AM2716B-100	DC, DI, LC, LI
AM2716B-150	
AM2732B-100	
AM2732B-150	
AM2716B-200	DC, DI, DE, LC, LI, LE
AM2716B-250	
AM2716B-300	
AM2716B-450	
AM2732B-200	
AM2732B-250	
AM2732B-300	
AM2732B-450	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

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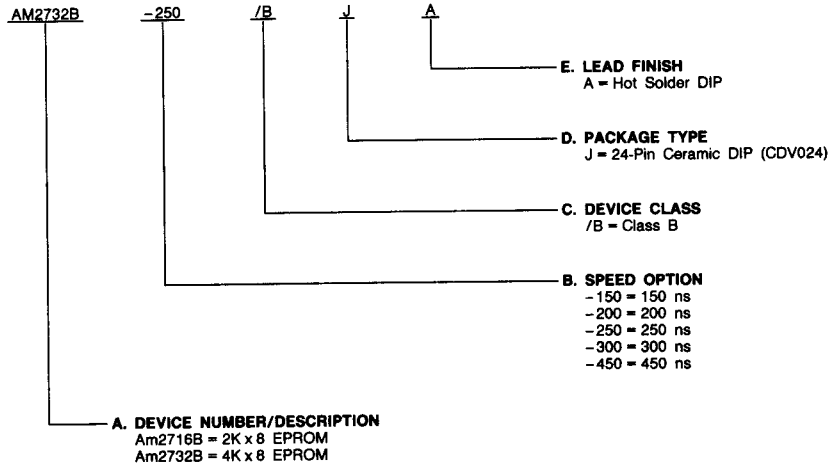
ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
±10% V_{CC} Tolerance	
AM2716B-150	/BJA
AM2716B-200	
AM2716B-250	
AM2716B-300	
AM2716B-450	
AM2732B-150	
AM2732B-200	
AM2732B-250	
AM2732B-300	
AM2732B-450	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

FUNCTIONAL DESCRIPTION

Erasing the EPROMs

In order to clear all locations of their programmed contents, it is necessary to expose the EPROMs to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an EPROM. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 $\mu W/cm^2$ for fifteen to twenty minutes. The EPROM should be about directly under and about one inch from the source and all filters should be removed from the ultraviolet light source prior to erasure.

It is important to note that the EPROMs will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with ultraviolet sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the EPROMs and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the EPROMs

Upon delivery, or after each erasure, the EPROM has all bits in the "1", or HIGH state. Zeros ("0s") are loaded into the EPROM through the procedure of programming.

The programming mode is entered when a voltage greater than 12.0, but less than 13.3 V is applied to the V_{PP} pin ($\overline{OE}/V_{PP}$ for 32K) and $\overline{CE}/\overline{PGM}$ is given a TTL-LOW pulse. The data to be programmed is applied 8 bits in parallel to the Data I/O (DQ_n) pins.

The flowchart (Figure 1) in the Programming section of this document shows the AMD-preferred interactive programming algorithm. Interactive algorithms requires less programming time than most other algorithms. This does not preclude the use of other algorithms, including the conventional 50-ms pulse, as long as the maximum specifications are not violated.

The AMD-preferred algorithm reduces programming time by using short (1 ms) program pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 15 pulses. This process is repeated while sequencing through each address of the EPROM. The interactive section of the algorithm is programmed and verified at $V_{CC} = 6.0$ V, ±5%.

The overprogram section of the algorithm programs the entire array by cycling through each address and applying an additional 2-ms program pulse. This section is done at $V_{CC} = 5.0$ V, ±5%.

After the final address is completed, the entire EPROM is verified to the data-sheet specifications of $V_{CC} = 5.0$ V, ±5%.

Auto Select Mode

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient-temperature range required when programming the EPROMs.

To activate this mode, the programming equipment must force 12.0 V ±0.5 V on address line A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Auto Select mode.

Byte 0 ($A_0 = V_{IL}$, $DQ_0 - DQ_7$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$, $DQ_0 - DQ_7$), the device identifier code. These identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the most significant bit (MSB), DQ_7, defined as the parity bit.

Read Mode

AMD EPROMs have two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

AMD EPROMs have a standby mode which reduces the active power dissipation up to 80%. The EPROM is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for: 1) low-memory power dissipation, and 2) assurance that output-bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array, and connected to the Read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs (including $\overline{OE}$ and V_{PP}) of the parallel EPROMs may be common. For the Am2716B, a LOW-level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROMs from being programmed. For the Am2732B, a HIGH-level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed.

Data for all the EPROMs should be verified t_{OE} after the falling edge of $\overline{OE}$, V_{PP} may remain at 12.5 V for the 2716B during program verify, but for the 2732B, $\overline{OE}/V_{PP}$ must be a TTL low level.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capaci-

tance loading of the device. A 0.1-μF ceramic capacitor (high-frequency, low-inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit-board traces on EPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

FUNCTION TABLES

TABLE 1. Am2716B MODE SELECT

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	V_{PP}	OUTPUTS
Read	L	L	X	V_{CC}	D_{OUT}
Output Disable	L	H	X	V_{CC}	Hi-Z
Standby	H	X	X	V_{CC}	Hi-Z
Program	L	H	X	V_{PP}	D_{IN}
Program Verify	L	L	X	V_{PP}	D_{OUT}
Program Inhibit	L	H	X	V_{PP}	Hi-Z
Auto Select	L	L	V_H	V_{CC}	Code

TABLE 2. Am2732B MODE SELECT

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	A_9	OUTPUTS
Read	L	L	X	D_{OUT}
Output Disable	L	H	X	Hi-Z
Standby	H	X	X	Hi-Z
Program	L	V_{PP}	X	D_{IN}
Program Verify	L	L	X	D_{OUT}
Program Inhibit	H	V_{PP}	X	Hi-Z
Auto Select	L	L	V_H	Code

Key: L = LOW
H = HIGH
X = Can be either LOW or HIGH
V_H = 12.0 V ±0.5 V

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Supply Voltage
with respect to Ground
on all Inputs except A_9 and V_{PP} ..... +6.25 to −0.6 V
on A_9 ..... +13.50 to −0.6 V
on V_{PP} ..... +13.50 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Notes: 1. For −105, −155, −205, blank, −305, and −455 versions, V_{CC} = +4.75 to +5.25 V.
2. For −100, −150, −200, −250, −300, and −450 versions, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, & 4)*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1	V
V_{IL}	Input LOW Voltage			−0.1	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 to +5.5 V			10.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to −5.5 V			10.0	μA
I_{CC1}	V_{CC} Standby Current for Am2716B (Note 6)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		25	mA
			E/M Devices		40	
	V_{CC} Standby Current for Am2732B		C, I, E, & M Devices		40	
I_{CC2}	V_{CC} Active Current for Am2716B and Am2732B	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	C, I, E & M Devices		100	mA
I_{PP1}	V_{PP} Program Current (Note 5)	V_{PP} = 5.5 V	C, I, E, & M Devices		30	mA
I_{PP2}	V_{PP} Read Current	V_{PP} = 5.5 V	C, I, E, & M Devices		5	mA

Notes: See notes following the Capacitance table on next page.

*See the last page of this spec for Group A Subgroup Testing information.

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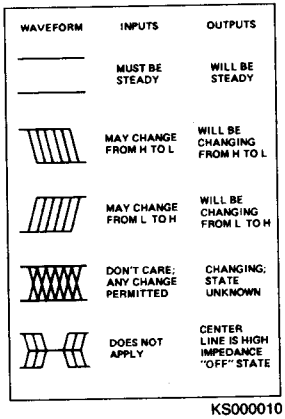
CAPACITANCE (Notes 2 & 3)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0$ V	4	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$ V	8	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0$ V	12	20	pF
C_{IN3}	$\overline{CE}/\overline{PGM}$ Input Capacitance		9	12	

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{CC}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The EPROMs must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
5. V_{PP} may be connected to V_{CC} directly except during programming. The supply would then be the sum of I_{CC} and I_{PP}.
6. I_{CC1} Max. is 40 mA for -4XX devices.

KEY TO SWITCHING WAVEFORMS



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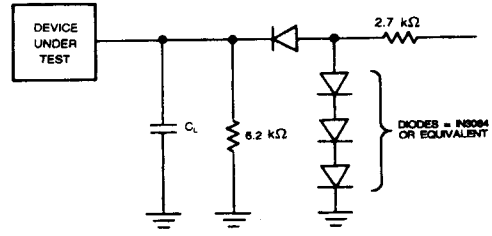
SWITCHING TEST CIRCUITS



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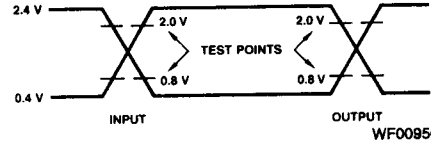
SWITCHING TEST WAVEFORMS



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AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.4 V for a logic "0". Input pulse rise and fall times are 5 ns.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Notes 1 & 3)

(Table 1 of 2)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	-105, -100		-155, -150		-205, -200		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		100		150		200	ns
2	t_{CE}	Chip Enable to Output Delay			100		150		200	ns
3	t_{OE}	Output Enable to Output Delay			75		75		75	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	60	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

(Table 2 of 2)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	Blank, -250		-305, -300		-455, -450		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		250		300		450	ns
2	t_{CE}	Chip Enable to Output Delay			250		300		450	ns
3	t_{OE}	Output Enable to Output Delay			100		110		150	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	80	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. Caution: The EPROMs must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C_L = 100$ pF,
Input Rise and Fall Times: ≤ 20 ns,
Input Pulse Levels: 0.45 to 2.4 V,
Timing Measurement Reference Level — Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V.

*See the last page of this spec for Group A Subgroup Testing information.

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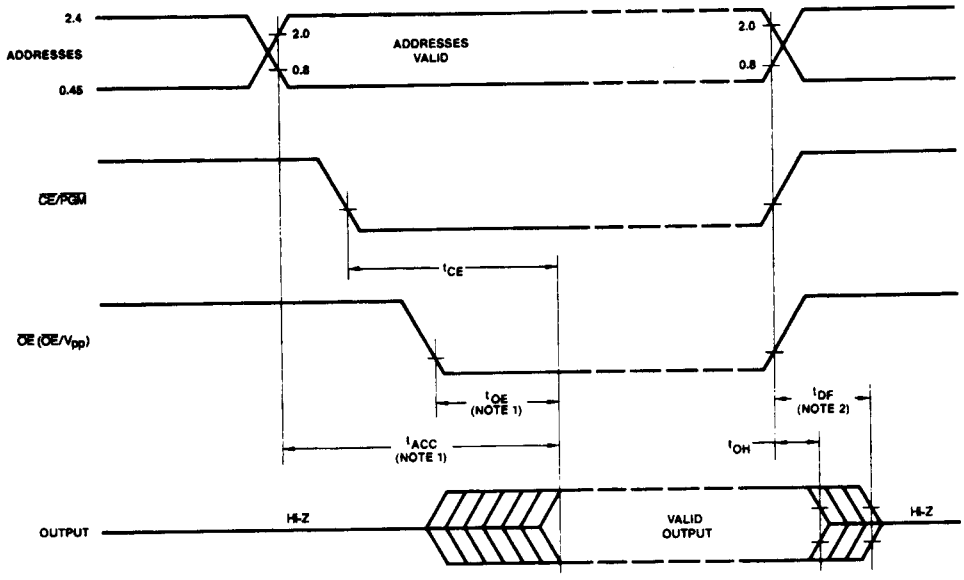
SWITCHING WAVEFORMS



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Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{OE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING

This section covers Identifier bytes, Interactive Flowcharts, and Interactive Programming Algorithms for DC Programming and Switching Programming Characteristics.

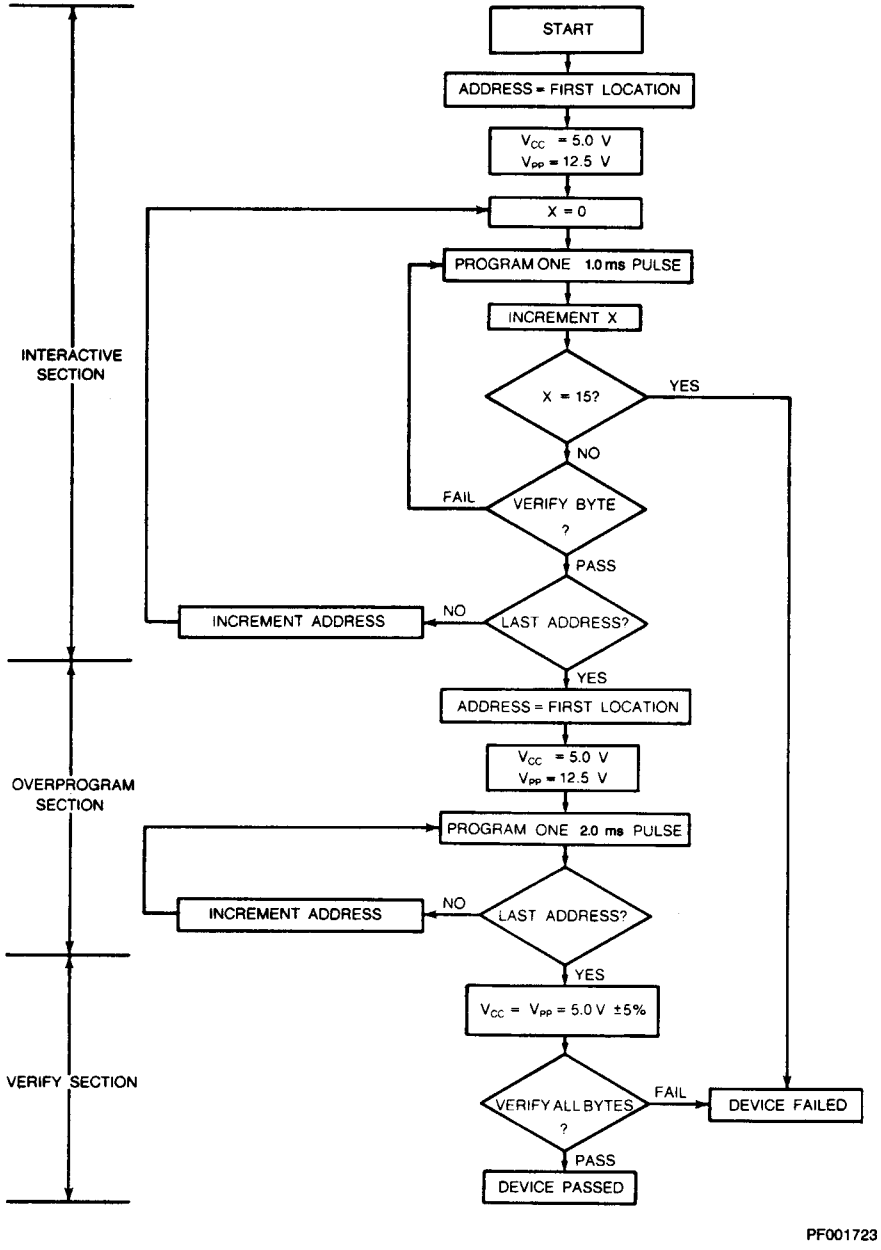


Figure 1. Interactive Programming Flow Chart

TABLE 4. IDENTIFIER BYTES

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Am2716B Device Code	V_{IH}	1	0	0	0	0	1	1	0	86
Am2732B Device Code	V_{IH}	0	0	0	0	0	1	1	1	07

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. All other Address Lines = $\overline{CE} = \overline{OE} = V_{IL}$

INTERACTIVE PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

(Notes 1, 2, and 4)

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Units
I_{LI}	Input Current (All Inputs)		$V_{IN} = V_{IL}$ or V_{IH}		10.0	μA
V_{IL}	Input LOW Level (All Inputs)			−0.1	0.8	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 1	V
V_{OL}	Output LOW Voltage during Verify		I_{OL} = 2.1 mA		.45	V
V_{OH}	Output LOW Voltage during Verify		I_{OH} = −400 μA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)	For Am2716B and Am2732B			100	mA
I_{PP1}	V_{PP} Supply Current (Program)		V_{PP} = 5.5 V		30	mA
V_{ID}	A_9 Auto-Select Voltage			11.5	12.5	V

Notes: See notes following the Interactive Programming Algorithm Switching Programming Characteristics table.

INTERACTIVE PROGRAMMING ALGORITHM SWITCHING PROGRAMMING CHARACTERISTICS

(Notes 1, 2, 3, and 4)

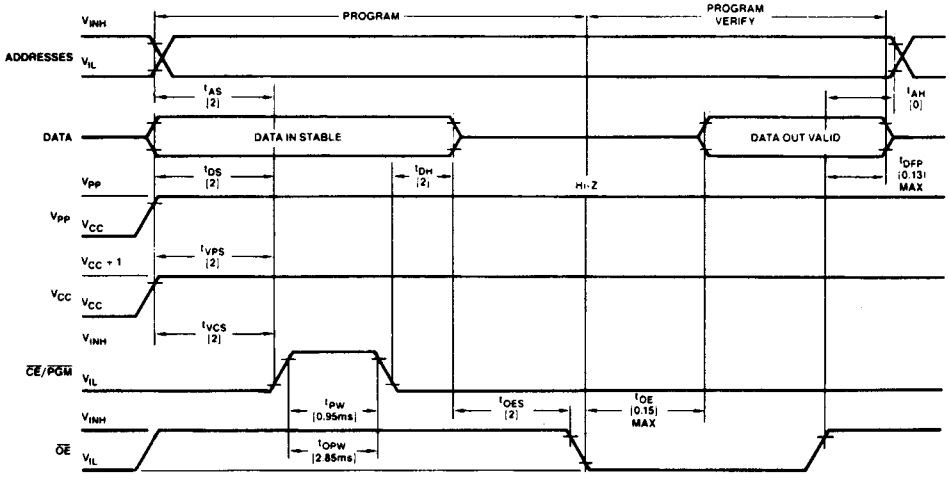
No.	Parameter Symbols	Parameter Description	Min.	Max.	Units
1	t_{AS}	Address Setup Time	2		μs
2	t_{OES}	$\overline{OE}$ Setup Time	2		μs
3	t_{DS}	Data Setup Time	2		μs
4	t_{AH}	Address Hold Time	2		μs
5	t_{DH}	Data Hold Time	2		μs
6	t_{DF}	Chip Enable to Output Float Delay	0	130	μs
7	t_{VPS}	V_{PP} Setup Time	2.0		μs
8	t_{VCS}	V_{CC} Setup Time	2		μs
9	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	.95	1.05	ms
10	t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width (Note 3)	1.9	55	ms
11	t_{CES}	$\overline{CE}$ Setup Time	2		μs
12	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes: 1. $T_A = +25°C \pm 5°C$; $V_{CC} = 6.0\ V \pm 0.25\ V$; $V_{PP} = 12.0$ to 13.3 V.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming the EPROMs, a 0.1-μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
4. Programming characteristics are guidelines which must be followed. They are not 100% tested to worst-case limits.

INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

AM2716B

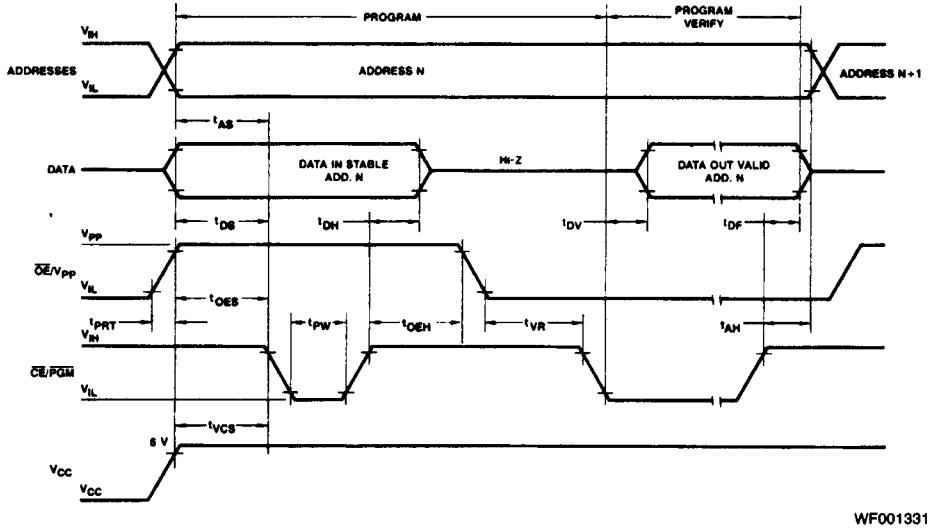
(Notes 1 and 3)



WF000583

Am2732B

(Notes 1 and 2)



WF001331

Notes: 1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DF} are characteristics of the device, but must be accommodated by the programmer.
3. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

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GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups*
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{PP1}	1, 2, 3
I_{PP2}	1, 2, 3
C_{IN}	4
C_{OUT}	4
C_{IN2}	4
C_{IN3}	4

*For DC Programming Characteristics, only Subgroup 1 applies.

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11
2	t_{CE}	9, 10, 11
3	t_{OE}	9, 10, 11
4	t_{DF}	9
5	t_{OH}	9

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.