LOW POWER DIGITAL UHF PAGING RECEIVER

GENERAL DESCRIPTION

The UAA2050T is a very low power UHF and VHF radio receiver circuit, primarily intended for use in paging receivers (27 MHz to 470 MHz) for wide-area digital paging systems employing direct FM non-return-to-zero (NRZ) frequency-shift keying (FSK) modulation.

Used in conjunction with the PCA5000T decoder for POCSAG paging systems, it offers an extremely advanced radio paging concept.

The radio receiver design is based on the offset receiver principle. The receiver provides fully filtered and squared data to drive the decoder and can be turned off completely by external inputs.

Features

- Low noise preamplifier ensuring high RF sensitivity
- Few external components required
- Low current consumption
- Wide operating supply voltage range
- Power on/off mode selectable via the enable input (RE)
- Low battery voltage detector
- Crystal controlled receiver frequency (AFC)
- Fully compatible with all FSK modulated systems (512 and 1200 bits/s)
- Uses low cost crystal

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage range		$V_P = V_{7-15}$	1.9	–	3.5	V
Supply voltage for preamplifier		$V_{23,24-15}$	1.0	–	3.5	V
Total supply current		I_{tot}	2.25	–	3.76	mA
Supply current OFF		$-I_{OFF}$	–	–	1.0	µA
RF sensitivity (RMS value)	1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
Preamplifier noise figure	note 1; f = 470 MHz	NF	–	4.5	–	dB
Operating ambient temperature range		T_{amb}	−10	–	+70	°C

Note to the Quick reference data

1. Including the transforming network.

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

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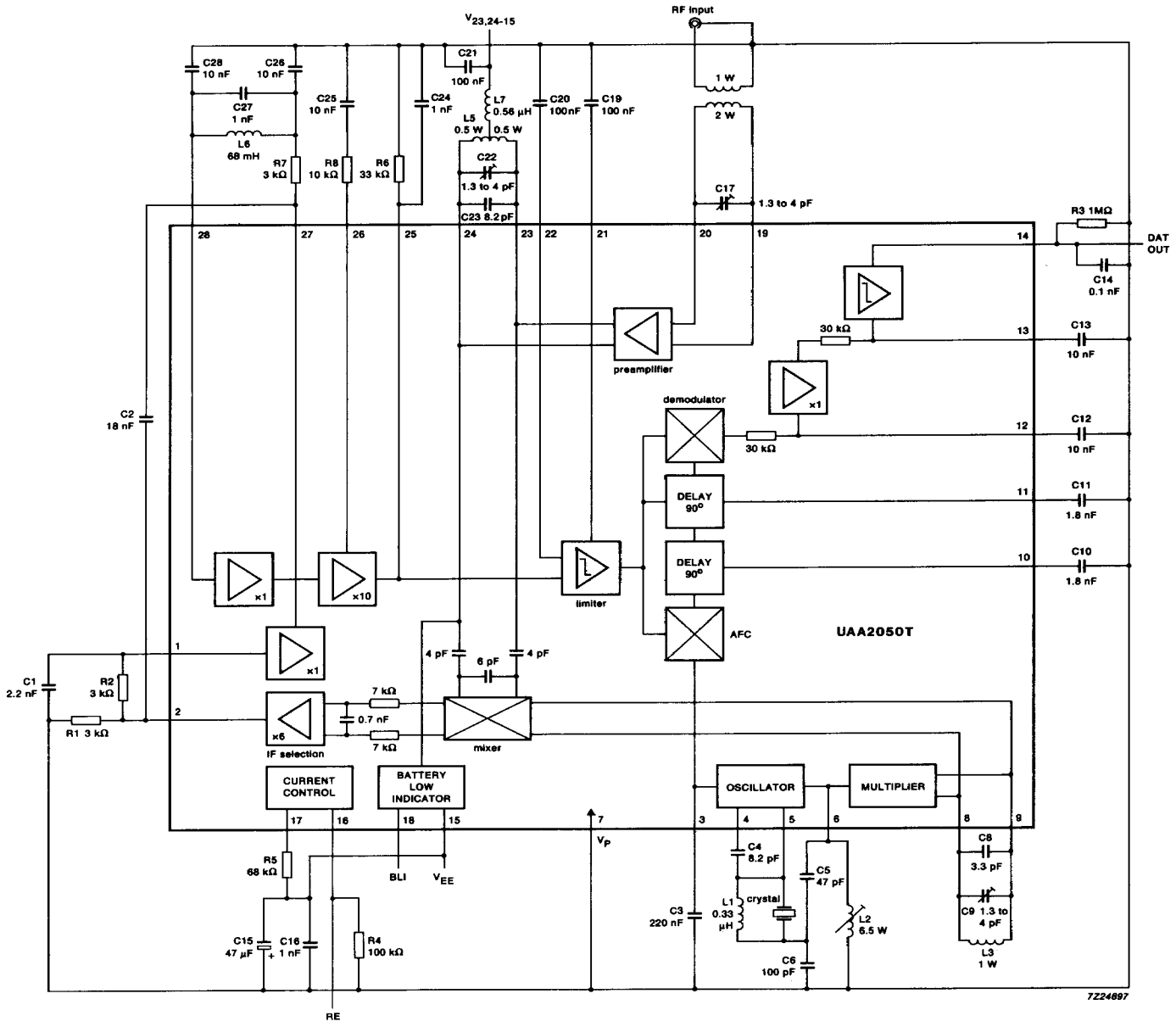


Fig.1 Block diagram (showing UHF external components).

DEVELOPMENT DATA

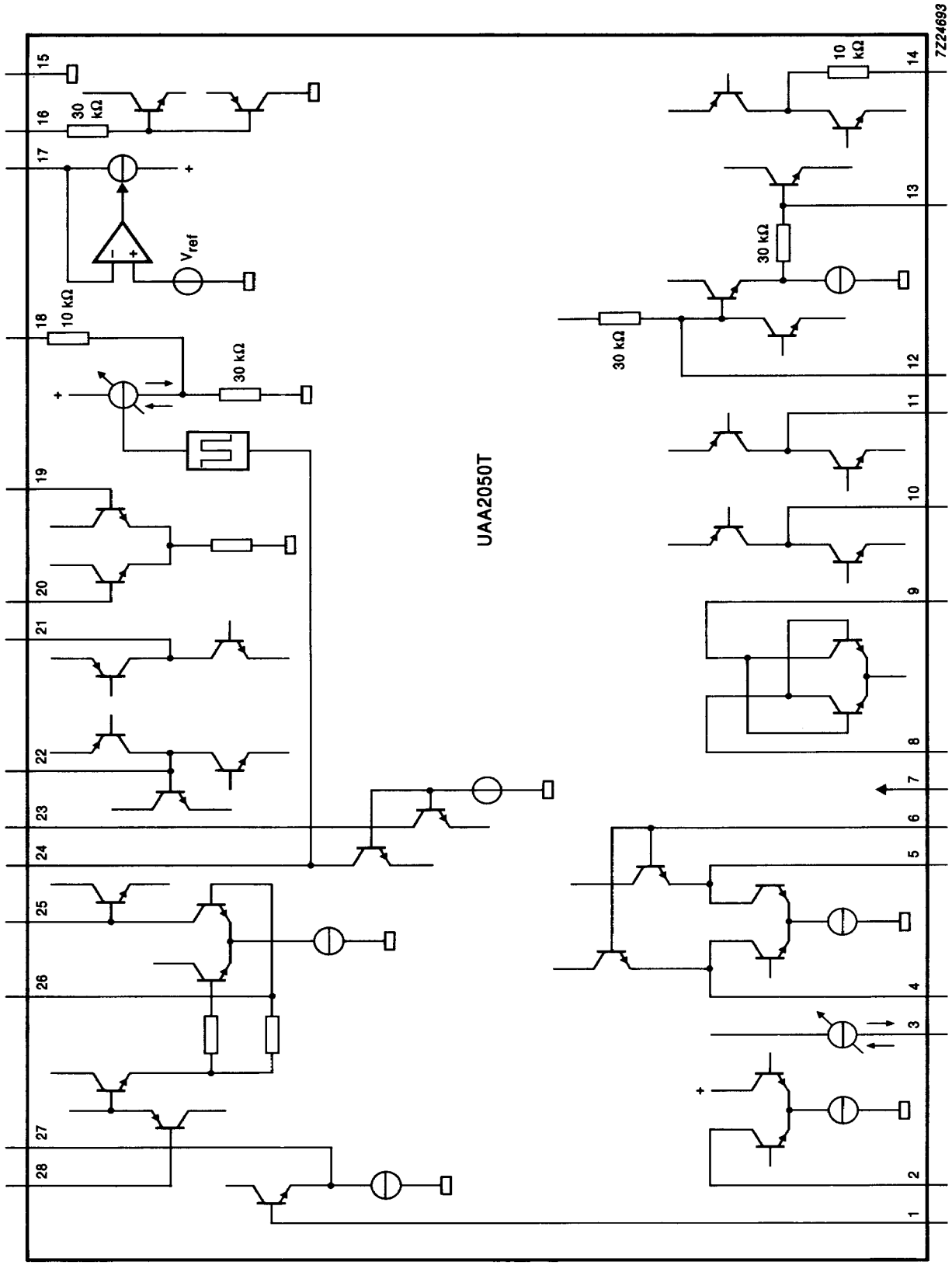


Fig.2 Pinning diagram and equivalent circuits.

PINNING

pin	mnemonic	description
1	IFF2	IF filter 2
2	IFF1	IF filter 1
3	AFC	AFC (test point 1)
4	OSC IN	oscillator input
5	OSC AFC	oscillator AFC range
6	OSC OUT	oscillator output
7	V_P	supply voltage (positive)
8	MC1	multiplier coil
9	MC2	multiplier coil
10	AFCD	AFC delay
11	DEMODD	demodulator delay
12	DAT F1	data filter 1
13	DAT F2	data filter 2
14	DAT OUT	data output
15	V_{EE}	supply voltage (negative)
16	RE	receiver enable input
17	CC	current control input
18	BLI	battery low indicator output
19	PREAMP1	preamplifier input 1
20	PREAMP2	preamplifier input 2
21	LC2	limiter decoupling 2
22	LC1	limiter decoupling 1
23	MIX1	mixer input 1 (preamplifier output)
24	MIX2	mixer input 2 (preamplifier output)
25	LIM IN	limiter input (test point 2)
26	IFF5	IF filter 5
27	IFF3	IF filter 3
28	IFF4	IF filter 4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	condition	symbol	min.	max.	unit
Supply voltage		$V_P = V_{7-15}$	−0.3	+5.0	V
Supply voltage for preamplifier		$V_{23,24-15}$	−0.3	+5.0	V
Operating ambient temperature range		T_{amb}	−10	+70	°C
Storage temperature range		T_{stg}	−55	+125	°C
Electrostatic handling; human body model*	except pins 19 and 20	V_{ESD}	−1000	+1000	V
	only pins 19 and 20	V_{ESD}	−500	+1000	V

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4; L2 and L3 short-circuited; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{7-15}$	1.9	2.0	3.5	V
Supply voltage for preamplifier	$V_{23,24-15} \leqslant V_P$	$V_{23,24-15}$	1.0	1.1	3.5	V
Supply current	$V_{RE} \geqslant V_P - 0.6$ V	I_7	1.9	2.5	3.2	mA
Supply current for preamplifier	$V_{RE} \geqslant V_P - 0.6$ V	$I_{23,24}$	0.35	0.45	0.56	mA
Supply current OFF	$V_{RE} \leqslant 0.4$ V	I_{OFF}	–	–	1.0	µA
Receiver enable (RE)						
POWER-OFF MODE:						
input voltage		$V_{RE} = V_{16-15}$	–	–	0.4	V
input current	V_{RE} = 0.4 V	I_{16}	–	–	1.0	µA
POWER-ON MODE:						
input voltage		$V_{RE} = V_{16-15}$	$V_P - 0.6$ V	–	–	V
input current	V_{RE} = 1.4 V	I_{16}	–	1.0	5.0	µA
Data output (DAT OUT)						
Output voltage HIGH	$I_{14} = \pm 10$ µA	V_{14-15}	$V_P - 0.7$ V	–	–	V
Output voltage LOW	$I_{14} = \pm 10$ µA	V_{14-15}	–	–	0.5	V
Battery voltage low indicator						
Detection voltage	see Fig.3	V_{DET} V_{DET}	1.10 1.90	1.17 2.00	1.24 2.10	V V
Output voltage HIGH	1.0 V ⩽ V_{24-15} ⩽ 1.10 V; 1.85 V ⩽ V_{24-15} ⩽ 1.90 V; $I_{18} = \pm 7$ µA	V_{OH}	$V_P - 0.5$ V	–	–	V
Output voltage LOW	1.24 V ⩽ V_{24-15} ⩽ 1.65 V; 2.10 V ⩽ V_{24-15}; $I_{18} = \pm 7$ µA	V_{OL}	–	–	0.5	V

Note to the DC characteristics

1. V_{18-15} goes HIGH if V_{24-15} is less than V_{DET}.

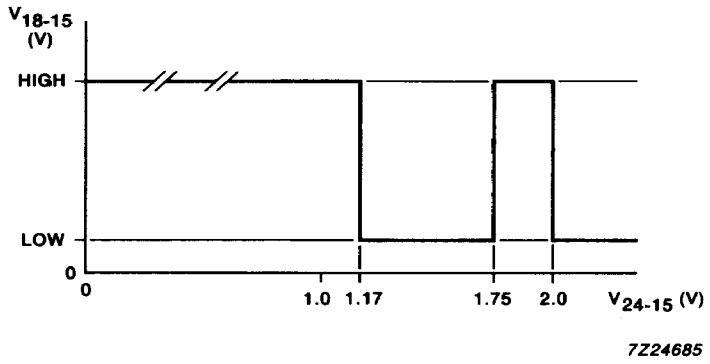


Fig.3 Typical battery low indicator thresholds.

DEVELOPMENT DATA

AC CHARACTERISTICS (UHF)

For AC test procedures refer to section 'TEST INFORMATION'. V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4 and printed-circuit board layout as Fig.7; test signal: f = 469.200 MHz: deviation = ±4.5 kHz: modulation = 256 Hz rectangular; channel spacing = 25 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
UHF sensitivity range (RMS value)	note 1; 1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
		EMF/2	–	−122	−119	dBm
	T_{amb} = −10 to +70 °C	EMF/2	–	–	−116	dBm
Adjacent channel selectivity		αa	60	67	–	dB
	T_{amb} = −10 to +70 °C	αa	50	–	–	dB
Co-channel selectivity		αc	8	–	–	dB
Spurious response rejection		αs	55	58	–	dB
Intermodulation response		IM	50	60	–	dB
Blocking	Δf ≥ ±4 MHz	EMF	80	83	–	dBµV
AFC lock-in range		±Δf	3	–	–	kHz
Preamplifier	see Fig.9					
Noise Figure	note 2	NF	–	4.5	–	dB
Third order intercept point		IP3	–	−20	–	dBm
Available power gain		G_p	–	6	–	dB
1 dB compression point (RMS value)		EMF/2	–	10	–	mV
VHF RF sensitivity range (RMS value)	see Fig.10; f = 173.95 MHz; 1 x 10^{-2} bit error rate	EMF/2	–	0.14	–	µV
		EMF/2	–	−124	–	dBm

Notes to the AC characteristics

1. A simple digital method of performing an approximate bit error rate (BER) measurement with a counter is shown in Fig.5. At high signal levels (10 µV) the counter should read the exact frequency of the data input to the signal generator (256 Hz). As the signal level is reduced, errors occur at the receiver output and effectively changes the output frequency read by the counter (error duration is nearly always less than one bit length).
   The input signal level (V_{ref}) is reduced until the bit error rate is ≤ 1 x 10^{-2} (5 bit errors for 512 bit/s system). The frequency from the data output signal will change from 256 Hz (512 bit/s system) to 261 Hz. This RF-level is the reference for the following tests (V_{ref}).

2. Including the transforming network.

TEST INFORMATION

Tuning procedure for AC tests

1. After performing the DC tests, prepare the device for AC testing (as shown in Fig. 4).

2. Connect pin 3 to a voltage source of $V_{3-7} = -0.5$ V. Measure the multiplier frequency with a counter or spectrum analyzer connected to the link winding of L3. Tune L2 to set the crystal oscillator to a frequency of:

   $$\frac{\text{Received frequency} + 2.2\ \text{kHz}}{5} \quad (\pm 100\ \text{Hz})$$

   For a received frequency of f = 469.200 MHz, the oscillator frequency (f_{OSC}) = 93.840 MHz.

3. Remove the test voltage source and turn on the signal generator (f = 469.200 MHz; deviation = ±4.5 kHz; rectangular 256 Hz modulation; RF input level = 1 mV).

   Note During the following tests the RF signal generator level should be reduced as the receiver is tuned, to ensure the peak-to-peak output voltage at pin 25 lies between 20 mV and 100 mV.

4. Tune C9 (multiplier) to obtain a peak audio output voltage on pin 25.

5. Tune C22 (Mixer input) to obtain a peak audio output voltage on pin 25.

6. Disconnect the frequency counter from the multiplier output. Measure the voltage at pin 3 and check if it is within the range of −0.48 V to −0.52 V. If it is outside this range then adjust L2 (oscillator) until it is within the limits.

7. Check with an oscilloscope that clean data is appearing on the data output (pin 14) and proceed with the AC tests.

DEVELOPMENT DATA

Test conditions

The data output signal corresponds to the sensitivity definition.

Where:

f_1 is the modulated test signal
f_2 is the unmodulated test signal
f_{cs} is the channel spacing (25 kHz)
V_1 is the signal generator 1 output
V_2 is the signal generator 2 output
V_{ref} is defined in 'Notes to the AC characteristics'.

1. Adjacent channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3dB$
   - generator 2: unmodulated test signal; $V_2 = V_1 + 60$ dB ($f_2 = f_1 \pm \Delta f_{cs}$).

2. Co-channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 - 8$ dB ($f_2 = f_1 \pm 3$ kHz maximum).

3. Spurious response rejection (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 + 55$ dB (f_2 =100 kHz to 1 GHz; $|f_2 - f_1| \geq 2\Delta f_{cs}$).

4. Intermodulation response (see Fig.6);
   - generator 1: modulated test signal; $f_1 = 469.2$ MHz $\pm 2 \times n \times \Delta f_{cs}$) n = 1 to 4 .
   - generator 2: unmodulated test signal; $f_2 = 469.2$ MHz $\pm n \times \Delta f_{cs}$). n = 1 to 4.

   Output voltages of both generators increase with the same level, until a data output signal corresponding to the sensitivity definition is reached. The level must be 50 dB above the V_{ref} + 3 dB level.

5. Blocking (see Fig.6);
   - generator 1: modulated test signal; V_1 (EMF) = 3 dBμV
   - generator 2: unmodulated test signal; V_2 (EMF) = 80 dBμV ($f_2 = f_1 \pm \Delta f$; $\Delta f \geq 4$ MHz)

6. AFC lock-in-range (see Fig.5);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB ($f_1 = 469.2$ MHz ±3 kHz)

DEVELOPMENT DATA

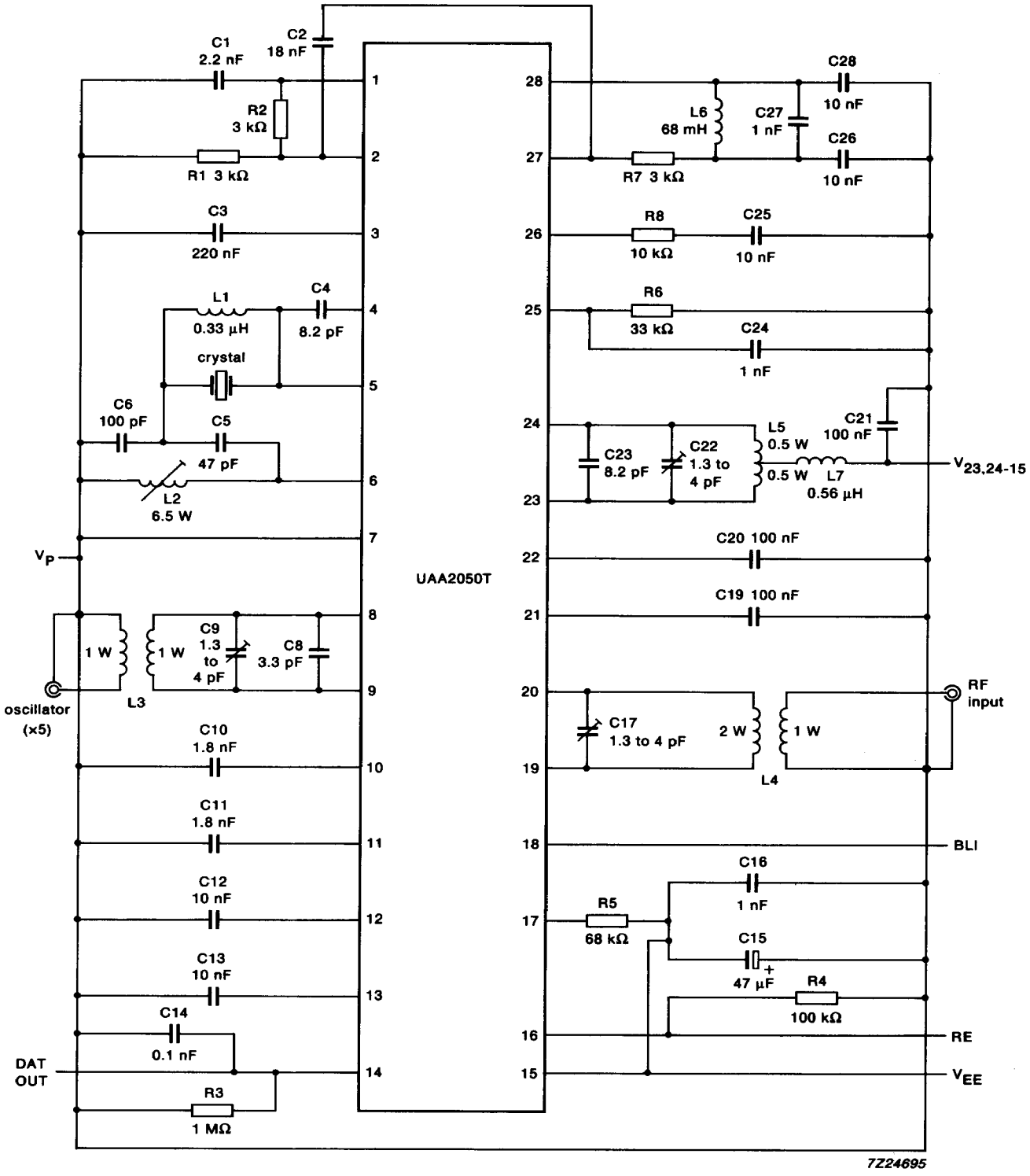


Fig.4 Test circuit (UHF).

Crystal data

Test frequency for the receiver chip is 469.2 MHz, crystal frequency is 93.838 MHz.

Static capacitance C0 (max.) = 4 pF
Dynamic capacitance C1 = 0.4 fF ±20%
Dynamic resistance R1 (max.) = 75 Ω
Temperature drift = $\pm 5 \times 10^{-6}$.

Inductors

L3, L4 and L5: wound with 0.9 mm silvered wire, without pot or core and diameter of 4.5 mm.

L1 = 0.33 µH chip inductor (at 25 MHz minimum value of Q = 12)
L2 = 6.5 turns
L3 = 1 turn
L4 = 2 turns
L5 = 1 turn
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)

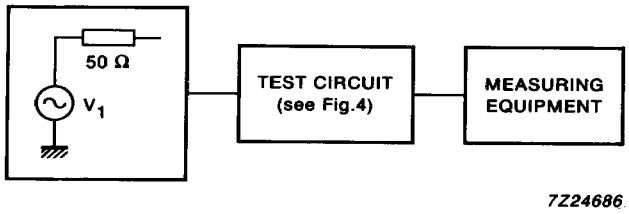


Fig.5 Test figure A.

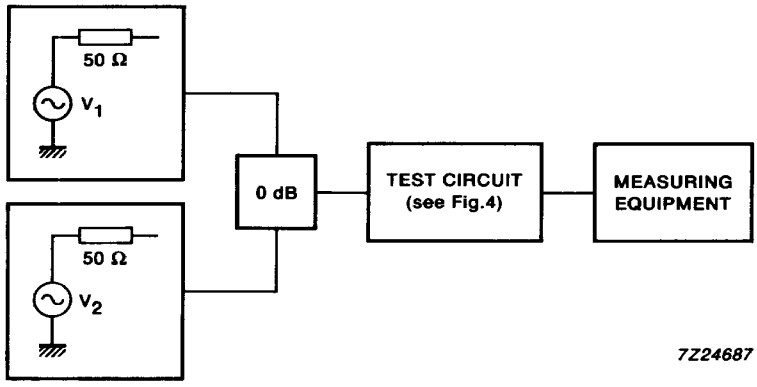
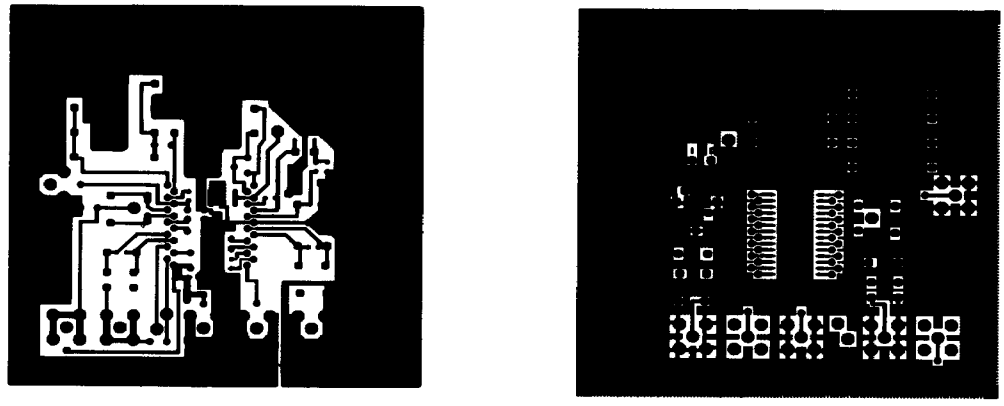


Fig.6 Test figure B.



(a) underside

(b) top side

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Fig. 7 Printed-circuit board for UHF range (see Fig.4).

DEVELOPMENT DATA

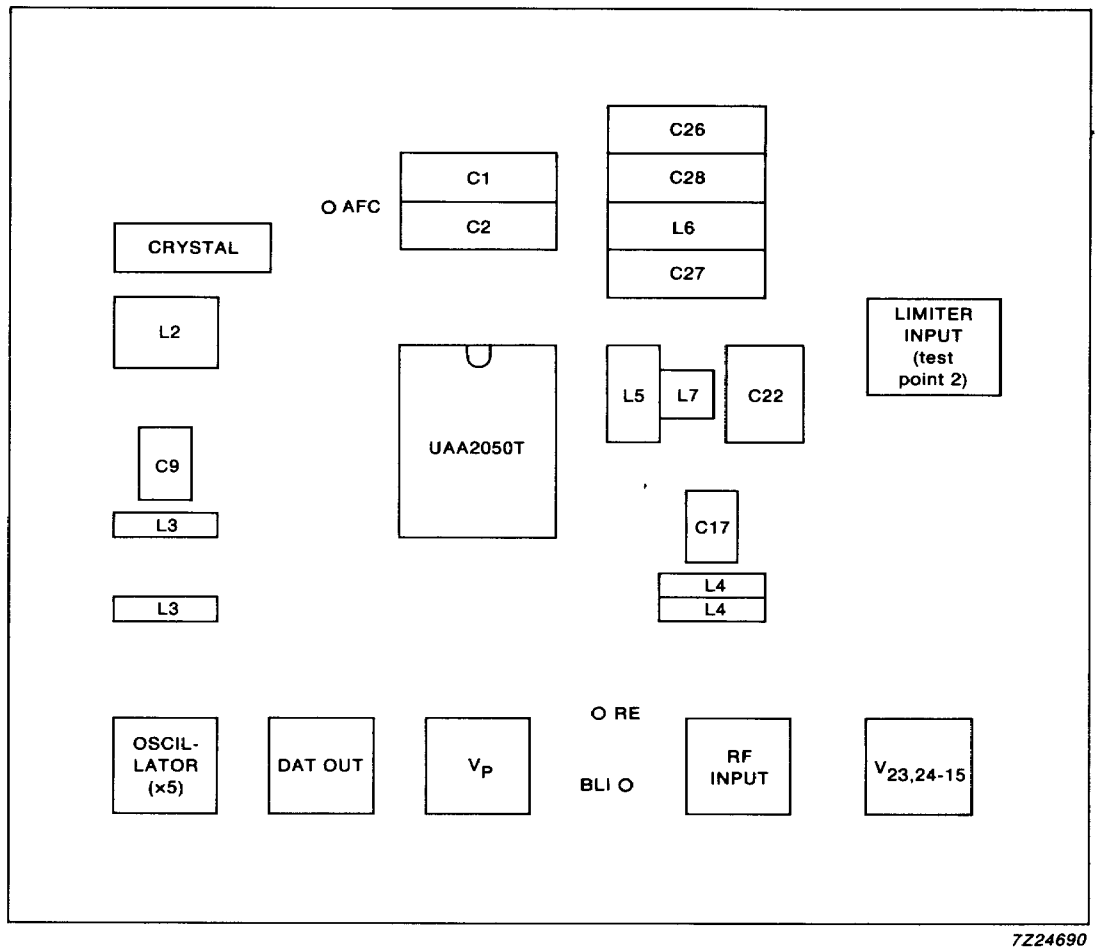


Fig. 8 Printed-circuit board for UHF range (component arrangement).

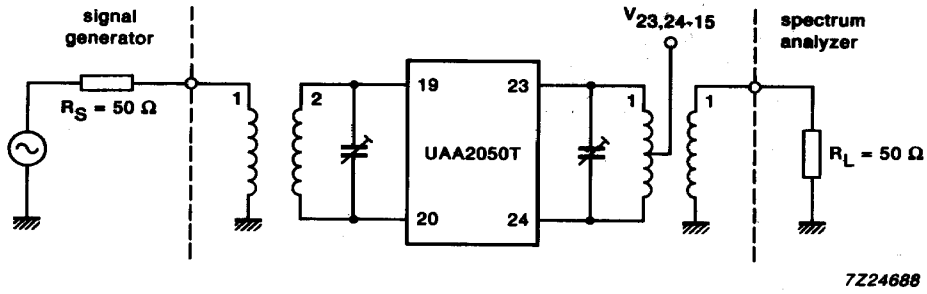


Fig.9 Test circuit for the preamplifier.

DEVELOPMENT DATA

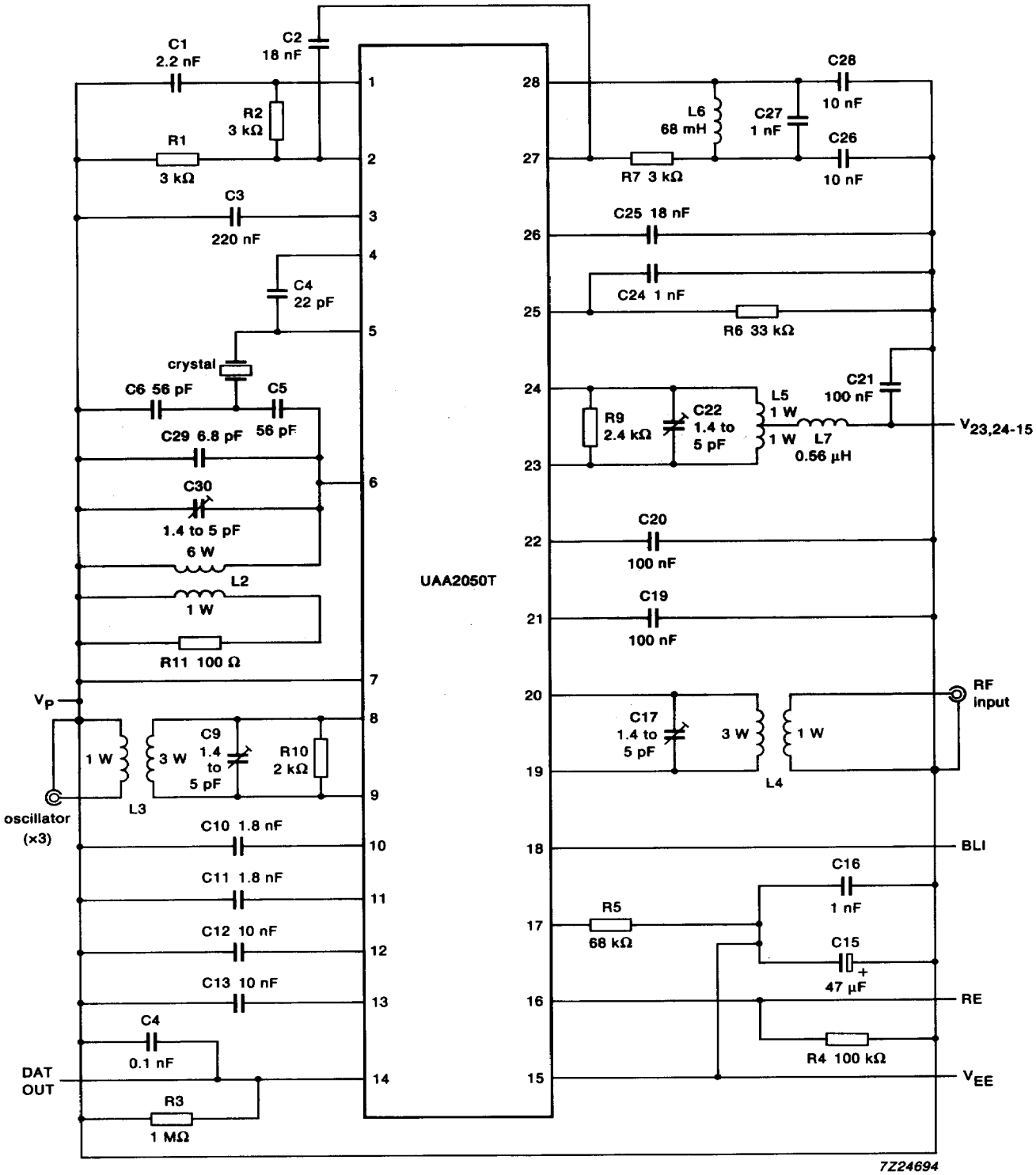


Fig.10 Test circuit (VHF).

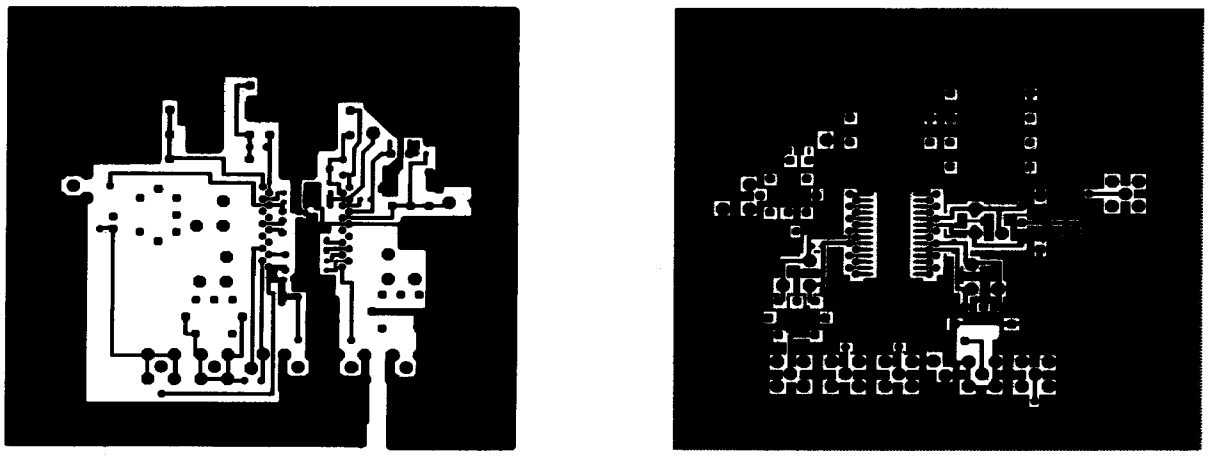
Crystal data

Test frequency for the receiver chip is 173.95 MHz, crystal frequency is 57.9859 MHz.

Inductors

L2, L3, L4 and L5: wound with 0.3 mm enamelled copper wire on Toko 4.5 mm diameter former, without pot or core. Screening cans are also used.

L2 = 6 turns, 2 turns per groove; link winding, 1 turn over the centre of the other winding
L3 = 3 turns, 1 turns per groove; link winding, 1 turn at the bottom of the former
L4 = 3 turns, 1 turns per groove; link winding, 1 turn at the centre of the other winding
L5 = 2 turns
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)



(a) underside

(b) top side

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Fig. 11 Printed-circuit board for VHF range (see Fig.10).

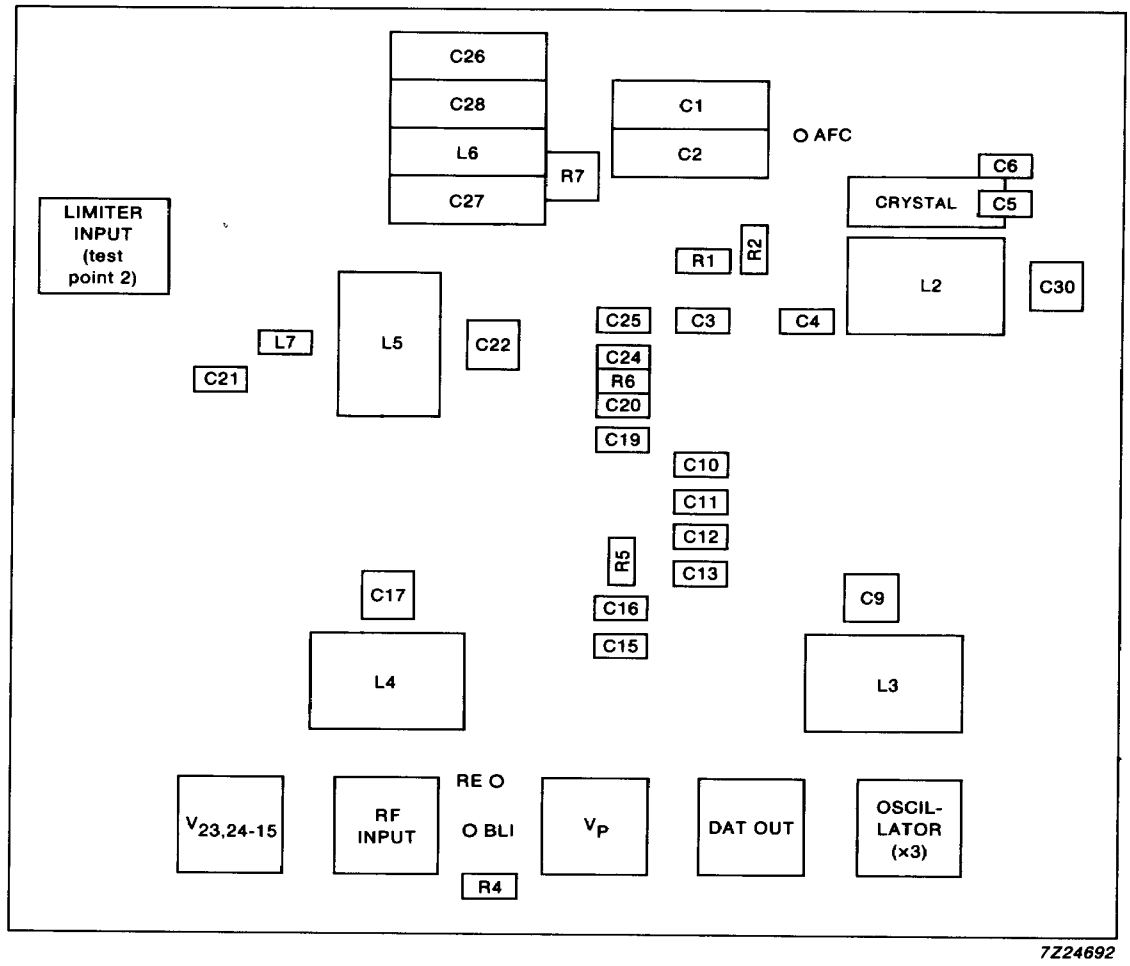


Fig. 12 Printed-circuit board for VHF range (component arrangement).

DEVELOPMENT DATA

APPLICATION INFORMATION

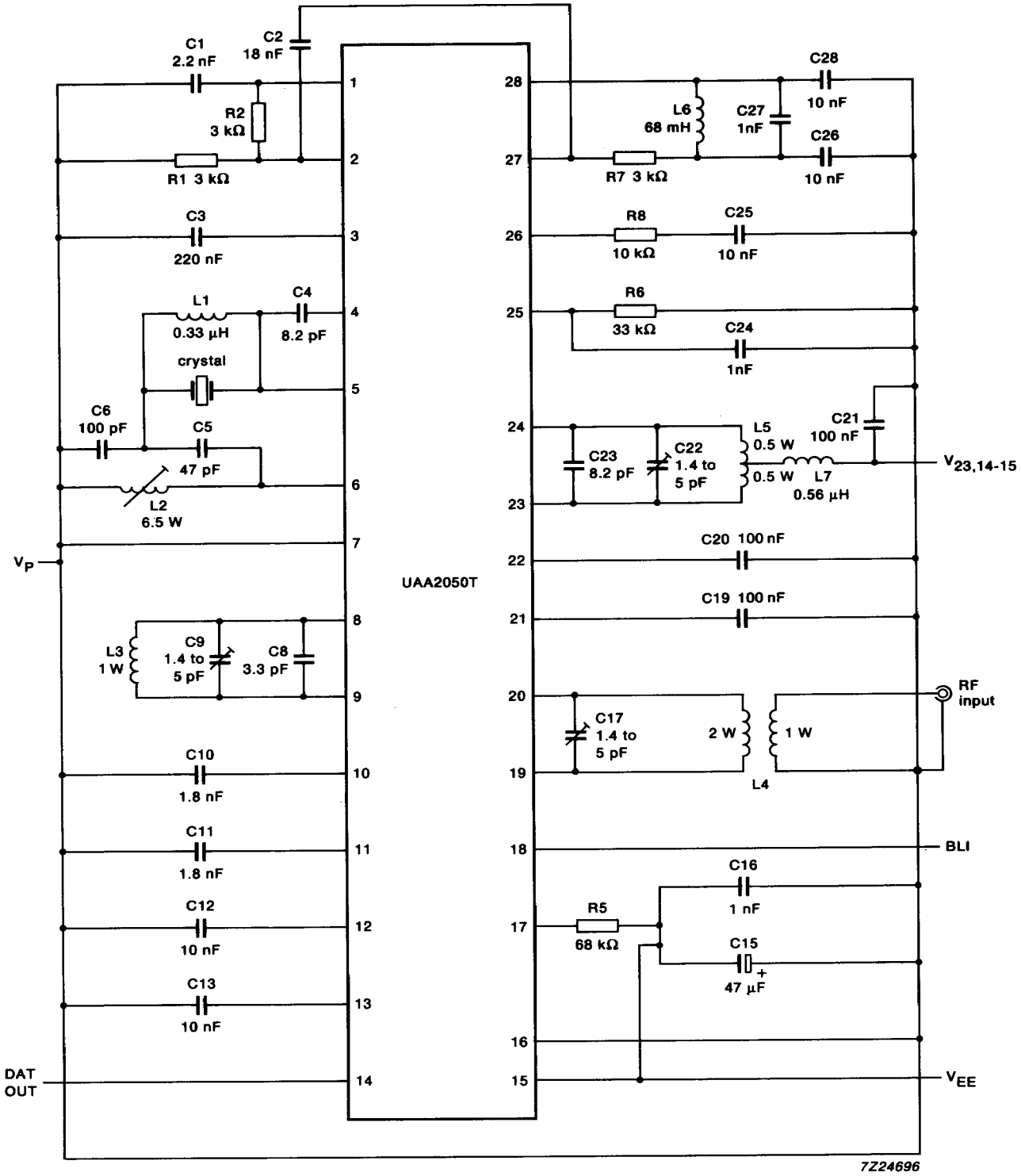
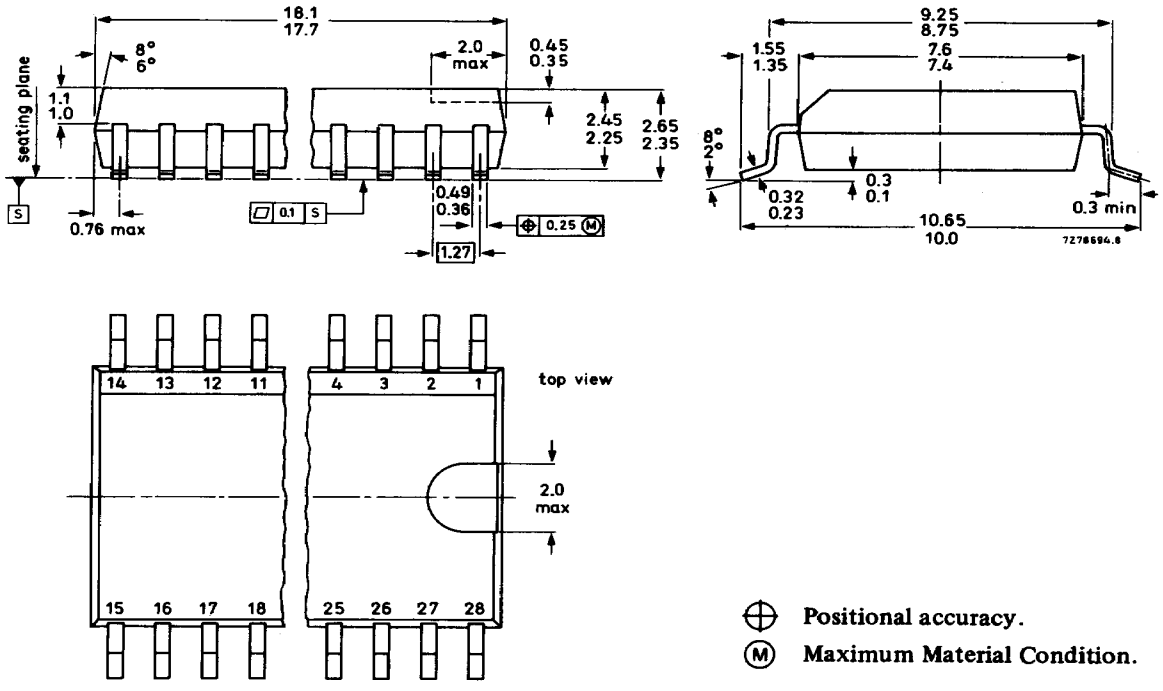


Fig.13 Application diagram (UHF).

Note to Fig.13

For information concerning the crystal oscillator and inductors, refer to Fig.4.

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



Dimensions in mm

DEVELOPMENT DATA

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.