TOSHIBA ASIC

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

TC11L CMOS Gate Array 1.5 micron
TC14L CMOS Gate Array 1.0 micron

These two gate array families provide a unique solution for designs which have a high ratio of pin count to gates. Toshiba's optimized assembly technology allows the use of smaller die sizes in traditional plastic and ceramic flat packs–thus providing a silicon efficient solution for pad limited designs. Applications include any low gate count, high pin count design (for example, peripheral interfaces and 32- and 64-bit bus applications).

Fast-turnaround ASICs, efficient tools, service and engineering support enable you to meet aggressive product introduction schedules.

- The Toshiba Design Environment embraces popular EWS and CAE systems such as: AIDA™, Cadence, Dazix, HILO™, HP, IKOS™, Mentor, Synopsys, Valid, Verilog-XL™ and Viewlogic™
- Comprehensive cell libraries with helpful utilities for all product families
- Logic synthesis capability supported through Synopsis
- Design interface thru hardware description language
- Design for test features include support for SCAN: AIDA, JTAG, Toshiba scan bureau service
- Design assistance through local design centers which are supported by U.S. headquarters in Sunnyvale, CA
- Flexibility in design services and interface

TC11L, 1.5µm CMOS

- 300, 500 and 700 usable gates
- 0.6ns typical delay
- 44 pads
- Through hole and surface mount packaging
  - 16 to 42 pin DIP
  - 24, 28 SOP
  - 44 PLCC
  - µ44 QFP
- Compatible with the TC110G "parent family"
  - Process technology
  - Internal gate delays
  - Tested, verified cell libraries

TC14L, 1.0µm CMOS

- 1K, 2K, 4K, 5K, 6K, 7K, 8K,10K usable gates
- 0.4ns typical delay
- From 100 to 208 pads
- Through hole and surface mount packaging
  - 84 PLCC
  - 120, 144, 160, 176, 184, 208 QFP
  - 80, 100 RFP
- Compatible with the TC140G "parent family"
  - Process technology
  - Internal gate delays
  - Tested, verified cell libraries

Part number	Estimated max. useable gates (1)	Maximum pads (2)
TC11L003	300	44
TC11L005	500	44
TC11L007	700	44
TC14L010	1,000	100
TC14L020	2,000	100
TC14L040	4,000	160
TC14L050	5,000	160
TC14L060	6,000	176
TC14L070	7,000	176
TC14L080	8,000	208
TC14L100	10,000	208

Notes: 1. If the useable number of gates is exceeded, contact your local Design Center.
2. Additional I/O pads may be configured as VDD/VSS, subject to the number and drive of the output buffers.

Package Availability

Package		Part No.	TC11L series			TC14L series							
			003	005	007	010	020	040	050	060	070	080	100
DIP		16	A*	A*	A*								
		18	A*	A*	A*								
		24	A*	A*	A*								
		28	A*	A*	A*								
		40	A*	A*	A*								
		42	A*	A*	A*								
		S42	A*	A*	A								
SOP		24	A	A	A								
		28	A	A	A								
PLCC		44	A*	A*	A*								
		84				A*	A*						
PFP	Square	μ44	A	A	A								
		120						A*	A*				
		144						A*	A*	D	D		
		160						A	A	D	D	D	D
		176								D	D	D	D
		184										D	D
		208										D	D
	Rectangular	80				A*	A*						
		100				A	A						

Remarks: A — Available

A*— Confirm schedule of availability with your Toshiba design center

D — Under development (release schedule: 4Q90)

Pin Arrangement Restrictions

TC11L Series

A no connect pin may be required for every I/O cell that uses more than one I/O slot, or internal cells that use an I/O slot.

TC14L Series

1. A no connect pin may be required for an internal cell that uses an I/O slot..
2. Depending on the part number and package combination, there are pins to which bidirectional or tri-state output buffers cannot be assigned.

Part number	Package	Pins for which bidirectional and tri-state are not allowed	Pins for which bidirectional is not allowed
TC14L010/020	FP100	No. 53, No. 78	No. 3, No. 28
TC14L040/050	FP160	No. 81, No. 121	No. 1, No. 41

a) There is no restrictions for TC14L010/020: FP80, TC14L040/050: FP120, FP144.
b) The above restrictions do not apply to the TC11L series.

Absolute Maximum Ratings (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	– 0.3 to +7.0	V
V_{IN}	DC input voltage	– 0.3 to V_{DD} +0.3	V
I_{IN}	DC input current	± 10	mA
T_{stg}	Storage temperature	– 40 to +125	°C

Recommended Commercial Operating Conditions (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	4.75 to 5.25	V
T_a	Ambient temperature	0 to +70	°C

DC Electrical Characteristics

Specified at V_{DD} = 5V ±5%, ambient temperature 0 to +70°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage					V
	TTL level		2.2			
	TTL level SCHMITT trigger		2.2			
	CMOS level		3.5			
	CMOS level SCHMITT trigger		4.0			
V_{IL}	Low level input voltage					V
	TTL level				0.8	
	TTL level SCHMITT trigger				0.8	
	CMOS level				1.5	
	CMOS level SCHMITT trigger				1.0	
I_{IH}	High level input current	$V_{IN} = V_{DD}$	– 10		10	µA
	Input buffer with pull-down	$V_{IN} = V_{DD}$	10		200	
I_{IL}	Low level input current	$V_{IN} = V_{SS}$	– 10		10	µA
	Input buffer with pull-up	$V_{IN} = V_{SS}$	– 200		– 10	
V_{OH}	High level output voltage					V
	Type B1	I_{OH} = – 1mA	2.4			
	Type B2	I_{OH} = – 2mA	2.4			
	Type B4	I_{OH} = – 4mA	2.4			
	Type B6	I_{OH} = – 6mA	2.4			
	Type B8	I_{OH} = – 8mA	2.4			
	Type B12(2)	I_{OH} = – 12mA	2.4			
	Type B16(2)	I_{OH} = – 16mA	2.4			
		I_{OH} = – 1µA	V_{DD} – 0.05			
V_{OL}	Low level output voltage					V
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA			0.4	
	Type B4	I_{OL} = 4mA			0.4	
	Type B6	I_{OL} = 6mA			0.4	
	Type B8	I_{OL} = 8mA			0.4	
	Type B12(2)	I_{OL} = 12mA			0.4	
	Type B16(2)	I_{OL} = 16mA			0.4	
		I_{OL} = 1µA			V_{SS} + 0.05	
I_{OZ}	High impedance leakage current		– 10		10	µA
	Output buffer with pull-up	$V_{OUT} = V_{DD}$ or V_{SS}	– 200		– 10	
	Output buffer with pull-down	$V_{OUT} = V_{DD}$ or V_{SS}	10		200	
I_{DD}	Quiescent supply current	$V_{IN} = V_{DD}$ or V_{SS}			100(3)	µA

Note: (1) Usage restrictions. TC14L series: output is allowed up to B12, bidirectional is allowed up to B6

(2) TC11L series: requires two output pads.

(3) Customer-design dependent.

(4) TTL SCHMITT trigger only available on TC14L.

ASIC | TC11L & TC14L CMOS GATE ARRAYS

Library

TC11L series
Internal cells and I/O buffers are fully compatible with the TC110G sereis.

TC14L series
Internal cells and I/O buffers are compatible with the TC140G sereis.

Macrocells

Function	Types	
	TC11L	TC14L
Logic gate	62	62
Inverter/internal buffer	22	23
Tri-state internal buffer	6	6
Delay buffer	6	6
Latch	21	21
Flip-flop	50	50
Decoder	8	8
Multiplexer	14	14
Adder	6	6
Input buffer	63	36
Output buffer	48	32
Bidirectional buffer	520	462
Oscillator	10	6
Total	**836**	**732**

Macrofunction List

Function	Types	
	74HC Series Compatible	Other
Adder	1	4
Comparator	2	6
Counter	11	19
Decoder	4	10
Flip-Flop	6	—
Gate	16	—
Multiplexer	10	11
Register	16	19
Other	7	8
Total	**73**	**77**

Library Restrictions

TC14L series

1. Internal cells and input buffer cells are both compatible with those of the TC140G Series. Clock drivers (such as DRVC4) cannot be used, however.
2. The following restrictions apply to output and bidirectional buffers.
   a) Output buffer: B1, B2, B4, B6, B8, and B12 are available.
   Output buffers with slew rate control are available.
   b) Tri-state output buffer: BT1, BT2, BT4, BT6, BT8, and BT12 are available.
   Tri-state output buffers with open drain, open source and slew rate control are available.
   c) Bidirectional buffer: BD1, BD2, BD4, and BD6 are available.
   Bidirectional buffers with open drain, open source and slew rate control are available for each input voltage level, CMOS, TTL, and Schmitt trigger.

TOSHIBA

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