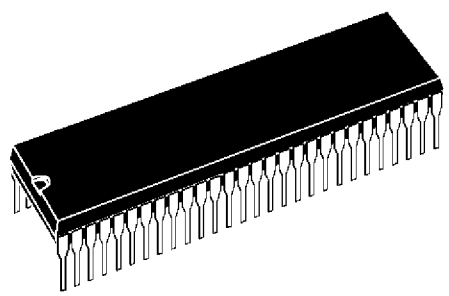
SGS-THOMSON MICROELECTRONICS

ST72E72
ST72T72

8-BIT MCU WITH 24K EPROM, EEPROM, ADC, PWM/BRM DACs, SYNC PROCESSOR, EWPCC, TIMER AND DDC I/F

PRELIMINARY DATA

- 4.5V to 5.5V Supply Operating Range
- 8MHz Maximum Oscillator Frequency
- Fully Static operation
- 0°C to + 70°C Operating Temperature Range
- Run, Wait, Halt, and RAM Retention modes
- User EPROM/OTP: 24Kbytes
- Data RAM: 384 bytes
- EEPROM: 640 + 256 bytes
- 56 pin Shrink Dual-in-Line package
- 27 multifunctional bidirectional I/O lines:
  - 8 lines with 12V open-drain drive capability
  - 8 Programmable Interrupt inputs
  - 8 Analog inputs
- 16-bit Timer, featuring:
  - 2 Input Captures
  - 2 Output Compares (1 output pin)
- 8-bit Analog-to-Digital converter
- Programmable Watchdog Timer
- 16 10-bit PWM/BRM Digital to Analog outputs
- 2 12-bit PWM/BRM Digital to Analog outputs
- EWPCC circuit with on-chip EEPROM
- New upgraded Sync processor for Mode Recognition, Power Management and Composite Video Blanking Generator
- DDC 1/2/AB interface with built-in DMA and I^2C Master/Slave Modes
- Master Reset and Power-On Reset
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (C-Compiler, Cross-Assembler, Debugger)



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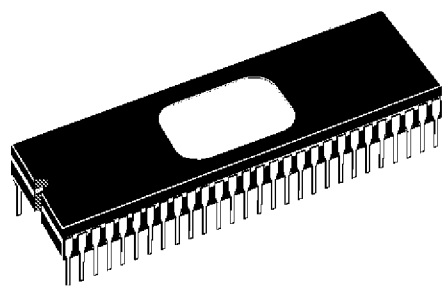


CSDIP56

1 GENERAL DESCRIPTION

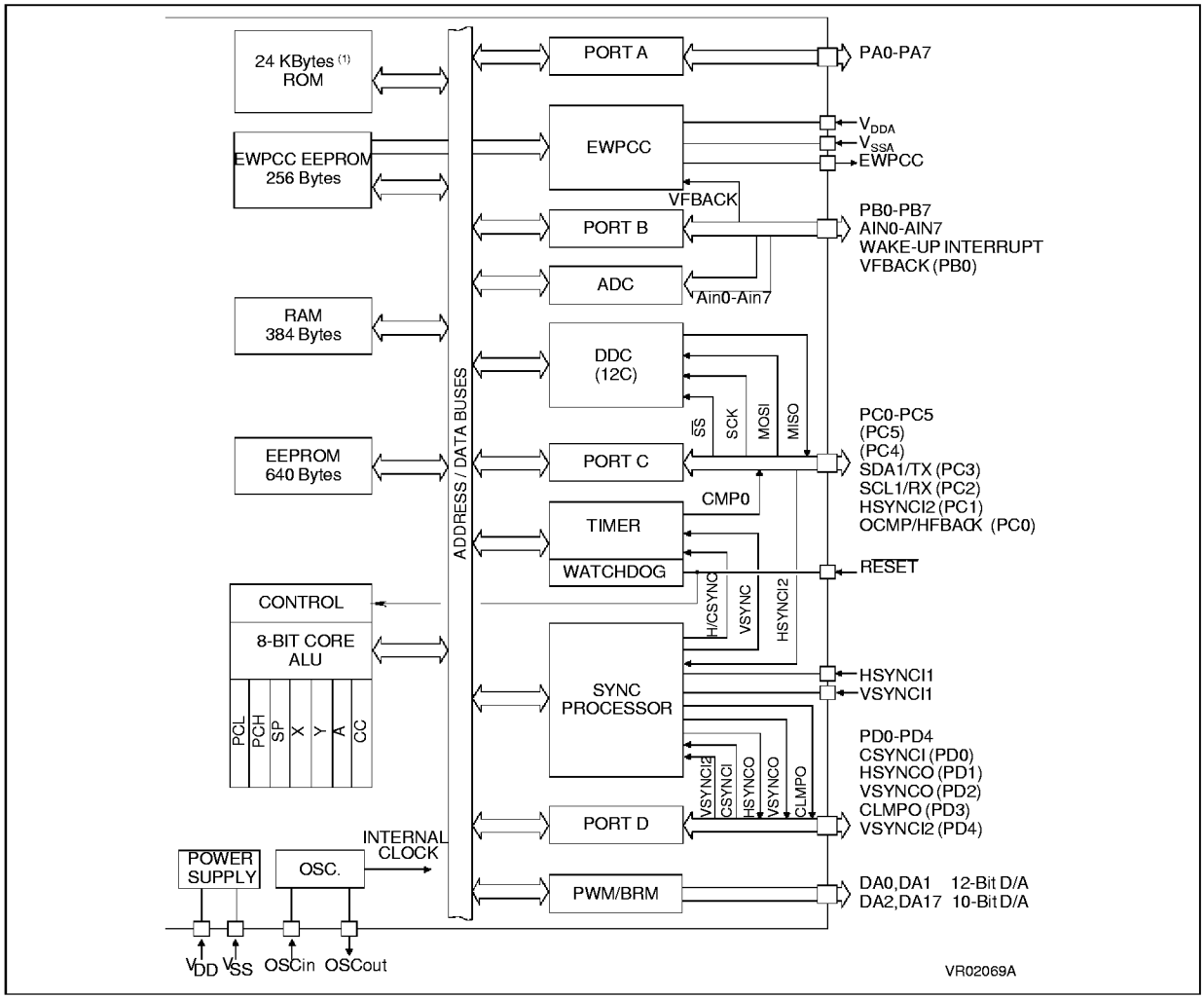
1.1 INTRODUCTION

The ST72T72 and the ST72E72 devices are OTP and EPROM versions respectively of the ST7272 ROM based HCMOS Microcontroller Unit. Please refer to the ST7272 ROM device Datasheet for further details.

From the user's point of view, both the OTP and EPROM devices are functionally identical to the ROM device and possess the same software and hardware features. An additional mode is available to allow programming of the EPROM user memory array. This is set by a specific voltage applied to the V_{PP}/Test pin.

The EPROM and OTP devices feature 24K of user programmable EPROM memory; the EPROM device features a windowed ceramic package which allows the contents of the memory array to be erased by exposure to UV light.

Figure 1. ST72E72/T72 Block Diagram



Note1: EPROM/OTP

1.2 PIN DESCRIPTION

V_{DD} Power supply

V_{SS} Digital Ground

V_{DDA} Analog V_{DD} and reference for EWPCC Digital to Analog Converter (typically 8 Volts).

V_{SSA} Analog V_{SS} for EWPCC DAC.

OSCin, OSCout Oscillator input and output pins; usually connected to a parallel resonant crystal or ceramic resonator. Altenatively an external clock source may also be input via OSCin.

EWPCC Analog correction signal output from East-West Pin Cushion Correction circuit.

SCL1/RX DDC Serial Clock or RX (Falling edge detector with interrupt).

SDA1/TX DDC Serial Data or TX.

OCMP / HFBACK Output compare signal from the Timer.

HSYNCI1 Horizontal Synchronization Input 1.

VSYNCI1 Vertical Synchronization Input 1.

HSYNCI2 Sync Processor Horizontal or complete Synchronization Input 2.

VSYNCI2 Vertical Synchronization Input 2.

CSYNCI Composite Synchronization Input. This pin accepts the composite synchronization input when the Sync Processor I/O functions are enabled.

VFBACK Vertical Flyback signal used for timing correlation for the East-West Pin Cushion correction.

HFBACK Horizontal Flyback Input.

BLANK OUT Video Blanking Output.

HSYNCO Horizontal Synchronization Output from the Sync Processor.

VSYNCO Vertical Synchronization Output from the Sync Processor.

CLMPO Clamp Output. This pin outputs the clamping (back porch) output signal from the Sync Processor .

DA0, DA1 12-bit PWM/BRM outputs (for Analog Controls, after external filtering).

DA2-DA17 10-bit PWM/BRM outputs (for Analog controls, after external filtering).

PORT A 8 I/O lines, bit programmable, accessed through PADDR and PADR Registers. Each bit can be defined as a standard input port bit without pull-up resistor or as an open drain output port (up to 12V).

PORT B 8 Standard bit-programmable I/O lines accessed through the PBDDR and PBDR Registers. Each bit can be programmed as an analog input (by control bits in the PORT B Configuration register), digital input (with internal pull-up resistor), push-pull digital output or as interrupt wake-up (with pull-up). These negative edge or low-level sensitive interrupt lines can wake-up the MCU from WAIT or HALT mode. PB0 is used for the East-West Pin cushion controller VFBACK input when the EWPCC is used.

PORT C 6 Standard bit-programmable I/O lines accessed through the PCDDR and PCDR Registers. PC 0,1 are Inputs with Pull-Up or Push-Pull Outputs, PC 2,3 are Open Drain outputs or Inputs without Pull-Up, PC 4,5 are Open Drain outputs or Digital Inputs with or without Pull-Up internal resistor. The pull-up resistor is enabled for all bits by one control bit in the Programmable Input/Output Configuration Register. PC0 can also be configured as Timer Output Compare pin or Horizontal Flyback Input. PC1 can be programmed as HSYNCI2 sync input for the Sync Processor. PC2/SCL1 and PC3/SDA1 are alternate functions with the DDC cell.

PORT D 5 Standard bit-programmable I/O lines accessed through PDDDR and PDDR Registers. Each bit can be programmed as an input (with internal pull-up resistor), push-pull output or Synchronization inputs and outputs to/from the Sync Processor. When programmed as inputs, Video Synchronization signals can be directly inspected. The inputs may also be passed through the Sync Processor to the Timer Input Captures.

$\overline{\text{RESET}}$ An active-low signal on this pin forces initialization of the MCU. This is the top priority non maskable interrupt. This pin is driven low if the Watchdog Timer has been triggered. The resulting pulse can be used to reset external peripherals.

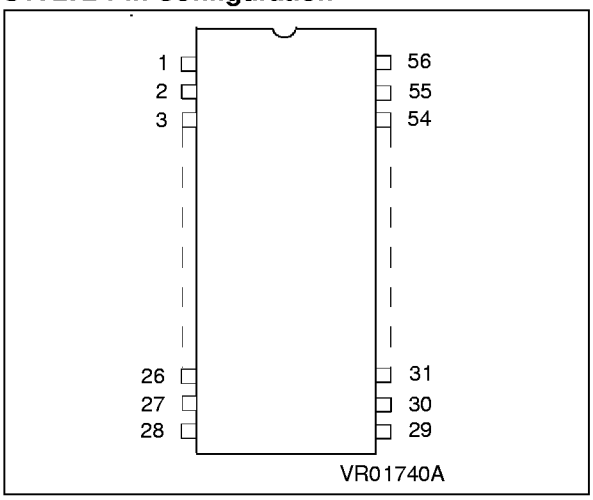
V_{PP}/TEST This pin must be held low for normal operation. In programing mode, this pin is connected to V_{PP}.

CAUTION: *The V_{PP}/TEST pin MUST be connected directly to the V_{SS} pin on the device in order to ensure correct operation.*

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration

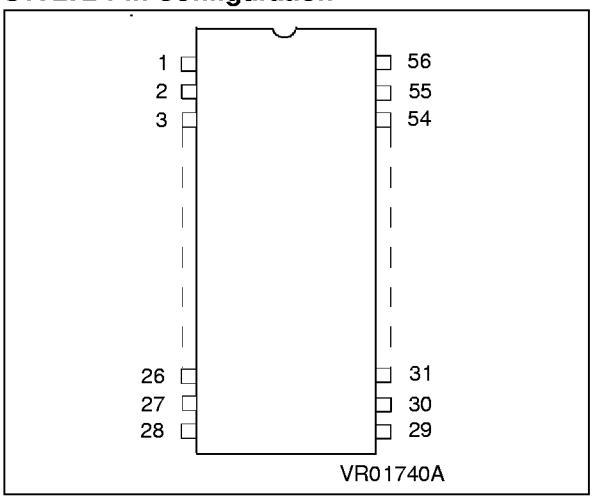


Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
V_{DDA}	Analog power supply	-	1	Typically +8V
EWPCC	EWPCC circuit analog output	-	2	2 - 6V
DA0	12-bit DAC PWM outputs	--	3	Generated by PWM/BRM circuitry, need external filtering.
DA1			4	
DA2	10-bit DAC PWM outputs	--	5	
DA3			6	
DA4			7	
DA5			8	
DA6			9	
DA7			10	
DA8			11	
DA9			12	
PB7	Port B I/Os	Analog input	13	Standard I/O or alternate function. The I/O configuration is software programmable as input with pull-ups, wake-up interrupt input, or push-pull output.
PB6			14	
PB5			15	
PB4			16	
PB3			17	
PB2			18	
PB1			19	
PB0 / VFBACK		Analog input or VFBACK	20	As above, or input for EWPCC circuit, when active.
PD4 / VSYNCI2	Port D I/O	VSYNCI2	21	Vertical Sync input 2 (TTL with pull-up).
PD3 / CLMPO	Port D I/O	CLMPO	22	Clamp output from Sync circuit.
DA10	10-bit DAC PWM outputs	-	23	Generated by PWM/BRM circuitry, need external filtering.
DA11			24	

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration

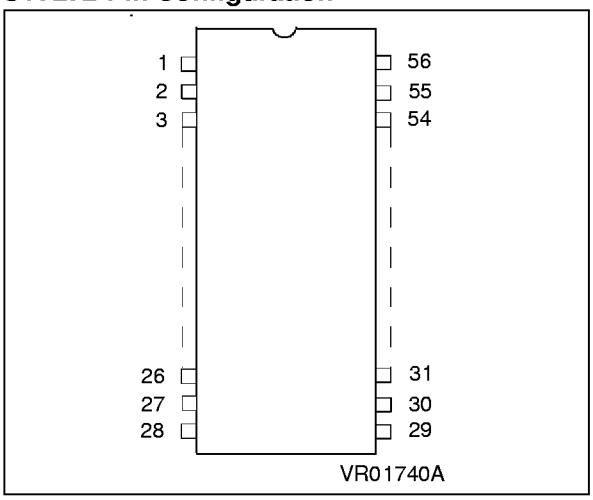


Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
$\overline{\text{RESET}}$	General reset input and output	-	25	As an input, a Reset is generated by an active low signal; when the Watchdog has triggered this pin will be driven low to reset external peripherals.
PD2 / VSYNCO	Port D I/O	VSYNCO	26	Vertical Sync output from Sync processor.
VSYNCI1	VSYNCI1		27	Vertical Sync input to Sync processor (TTL with pull-up).
V_{DD}	Power supply to digital circuits.	-	28	4.5 - 5.5V
HSYNCI1	HSYNCI1		29	Horizontal Sync input to Sync processor (TTL with pull-up).
PD1 / HSYNCO	Port D I/Os	HSYNCO	30	Horizontal Sync output from Sync processor.
PD0 / CSYNCI		CSYNCI	31	Composite Sync input (TTL with pull-up).
OSCOUT	Oscillator output	-	32	These pins may be connected to a parallel resonant crystal or ceramic resonator; alternatively an external clock source may be connected to OSCIN.
OSCIN	Oscillator input		33	
DA12	10-bit DAC PWM outputs	-	34	Generated by PWM/BRM circuitry, need external filtering.
DA13			35	
PA7 / BLANKOUT	Port A I/Os	BLANKOUT	36	Video blanking output from Sync processor.
PA6		-	37	Standard I/Os, bit programmable via PADDR and PADR registers as inputs without pull-ups or as open-drain outputs (up to 12V).
PA5			38	
PA4			39	
PA3			40	
PA2			41	
PA1			42	
PA0			43	

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration



Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
DA14	10-bit DAC PWM outputs	-	44	Generated by PWM/BRM circuitry, need external filtering.
DA15			45	
DA16			46	
DA17			47	
V_{PP}/TEST	TEST	V_{PP}	48	This pin is for SGS-THOMSON internal use only and **MUST** be tied directly to V_{SS} for normal operation. In programing mode this pin is connected to V_{PP}.
PC0 / OCMP / HFBACK	Port C I/Os	OCMP or HFBACK	49	Output compare from Timer peripheral. or Horizontal flyback input (TTL with pull-up).
PC1 / HSYNCI2		HSYNCI2	50	Horizontal Sync input to Sync processor (TTL with pull-up).
PC2 / SCL1 / RX		SCL1 RX	51	DDC serial clock. Can generate interrupt on falling edge for RX Start detection for software SCI.
PC3 / SDA1 / TX		SDA1 TX	52	DDC serial data. OCMP can generate interrupt for TX bit timing for software SCI.
PC4		-	53	
PC5			54	
V_{SS}	Digital Ground	-	55	
V_{SSA}	Analog Ground	-	56	

1.3 MEMORY MAP

Table 1. ST7272 Memory Map

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0000h		PADR	Port A Data Register	XXh	R/W Register
0001h		PBDR	Port B Data Register	XXh	R/W Register
0002h		PCDR	Port C Data Register	XXh	R/W Register
0003h		PDDR	Port D Data Register	XXh	R/W Register
0004h		PADDR	Port A Data Direction Register	00h	R/W Register
0005h		PBDDR	Port B Data Direction Register	00h	R/W Register
0006h		PCDDR	Port C Data Direction Register	00h	R/W Register
0007h		PDDDR	Port D Data Direction Register	00h	R/W Register
0008h	ADC	DR	ADC Data Register	XX	Read Only Register
0009h		CR	ADC control/Status register	00h	R/W Register
000Ah	Reserved				
000Bh		DACR	East/West DAC Register	00h	R/W Register
000Ch	EW	PCC0	East/West Control 0	00h	R/W Register
000Dh		PCC1	East/West Control 1	C0h	R/W Register
000Eh		CR0	DDC EEPROM Control register	00h	R/W Register
000Fh	EEP	CR1	GP1 EEPROM Control register	00h	R/W Register
0010h		CR2	GP2 EEPROM Control register	00h	R/W Register
0011h		CR3	E/W EEPROM Control register	00h	R/W Register
0012h		CR	TIMER Control Register	00h	R/W Register
0013h		SR	TIMER Status Register	XXh	Read Only Register
0014h		IC1HR	TIMER Input Capture High Register 1	XXh	Read only
0015h		IC1LR	TIMER Input Capture Low Register 1	XXh	Read only
0016h		OC1HR	TIMER Output Compare High Register 1	XXh	R/W Register
0017h		OC1LR	TIMER Output Compare Low Register 1	XXh	R/W Register
0018h	TIM	CNTHR	TIMER Counter High Register	FFh	Read only
0019h		CNTLR	TIMER Counter Low Register	FCh	R/W Register
001Ah		ACNTHR	TIMER Alternate Counter High Register	FFh	Read only
001Bh		ACNTLR	TIMER Alternate Counter Low Register	FCh	R/W Register
001Ch		IC2HR	TIMER Input Capture High Register 2	XXh	Read only
001Dh		IC2LR	TIMER Input Capture Low Register 2	XXh	Read only
001Eh		OC2HR	TIMER Output Compare High Register 2	XXh	R/W Register
001Fh		OC2LR	TIMER Output Compare Low Register 2	XXh	R/W Register
0020h		PWM0	(12-BIT PWM) Register	80h	R/W Register
0021h	PWM/BRM	BRM0	(12-BIT BRM) Register	C0h	R/W Register
0022h		PWM1	(12-BIT PWM) Register	80h	R/W Register
0023h		BRM1	(12-BIT BRM) Register	C0h	R/W Register

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0024h	PWM/BRM	PWM2	10-BIT PWM/BRM Registers	80h	R/W Registers
0025h		BRM3 + BRM2		00h	
0026h		PWM3		80h	
0027h		PWM4		80h	
0028h		BRM5+ BRM4		00h	
0029h		PWM5		80h	
002Ah		PWM6		80h	
002Bh		BRM7 + BRM6		00h	
002Ch		PWM7		80h	
002Dh		PWM8		80h	
002Eh		BRM9+ BRM8		00h	
002Fh		PWM9		80h	
0030h		PWM10		80h	
0031h		BRM11 + BRM10		00h	
0032h		PWM11		80h	
0033h		PWM12		80h	
0034h		BRM13+ BRM12		00h	
0035h		PWM13		80h	
0036h		PWM14		80h	
0037h		BRM15 + BRM14		00h	
0038h		PWM15		80h	
0039h		PWM16		80h	
003Ah		BRM17+ BRM16		00h	
003Bh		PWM17		80h	
003Ch		PBICFGR	Port B Input Pull-Up Configuration Register	00h	R/W Register
003Dh		PIOCFGR	Programmable I/O Configuration Register	F8h	R/W Register
003Eh		WDOGR	Watchdog Register	7Fh	R/W Register
003Fh		MISCR	Miscellaneous Register	2Ah	R/W Register
0040h	SYNC	CFGR	SYNCHRO Configuration Register	00h	R/W Register
0041h		MCR	SYNCHRO Multiplexer Register	00h	R/W Register
0042h		CCR	SYNCHRO Counter Register	00h	R/W Register
0043h		POLR	SYNCHRO Polarity Register	00h	R/W Register
0044h		LATR	SYNCHRO Latch Register	00h	R/W Register
0045h		HGENR	SYNCHRO H Sync Generator Register	00h	R/W Register
0046h		VGENR	SYNCHRO V Sync Generator Register	00h	R/W Register
0047h		ENR	SYNCHRO Processor Enable Register	00h	R/W Register

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0048h	DMA	IADHR	DMA Initial High Address Register	XXh	R/W Register
0049h		IADLR	DMA Initial Low Address Register	XXh	R/W Register
004Ah		CADHR	DMA current High Address Register	XXh	R/W Register
004Bh		CADLR	DMA current Low Address Register	XXh	R/W Register
004Ch		ICTR	DMA Initial Counter Register	XXh	R/W Register
004Dh		CCTR	DMA current Counter Register	XXh	R/W Register
004Eh		CTLR	DMA Control Register	00h	R/W Register
004Fh	Reserved				
0050h	DDC	CR	DDC Control Register	00h	R/W Register
0051h		SR1	DDC 1st Status Register	00h	Read only
0052h		SR2	DDC 2nd Status Register	00h	Read only
0053h		CCR	DDC Clock Control Register	00h	R/W Register
0054h		OAR1	DDC 7 Bits Slave address Register	00h	R/W Register
0055h			Reserved		
0056h		DR	DDC Data Register	00h	R/W Register
0057h			Reserved		
0058h	CRC	CRCL	CRC Low register / Reserved	ST INTERNAL USE ONLY	
0059to		CRCH	CRC High register/ Reserved		
005Ah to 007Fh	Reserved				
0080h to 01BFh			User RAM 384 bytes, including stack		
01C0h to 01FFh			Stack 64bytes		
0200h to 027Fh	Reserved				
0280h to 02FFh		DDC-EEPROM	128 bytes dedicated for DDC EEPROM		EEPROM 896 bytes in 4 banks
0300h to 03FFh		GP1-EEPROM	256 bytes for Data GP1 EEPROM		
0400h to 04FFh		GP2-EEPROM	256 bytes for Data GP2 EEPROM		
0500h to 05FFh		EWPCC-EEP-ROM	256 bytes for either EWPCC or Data GP3 EEPROM		

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0600h to 07FFh	Unused				
0800h to 08FFh	Reserved				
0900h to 13FFh	Unused				
1400h to 1FFFh	Reserved				
2000h to 7EFFh			24K bytes program EPROM/OTP		
7F00h to 7FEFh	Reserved				
7FF0h to 7FFFh		7FF0-7FF1	DDC/DMA (OR wiring)		Internal Interrupts
		7FF2-7FF3	TIMER Overflow TOF		"
		7FF4-7FF5	TIMER Output compare OCMP		"
		7FF6-7FF7	TIMER Input capture ICAP		"
		7FF8-7FF9	RX falling edge		"
		7FFA-7FFB	Keyboard (PORT B)		External Interrupts
		7FFC-7FFD	TRAP (software)		"
		7FFE-7FFF7	RESET vector		CPU Interrupt

1.4 EPROM ERASURE

The EPROM memory on the ST72E72 device is erased by exposure to high intensity UV light admitted through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current.

It is recommended that the device be kept out of direct sunlight, since the UV content of sunlight can be sufficient to cause functional failure. Extended exposure to room level fluorescent lighting may also cause erasure. An opaque coating (paint, tape, label, etc...) should be placed over the package window if the product is to be operated under these lighting conditions. Covering the window also reduces I_{DD} in power-saving modes due to photo-diode leakage currents.

An Ultraviolet source of wave length 2537 Å yielding a total integrated dosage of 15 Watt-sec/cm is required to erase the device. The device will be erased in 15 to 20 minutes if such a UV lamp with a 12mW/cm power rating is placed 1 inch from the device window without any interposed filters.

2 ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS

Devices of the ST72 family contain circuitry to protect the inputs against damage due to high static voltage or electric fields. Nevertheless, it is recommended that normal precautions be observed in order to avoid subjecting this high-impedance circuit to voltages above those quoted in the Absolute Maximum Ratings. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained within the range:

$$V_{SS} \leq V_{IN} \text{ and } V_{OUT} \leq V_{DD}$$

To enhance reliability of operation, it is recommended to configure unused I/Os as inputs and to connect them to an appropriate logic voltage level such as V_{SS} or V_{DD}.

All the voltage in the following tables are referenced to V_{SS}.

Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings (Voltage Referenced to V_{SS}).

Symbol	Ratings	Value	Unit
V_{DD}	Recommended Supply Voltage	-0.3 to +6.0	V
V_{DDA}	Analog Reference Voltage	-0.3 to +9.0	V
V_{IN}	Input Voltage	V_{SS} -0.3 to VDD + 0.3	V
V_{OUT}	Output Voltage	V_{SS} -0.3 to VDD + 0.3	V
I_{IN}	Input Current	-10.....+10	mA
I_{OUT}	Output Current	-10.....+10	mA
T_A	Operating Temperature Range	0 to +70	^{O}C
T_{STG}	Storage Temperature Range	-65 to +150	^{O}C
PD	Power Dissipation	TBA	mW
ESD	ESD susceptibility	2000	V

Note: The maximum accumulated current off all I/O pins should not exceed 40 mA for V_{DD} and 40 mA for V_{SS}.

2.2 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \theta J_A) \quad (1)$$

Where:

– T_A is the Ambient Temperature in°C,

– θJ_A is the Package Junction-to-Ambient Thermal Resistance, in °C/W,

– P_D is the sum of P_{INT} and $P_{I/O}$,

– P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power

– $P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

For most applications $P_{I/O} < P_{INT}$ and may be neglected. $P_{I/O}$ may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore:

$$K = P_D \times (T_A + 273°C) + \theta J_A \times P_D^2 \quad (3)$$

Where:

– K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 3. Thermal Characteristics

Symbol	Package	Value	Unit
θJ_A	PSDIP56/CSDIP56W	60	°C/W

2.3 DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to +70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Value			Unit
			min	typ	max	
V_{DD}	Supply Voltage		4.5		5.5	V
V_{OL}	Output Voltage Low Port A (Open drain)	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port B (0-7), Port D(0:7) Push-pull	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port C (PC2,PC3,PC4) Push-pull	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port C (PC0,PC1,PC5) Open drain	I_{OL}=1.6 mA			0.4	V
V_{OL}	during Power ON Reset and Watch-dog Reset				0.4	V
V_{OH}	Output Voltage High Push-pull	I_{OH}=1.6 mA	V_{DD}-0.8			V
V_{IH}	Input High Voltage PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	Leading Edge	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	Trailing Edge	V_{SS}		0.3xV_{DD}	V
I_{IL}	I/O Ports Hi-Z Leakage Current PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	V_{SS} V_{DD}			10	uA uA
C_{OUT} C_{IN}	Capacitance: Ports (as Input or Output), RESET				12 8	pF pF
R_{ON}	DA1,D(A3-17)(PWM/BRM) Serial Resistor			700	1000	Ohms
I_{RPU}	Pull-up resistor current	V_{DD}=5v V_{IN}=V_{SS}		20		uA

DC ELECTRICAL CHARACTERISTICS(Cont'd)

DDC Bus (I^2C INTERFACE)				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{HYS}	Hysteress of Shmitt trigger inputs fixed input levels V_{DD}-related input levels	 na na	 na na	V
T_{SP}	Pulse width of spikes which must be suppressed by the input filter	na	na	ns
T_{OF}	Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400pF with up 3mA sink current at VOL1		 250	ns
I	Input current each I/O pin with an input voltage between 0.4v and 0.9 V_{DD} max	-10	10	µA
C	Capacitive load for each I/O pin		10	pF

A/D CONVERTER						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Val	Resolution	F_{OSC} = 8 MHz		8		bit
Terr	Total Error	F_{OSC} = 8 MHz			± 3	LSB
Tcon	Conversion Time	F_{OSC} = 8 MHz	16			µs
Rva	Analog Source Impedance			30		KΩ

2.4 AC ELECTRICAL CHARACTERISTICS

(T_A = 0 to +70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ.	Max	
V_{DD}	Operating Supply Voltage	4 MHz Internal	4.5		5.5	V
I_{DD}	Supply Current	RUN Mode F_{ext} = 8MHz V_{DD} = 5.0V		7.5	10	mA
		WAIT Mode f_{ext} = 8MHz V_{DD} = 5.5V		3.5	5	mA

2.5 CONTROL TIMING

(Operating conditions T_A 0 to +70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ.	Max	
f_{OSC}	Frequency of Operation	V_{DD} = 4.5V f external f internal			8 4	MHz
t_{ILCH}	Halt Mode Recovery Startup Time				20	ms
t_{RL}	External RESET Input pulse Width		1.5			t_{CYC}
t_{PORL}	Power Reset Duration		4096			t_{CYC}
T_{DOGL}	Watchdog RESET Output Pulse Width		2		2	t_{CYC}
t_{DOG}	Watchdog Time-out		49,152		3,145,728	t_{CYC}
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{OXOV}	Crystal Oscillator Start-up Time				50	ms
t_{DDR}	Power up rise time	V_{DD} min			100	ms

Notes :
1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

AC ELECTRICAL CHARACTERISTICS(Cont'd)

2.5.1 DDC (I^2C BUS) INTERFACE

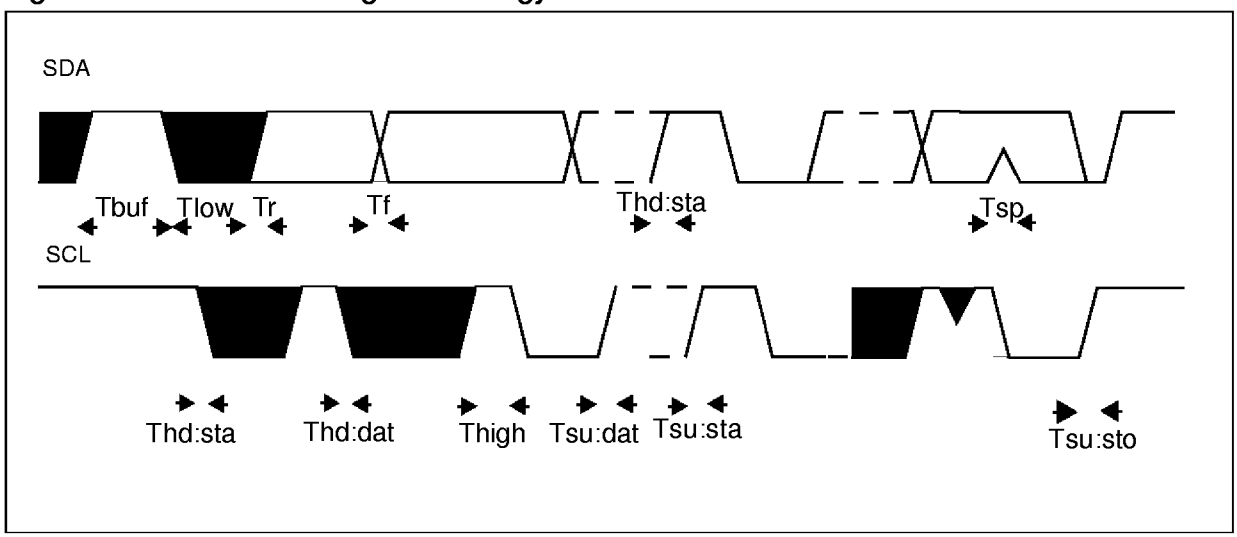
2.5.1.1 Timing

Parameter	Min	Max	Symbol	Unit
Bus free time between a STOP and START condition	4.7		Tubs	ms
Hold time START condition. After this period, the first clock pulse is generated	4.0		Thd:sta	µs
LOW period of the SCL clock	4.7		Tlow	µs
HIGH period of the SCL clock	4.0		Thigh	µs
Set-up time for a repeated START condition	4.7		Tsu:sta	µs
Data hold time	250 (1)		Thd:dat	ns
Data set-up time	250		Tsu:dat	ns
Rise time of both SDA and SCL signals		1000	Tr	ns
Fall time of both SDA and SCL signals		300	Tf	ns
Set-up time for STOP condition	4.0		Tsu:sto	ns
Capacitive load for each bus line		400	Cb	pF

1. The device provides a hold time of at least 250ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Cb = total capacitance of one bus line in pF

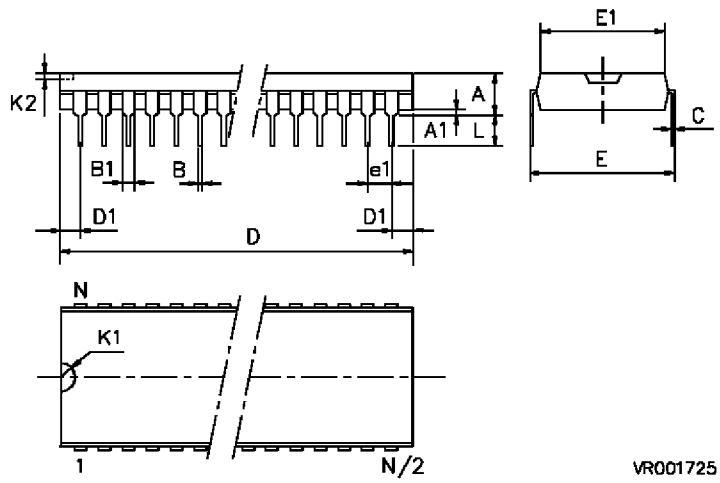
Figure 2. Definition of Timing Terminology



3 GENERAL INFORMATION

3.1 PACKAGE MECHANICAL DATA

Figure 3. 56 Shrink Plastic Dual In Line Package, 600-mil Width



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D		52.12			2.052	
D1	-	-	-	-	-	-
E			18.54			0.730
E1		13.72				0.540
K1	-	-	-	-	-	-
K2	-	-	-	-	-	-
L	2.54		3.81	0.100		0.150
e1		1.78			0.070	
Number of Pins						
N	56					

3.2 ORDERING INFORMATION

Sales Types	EPROM/OTP Size	RAM Size	Temperature Range	Package
ST72E72N5D1	24K	384	25°C	CSDIP56
ST72T72N5B1	24K	384	0 to +70°C	PSDIP56

ST72T72 MICROCONTROLLER OPTION LIST

Customer . . . . . .

Address . . . . . .

. . . . . .

Contact . . . . . .

Phone No . . . . . .

Reference . . . . . .

SGS-THOMSON Microelectronics references

Device:

[ ] ST72T72N5B1
24K OTP

CLPOUT OPTION:
Maximum delay 250ns
Programmable back porch clamping width
(0, 250ns, 500ns, 1 us)

Package: PSDIP56

[ ] ST72E72N5B1
24K EPROM

CLPOUT OPTION:
Maximum delay 250ns
Programmable back porch clamping width
(0, 250ns, 500ns, 1 us)

Package: CSDIP56

[ ] ST72T72M5B1
24K OTP

CLPOUT OPTION:
Maximum delay 125ns
Programmable back porch clamping width
(0, 125ns, 250ns, 500 us)

Package: PSDIP56

[ ] ST72E72M5B1
24K EPROM

CLPOUT OPTION:
Maximum delay 125ns
Programmable back porch clamping width
(0, 125ns, 250ns, 500 us)

Package: CSDIP56

Temperature Range: [ ] 0°C to + 70°C

Signature

Date