

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator type

Description

The CXP88800 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP88616/88624, CXP88732/88740/88748 and CXP88852/88860.

Features

- A wide instruction set (213 instructions) which cover various types of data.
 - 16-bit operation/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
- Applicable EPROM

- Incorporated RAM capacity
- Peripheral functions
 - A/D converter
 - Serial interface
 - Timer
 - High precision timing pattern generator
 - PWM/DA gate output
 - Analog signal input circuit

- CTL write/rewrite circuit
- Servo input control
- VSYNC separator
- FRC capture unit
- PWM output
- VISS/VASS circuit
- Remote control receiving circuit
- Tri-state output
- Pseudo HSYNC output function
- High-speed head switching circuit
- Interruption
- Standby mode
- Package

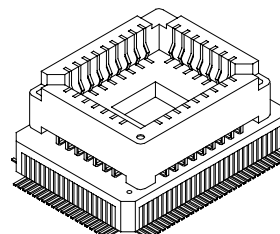
Note) Mask option depends on the type of the CXP88800. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

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100 pin QFP (Ceramic)



250ns at 16MHz operation

122μs at 32kHz operation

LCC type 27C512

(Maximum capacity : 60K bytes for option1,
32K bytes for option2)

1600 bytes

8-bit, 8-channel, successive approximation method

(Conversion time of 20.0μs/16MHz)

Incorporated 8-bit and 8-stage FIFO

(auto transfer for 1 to 8 bytes), 1 channel

8-bit clock synchronous type, 1 channel

8-bit timer, 8-bit timer/counter, 2 channels

19-bit time base timer, 32kHz timer/counter

PPG 19-pin, 32-stage programmable, RTG 5 pins, 2 channels

5-bit, 8-stage FIFO (RECCTL control), 1 channel

PWM output 12 bits 2 channels

(Repetitive frequency 62.5kHz/16MHz)

DA gate pulse output 13 bits, 2 channels

Capstan FG amplifier circuit

Drum FG amplifier circuit

Drum PG amplifier circuit

PBCTL amplifier circuit

Recording current control circuit

Capstan FG, drum FG/PG, CTL input

Incorporated 26-bit and 8-stage FIFO

14 bits, 1 channel

Pulse duty auto detection circuit

8-bit pulse measurement counter with on-chip, 6-stage FIFO

PPG output 1 pin, output 8 pins

20 factors, 15 vectors, multi-interruption possible

SLEEP/STOP

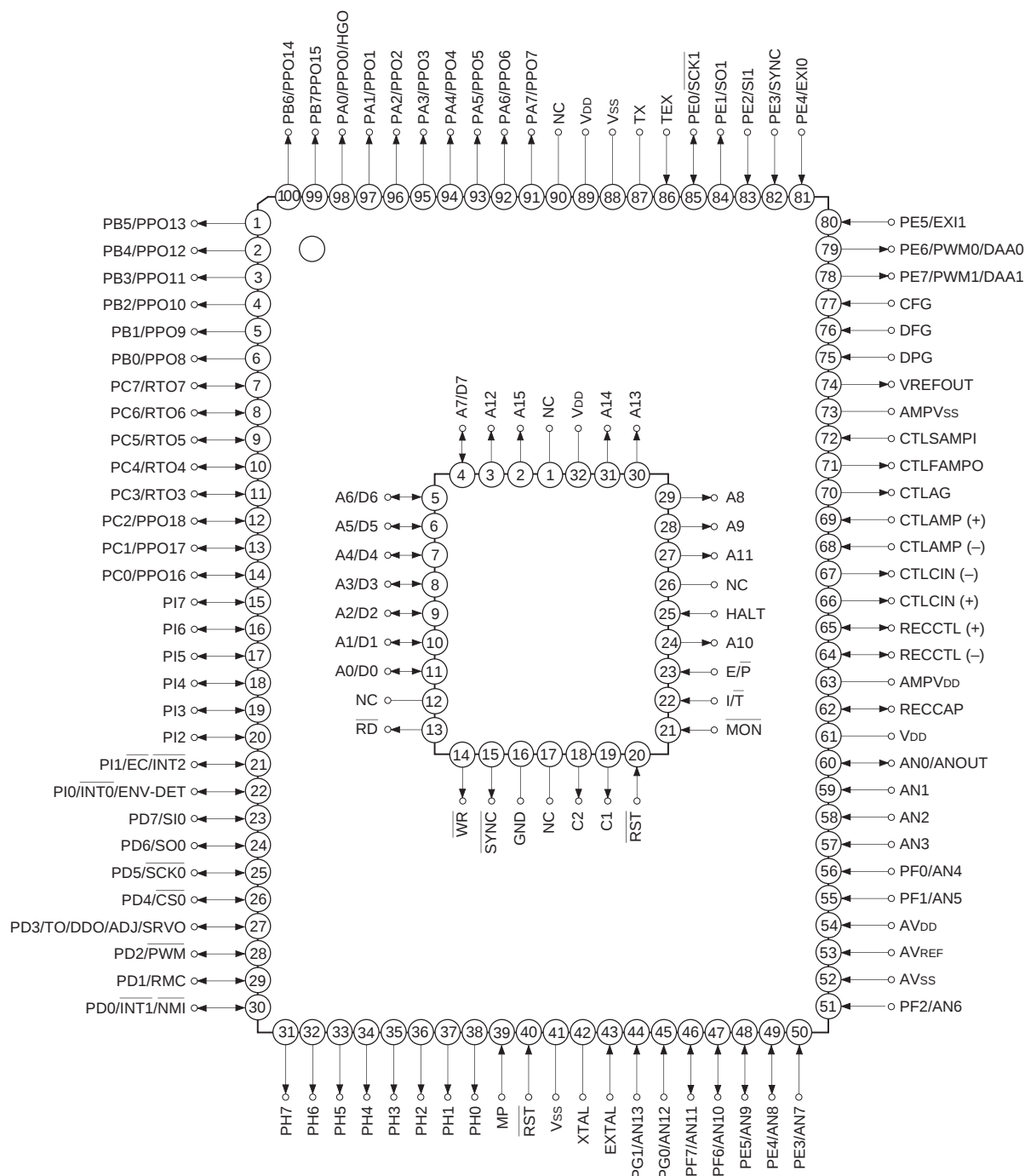
100-pin ceramic QFP

The diagram shows the ATmega328P microcontroller with its pins numbered 1 to 50. The functions for each pin are as follows:

- Pin 1:** PB5/PP013
- Pin 2:** PB4/PP012
- Pin 3:** PB3/PP011
- Pin 4:** PB2/PP010
- Pin 5:** PB1/PP09
- Pin 6:** PB0/PP08
- Pin 7:** PC7/RTO7
- Pin 8:** PC6/RTO6
- Pin 9:** PC5/RTO5
- Pin 10:** PC4/RTO4
- Pin 11:** PC3/RTO3
- Pin 12:** PC2/PP018
- Pin 13:** PC1/PP017
- Pin 14:** PC0/PP016
- Pin 15:** PI7
- Pin 16:** PI6
- Pin 17:** PI5
- Pin 18:** PI4
- Pin 19:** PI3
- Pin 20:** PI2
- Pin 21:** PI1/EC/INT2
- Pin 22:** PI0/INT0/ENV-DET
- Pin 23:** PD7/SI0
- Pin 24:** PD6/SO0
- Pin 25:** PD5/SCK0
- Pin 26:** PD4/CS0
- Pin 27:** PD3/TO/DDO/ADJ/SRVO
- Pin 28:** PD2/PWM
- Pin 29:** PD1/RMC
- Pin 30:** PD0/INT1/NMI
- Pin 31:** PH7
- Pin 32:** PH6
- Pin 33:** PH5
- Pin 34:** PH4
- Pin 35:** PH3
- Pin 36:** PH2
- Pin 37:** PH1
- Pin 38:** PH0
- Pin 39:** MP
- Pin 40:** RST
- Pin 41:** Vss
- Pin 42:** XTAL
- Pin 43:** EXTAL
- Pin 44:** CG1/AN13
- Pin 45:** CG0/AN12
- Pin 46:** PPF7/AN11
- Pin 47:** PPF6/AN10
- Pin 48:** PF5/AN9
- Pin 49:** PF4/AN8
- Pin 50:** PF3/AN7

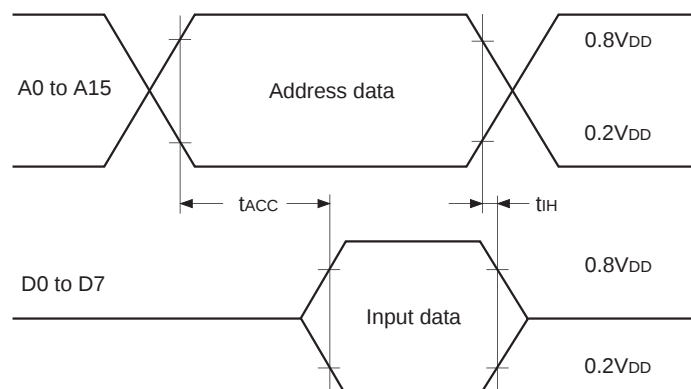
- Note)**
1. NC (Pin 90) is always connected to V_{DD} .
 2. V_{DD} (Pins 61 and 89) are both connected to V_{DD} .
 3. V_{SS} (Pins 41 and 88) are both connected to GND.
 4. MP (Pin 39) is always connected to GND.

Pin Assignment in Evaluator Mode



EPROM Read Timing ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

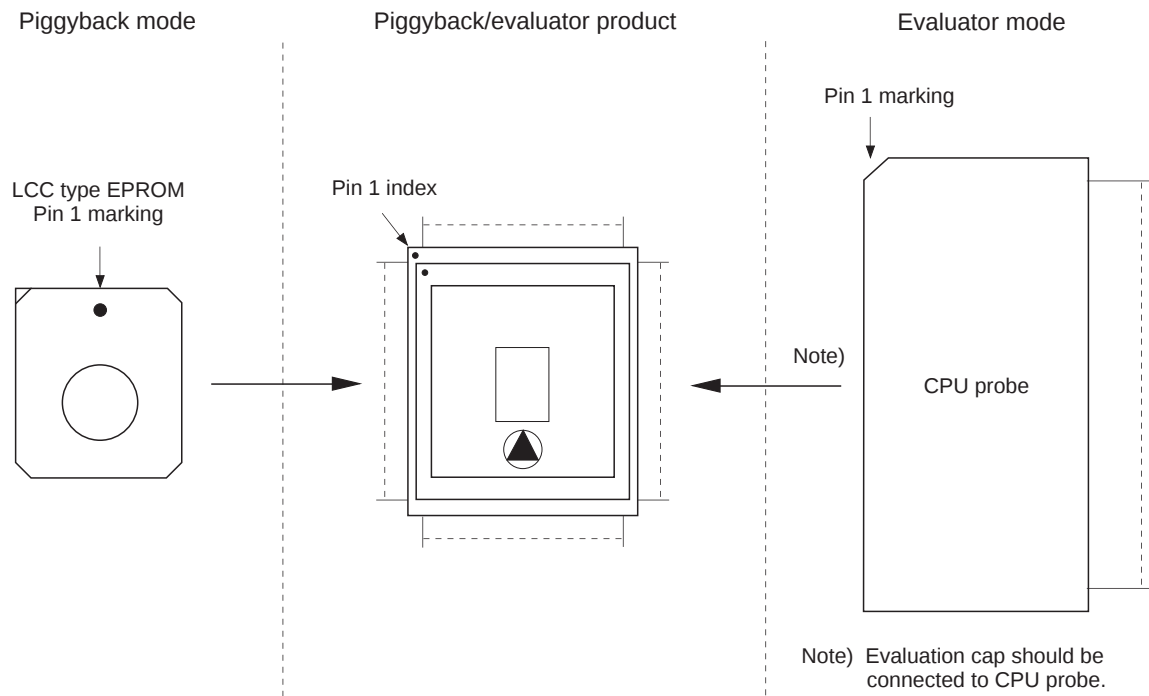
Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		75	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

**Product List**

Option item	Products									
	Mask product								Piggyback/evaluator product	
	CXP 88616	CXP 88624	CXP 88732	CXP 88740	CXP 88748	CXP 88852	CXP 88860	CXP88800 -U01Q	CXP88800 -U02Q	
Package	100-pin plastic QFP								100-pin ceramic QFP	
ROM capacity	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes	52K bytes	60K bytes	EPROM 60K bytes	EPROM 32K bytes	
									27C512 used	
Reset pin pull-up resistor	Existent/Non-existent								Existent	
Input circuit format*1	CMOS schmitt/TTL schmitt								TTL schmitt	
Power-on reset circuit	Existent/Non-existent		Non-existent						Non-existent	Existent

*1) The input circuit format can be selected for PE3/SYNC.

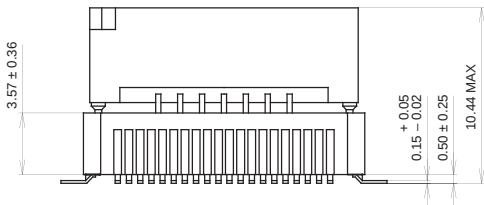
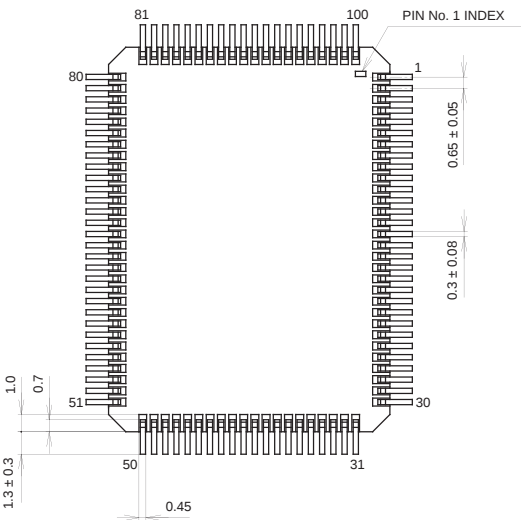
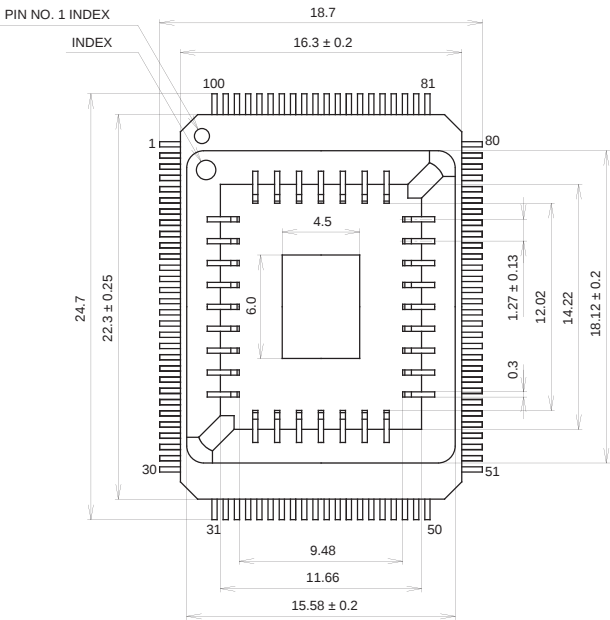
Piggyback mode/evaluator mode can be switched as shown below.



Package Outline

Unit: mm

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g