珠海炬力集成电路设计有限公司

ATJ2001(LQFP176)

DATA SHEET

Ver1.02

Tel：86-756-3392353 Fax：86-756-3392251

Short Descriptions

This is an SoC chip suitable for portable MP3 audio player with minimal component. With developing system provided, it is easy to fit every versatile applications.

Features

- 24 bits DSP Core with on-chip ICE support
- On-chip DSP 16K*24 PM and (16K-256)*24 DM, can be switched to be MCU memory space
- Integrated 8bit MCU with on-chip ICE support which the instructions are compatible with the Z80 CPU
- Internal 16k bytes SRAM accessed by MCU
- External up to 512M bytes program MROM/Flash/SRAM accessed by MCU or DMA
- External SmartMedia Card/MultiMedia Card support
- Support 14.318MHz/16.368MHz/17.734475MHz/24.576MHz OSC with on-chip PLL for DSP
- Supported Nand type and Nor type flash memory
- 2-channel DMA for MCU
- 1-channel CTC(Counter/Timer Controller) for MCU
- On-chip interrupt controller for MCU
- Built-in power management unit(PMU), supporting 1 or 2 batteries operation
- Support RTC with 32.768kHz or 76.8kHz OSC
- Support USB1.1 interface
- Support SPDIF IN/UART/IR interface
- Support on-chip Stereo 18 bit Sigma-Delta DAC
- Support external LCM/Keyboard Autoscan(4*9)/GPIO
- Support external 320*240/240*160/240*120… LCM with Frame Buffer built-in
- Support external 68xx interface LCM, such as Motorola MC141803 LCD
- Support on-chip 1/3 biased 1/4 duty LCD driver(4*13DOTs)/Keyboard(2*13)/GPIO
- Support external CMOS image sensor interface
- Support FM IF input with counter
- On-chip 16-bit ADC for Microphone input and touch panel support , sample rate at 8K/11K/12K/16K/22K/24K/32K
- On-chip 2 channel power amplifiers
- Key-in Tone uses GPIO, implemented by SW
- 176-pin LQFP package

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1. Pin descriptions

Pin No.	Pin Name	I/O Type	Reset Default	Short Description
1	LOSCI	AI	/	Low frequency crystal OSC input
2	LOSCO	AO	/	Low frequency crystal OSC output
3	GND	PWR	/	Digital signal ground
4 4(1)	A15	O	L	Bit15 of ext. memory address bus
	CLE	O	L	Command latch enable of Nand type flash
5 5(1)	AC'97RST-	O	H	Reset to AC'97 block
	ATA_RST-	O	H	ATA device reset
6 6(1)	A16	O	L	Bit16 of ext. memory address bus
	ALE	O	L	Address latch enable of Nand type flash
7 7(1)	GIOB0	BI	Z	Bit0 of general purpose I/O port B
	DAC_BCK	O	Z	Ext. ΣΔ DAC bit clock output
8 8(1)	A17	O	L	Bit17 of ext. memory address bus
	ATAD8	BI	L	Bit8 of ATA device data bus
9 9(1)	GIOB1	BI	Z	Bit1 of general purpose I/O port B
	DAC_LR	O	Z	Ext. ΣΔ DAC left/right channel output
10 10(1)	A18	O	L	Bit18 of ext. memory address bus
	ATAD9	BI	L	Bit9 of ATA device data bus
11 11(1)	GIOB2	BI	Z	Bit2 of general purpose I/O port B
	DAC_SDATA	O	Z	Ext. ΣΔ DAC serial data output
12 12(1)	A19	O	L	Bit19 of ext. memory address bus
	ATAD10	BI	L	Bit10 of ATA device data bus
13 13(1)	GIOB3	BI	Z	Bit3 of general purpose I/O port B
	DAC_FS256	O	Z	Ext. ΣΔ DAC 256x over sampling clock
14 14(1)	A20	O	L	Bit20 of ext. memory address bus
	ATAD11	BI	L	Bit11 of ATA device data bus
15 15(1)	GIOB4	BI	Z	Bit4 of general purpose I/O port B
	AC'97BITCK	O	Z	AC'97 codec bit clock
16 16(1)	A21	O	L	Bit21 of ext. memory address bus
	ATAD12	BI	L	Bit12 of ATA device data bus
17	GIOB5	BI	Z	Bit5 of general purpose I/O port B

17(1)	AC'97SYNC	O	Z	AC'97 codec sample SYNC
18 18(1)	A22	O	L	Bit22 of ext. memory address bus
	ATAD13	BI	L	Bit13 of ATA device data bus
19 19(1) 19(2)	GIOB6	BI	Z	Bit6 of general purpose I/O port B
	AC'97SDI	I	Z	AC'97 codec serial data input
	DAC3LO	O	Z	Int. Σ Δ DAC3 right channel digital output
20 20(1)	A23	O	L	Bit23 of ext. memory address bus
	ATAD14	BI	L	Bit14 of ATA device data bus
21 21(1)	A24	O	L	Bit24 of ext. memory address bus
	ATAD15	BI	L	Bit15 of ATA device data bus
22 22(1) 22(2)	GIOB7	BI	Z	Bit7 of general purpose I/O port B
	AC'97SDO	O	Z	AC'97 codec serial data output
	DAC3RO	O	Z	Int. Σ Δ DAC3 right channel digital output
23	VCC	PWR		Power supply for Pads circuits (3.15v)
24	USBD-	A	/	USB negative connect
25	USBD+	A	/	USB positive connect
26	USBVBUS	I	L	USB cable power signal
27	PVDD	A	/	Bypass capacitor for power amplifier
28	PAOR	A	/	Output of right channel power amplifier
29	PAOL	A	/	Output of left channel power amplifier
30	PGND	PWR	/	Ground for power amplifier circuits
31	PAIR	A	/	Input of right channel power amplifier
32	PAIL	A	/	Input of left channel power amplifier
33	AOUTR	A	/	Int. sigma-dalta DAC right channel analog output
34	AOUTL	A	/	Int. sigma-dalta DAC left channel analog output
35	VRDA	A	/	Reference voltage for DAC
36	VLAD	A	/	Low voltage for Touch Panel
37	VRAD	A	/	Reference voltage for ADC
38	AGCI	A	/	Microphone ADC amplifier input
39	MICOUT	A	/	Microphone pre-amplifier output
40	MICIN	A	/	Microphone pre-amplifier input
41	VMIC	A	/	Power supply for microphone & Touch Panel

42	AGND	PWR	/	Analog ground for record, touch panel and ADC blocks
43	Y2	AI	/	Connect to touch panel Y2
44	Y1	AI	/	Connect to touch panel Y1
45	X1	AI	/	Connect to touch panel X1
46	X2	AI	/	Connect to touch panel X2
47	AVCC	PWR		Power supply for record, touch panel and ADC blocks (3.15v)
48	BATSEL	I		Battery select, 0:one battery 1:two batteries
49	IBIAS	I		Int. bias pin with a ext.R(1.5Mohm) to ground
50	VREFI	A		Reference voltage input (1.5v)
51	VL0	AI		Battery monitor reference voltage input (1.40v)
52	VL1	AI		Battery monitor reference voltage input (1.30v)
53	VL2	AI		Battery monitor reference voltage input (1.15v)
54	VL3	AI		Battery monitor reference voltage input (1.05v)
55	DCDIS	I	L	Int DC-DC convertor disable, 0:enable 1:disable
56	VBAT	I		Battery signal input (1.0-1.5v)
57	DCF3	AI	/	The third DC-DC feedback pin
58	DCF2	AI	/	VCC(3.15V) DC-DC feedback pin
59	DCF1	AI	/	VDD(2.35V) DC-DC feedback pin
60	VP1	PWR		Power supply for int. regulator
61	VDD	PWR		Power supply for core (2.35v)
62	VP2	AI	/	Input for int. power switch
63	DCOP2	AO	/	VCC(3.15V) DC-DC pulse output
64	DCOP3	AO	/	The third DC-DC pulse output
65	DCOP1	AO	/	VDD(2.35V) DC-DC pulse output
66	AVDD	PWR		Power supply for PLL analog circuits (2.35v)
67	AVSS	PWR	/	Ground for PLL analog circuits
68	HOSCI	AI	/	High frequency crystal OSC input
69	HOSCO	AO	/	High frequency crystal OSC output
70	GND	PWR	/	Digital signal ground

71	CKOUT2	O	L	High frequency clock output
72 72(1)	GIOC0	BI	Z	Bit0 of general purpose I/O port C
	SIN1	I	Z	UART1 serial input
73 73(1)	XSCLK	O	H	TCP LCM XSCLK output
	LCDCK	O	H	TCP2 LCD module CK
74 74(1)	GIOC1	BI	Z	Bit1 of general purpose I/O port C
	SOUT1	O	Z	UART1 serial output
75 75(1)	DISPOFF	O	Z	TCP LCM display off control output
	FMIFIN	I	Z	FM radio IF counter input
76	VDD	PWR		Power supply for core (2.35v)
77 77(1) 77(2)	FRAME	O	Z	TCP LCM frame signal output
	V2	O	Z	Int. 4comX28seg LCD driver V2
	LCM_CE	O	Z	MC141803 CE
78	VCC	PWR		Power supply for Pads circuits (3.15v)
79 79(1) 79(2)	YSCLK_LP	O	L	TCP LCM YSCLK/LP signal output
	LCM_RW-	O	L	MC141803 RW-
	LCDCE	O	L	TCP2 LCD module CE
80 80(1) 80(2)	GIOC2	BI	Z	Bit2 of general purpose I/O port C
	SIN2	I	Z	UART2 serial input
	IRRX	I	Z	IR receive input
81 81(1) 81(2)	YDU	O	Z	TCP LCM YDU signal output
	V1	O	Z	Int. 4comX28seg LCD driver V1
	LCM_CS-	O	Z	MC141803 CS-
82 82(1) 82(2)	GIOC3	BI	Z	Bit3 of general purpose I/O port C
	SOUT2	O	Z	UART2 serial output
	IRTX	O	Z	IR transmit output
83 83(1) 83(2)	GIOF7	BI	Z	Bit7 of general purpose I/O port F
	SEG19	O	Z	SEG19 of int. 4comX28seg LCD driver
	KEYO7	O	Z	Bit7 of key scan circuit output
84	GIOC4	BI	Z	Bit4 of general purpose I/O port C
85 85(1) 85(2)	GIOF6	BI	Z	Bit6 of general purpose I/O port F
	SEG18	O	Z	SEG18 of int. 4comX28seg LCD driver
	KEYO6	O	Z	Bit6 of key scan circuit output
86	GIOC5	BI	Z	Bit5 of general purpose I/O port C

87 87(1) 87(2)	GIOF5	BI	Z	Bit5 of general purpose I/O port F
	SEG17	O	Z	SEG17 of int. 4comX28seg LCD driver
	KEYO5	O	Z	Bit5 of key scan circuit output
88 88(1) 88(2)	GIOF4	BI	Z	Bit4 of general purpose I/O port F
	SEG16	O	Z	SEG16 of int. 4comX28seg LCD driver
	KEYO4	O	Z	Bit4 of key scan circuit output
89	VCC	PWR		Power supply for Pads circuits (3.15v)
90 90(1)	GIOG0	BI	Z	Bit0 of general purpose I/O port G
	SEG20	O	Z	SEG20 of int. 4comX28seg LCD driver
91 91(1) 91(2)	GIOF3	BI	Z	Bit3 of general purpose I/O port F
	SEG15	O	Z	SEG15 of int. 4comX28seg LCD driver
	KEYO3	O	Z	Bit3 of key scan circuit output
92 92(1) 92(2)	GIOF2	BI	Z	Bit2 of general purpose I/O port F
	SEG14	O	Z	SEG14 of int. 4comX28seg LCD driver
	KEYO2	O	Z	Bit2 of key scan circuit output
93 93(1) 93(2)	GIOF1	BI	Z	Bit1 of general purpose I/O port F
	SEG13	O	Z	SEG13 of int. 4comX28seg LCD driver
	KEYO1	O	Z	Bit1 of key scan circuit output
94 94(1) 94(2)	GIOF0	BI	Z	Bit0 of general purpose I/O port F
	SEG12	O	Z	SEG12 of int. 4comX28seg LCD driver
	KEYO0	O	Z	Bit0 of key scan circuit output
95 95(1)	GIOG1	BI	Z	Bit1 of general purpose I/O port G
	SEG21	O	Z	SEG21 of int. 4comX28seg LCD driver
96 96(1) 96(2)	GIOE7	BI	Z	Bit7 of general purpose I/O port E
	SEG11	O	Z	SEG11 of int. 4comX28seg LCD driver
	KEYI11	I	Z	Bit11 of key scan circuit input
97 97(1) 97(2)	GIOE6	BI	Z	Bit6 of general purpose I/O port E
	SEG10	O	Z	SEG10 of int. 4comX28seg LCD driver
	KEYI10	I	Z	Bit10 of key scan circuit input
98 98(1) 98(2)	GIOE5	BI	Z	Bit5 of general purpose I/O port E
	SEG9	O	Z	SEG9 of int. 4comX28seg LCD driver
	KEYI9	I	Z	Bit9 of key scan circuit input
99 99(1)	GIOE4	BI	Z	Bit4 of general purpose I/O port E
	SEG8	O	Z	SEG8 of int. 4comX28seg LCD driver

99(2)	KEYI8	I	Z	Bit8 of key scan circuit input
100 100(1) 100(2)	GIOE3	BI	Z	Bit3 of general purpose I/O port E
	SEG7	O	Z	SEG7 of int. 4comX28seg LCD driver
	KEYI7	I	Z	Bit7 of key scan circuit input
101 101(1)	GIOG2	BI	Z	Bit2 of general purpose I/O port G
	SEG22	O	Z	SEG22 of int. 4comX28seg LCD driver
102 102(1) 102(2)	GIOE2	BI	Z	Bit2 of general purpose I/O port E
	SEG6	O	Z	SEG6 of int. 4comX28seg LCD driver
	KEYI6	I	Z	Bit6 of key scan circuit input
103 103(1) 103(2)	GIOE1	BI	Z	Bit1 of general purpose I/O port E
	SEG5	O	Z	SEG5 of int. 4comX28seg LCD driver
	KEYI5	I	Z	Bit5 of key scan circuit input
104 104(1) 104(2)	GIOE0	BI	Z	Bit0 of general purpose I/O port E
	SEG4	O	Z	SEG4 of int. 4comX28seg LCD driver
	KEYI4	I	Z	Bit4 of key scan circuit input
105 105(1) 105(2) 105(3)	GIOD7	BI	Z	Bit7 of general purpose I/O port D
	SEG3	O	Z	SEG3 of int. 4comX28seg LCD driver
	TCPD7	O	Z	Bit7 of TCP data bus
	KEYI3	I	Z	Bit3 of key scan circuit input
106 106(1) 106(2) 106(3)	GIOD6	BI	Z	Bit6 of general purpose I/O port D
	SEG2	O	Z	SEG2 of int. 4comX28seg LCD driver
	TCPD6	O	Z	Bit6 of TCP data bus
	KEYI2	I	Z	Bit2 of key scan circuit input
107 107(1)	GIOG3	BI	Z	Bit3 of general purpose I/O port G
	SEG23	O	Z	SEG23 of int. 4comX28seg LCD driver
108 108(1) 108(2) 108(3)	GIOD5	BI	Z	Bit5 of general purpose I/O port D
	SEG1	O	Z	SEG1 of int. 4comX28seg LCD driver
	TCPD5	O	Z	Bit5 of TCP data bus
	KEYI1	I	Z	Bit1 of key scan circuit input
109	GND	PWR	/	Digital signal ground
110 110(1) 110(2) 110(3)	GIOD4	BI	Z	Bit4 of general purpose I/O port D
	SEG0	O	Z	SEG0 of int. 4comX28seg LCD driver
	TCPD4	O	Z	Bit4 of TCP data bus
	KEYI0	I	Z	Bit0 of key scan circuit input

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111	VDD	PWR		Power supply for core (2.35v)
112 112(1)	GIOD3	BI	Z	Bit3 of general purpose I/O port D
	COM3	O	Z	COM3 of int. 4comX28seg LCD driver
112(2) 112(3)	TCPD3	O	Z	Bit3 of TCP data bus
	LCDD3	O	Z	Bit3 of TCP2 data bus
113 113(1) 113(2) 113(3)	GIOD2	BI	Z	Bit2 of general purpose I/O port D
	COM2	O	Z	COM2 of int. 4comX28seg LCD driver
	TCPD2	O	Z	Bit2 of TCP data bus
	LCDD2	O	Z	Bit2 of TCP2 data bus
114 114(1)	GIOG4	BI	Z	Bit4 of general purpose I/O port G
	SEG24	O	Z	SEG24 of int. 4comX28seg LCD driver
115 115(1) 115(2) 115(3)	GIOD1	BI	Z	Bit1 of general purpose I/O port D
	COM1	O	Z	COM1 of int. 4comX28seg LCD driver
	TCPD1	O	Z	Bit1 of TCP data bus
	LCDD1	O	Z	Bit1 of TCP2 data bus
116 116(1) 116(2) 116(3)	GIOD0	BI	Z	Bit0 of general purpose I/O port D
	COM0	O	Z	COM0 of int. 4comX28seg LCD driver
	TCPD0	O	Z	Bit0 of TCP data bus
	LCDD0	O	Z	Bit0 of TCP2 data bus
117 117(1)	MWR-	BI	H	Ext. memory write active signal
	WE-	O	H	Nand type flash write enable
118 118(1)	MRD-	BI	H	Ext. memory read active signal
	RE	O	H	Nand type flash read enable
119	A0	BI	L	Bit0 of ext. memory address bus
120 120(1)	GIOG5	BI	Z	Bit5 of general purpose I/O port G
	SEG25	O	Z	SEG25 of int. 4comX28seg LCD driver
121	A1	BI	L	Bit1 of ext. memory address bus
122	A2	BI	L	Bit2 of ext. memory address bus
123	A3	BI	L	Bit3 of ext. memory address bus
124	A4	BI	L	Bit4 of ext. memory address bus
125	A5	BI	L	Bit5 of ext. memory address bus
126 126(1)	GIOG6	BI	Z	Bit6 of general purpose I/O port G
	SEG26	O	Z	SEG26 of int. 4comX28seg LCD driver
127	A6	BI	L	Bit6 of ext. memory address bus

128	A7	BI	L	Bit7 of ext. memory address bus
129	A8	BI	L	Bit8 of ext. memory address bus
130	ENMI-	SIU	H	Ext. non-maskable interrupt input
131 131(1)	GIOG7	BI	Z	Bit7 of general purpose I/O port G
	SEG27	O	Z	SEG27 of int. 4comX28seg LCD driver
132	GND	PWR	/	Digital signal ground
133	VCC	PWR		Power supply for Pads circuits (3.15v)
134	A9	BI	L	Bit9 of ext. memory address bus
135	A10	BI	L	Bit10 of ext. memory address bus
136	A11	BI	L	Bit11 of ext. memory address bus
137	SIRQ-	SIU	H	Ext. maskable interrupt input
138	A12	BI	L	Bit12 of ext. memory address bus
139	A13	BI	L	Bit13 of ext. memory address bus
140	STANDBY-	O	L	System in standby mode output signal
141	ZICEDO	O	L	Debug pin, data output from DSU
142	ZICEDI	SIU	H	Debug pin, data input to DSU
143	ZICECK	SIU	H	Debug pin, clock into DSU
144	CE2-	O	H	Ext. memory chip select 2
145	TEST	SI	L	Test mode control, 0:normal mode 1:test mode
146	ZICERST-	SIU	H	Debug pin, to reset DSU
147	CE3-	O	H	Ext. memory chip select 3
148	ZICEEN-	SIU	H	Debug pin, to enable DSU
149	CE4-	O	H	Ext. memory chip select 4
150	RESET-	SI	H	System reset input
151	A14	O	L	Bit14 of ext. memory address bus
152	CE5-	O	H	Ext. memory chip select 5
153	GND	PWR	/	Digital signal ground
154	D0	BI	Z	Bit0 of ext. memory data bus
155 155(1)	GIOA0	BI	Z	Bit0 of general purpose I/O port A
	CD0	I	Z	IDE card detection
156	D1	BI	Z	Bit1 of ext. memory data bus
157 157(1)	GIOA1	BI	Z	Bit1 of general purpose I/O port A
	IOCS16-	I	Z	IDE 8 or 16 data bus indicate

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158	D2	BI	Z	Bit2 of ext. memory data bus
159 159(1) 159(2)	GIOA2	BI	Z	Bit2 of general purpose I/O port A
	CS1-	O	Z	IDE chip select 1
	FX_SS-	O	Z	Active low slave select of FLEX decoder
160	D3	BI	Z	Bit3 of ext. memory data bus
161	D4	BI	Z	Bit4 of ext. memory data bus
162 162(1) 162(2)	GIOA3	BI	Z	Bit3 of general purpose I/O port A
	IORDY	I	Z	IDE IORDY
	FX_READY-	I	Z	FLEX decoder SPI packet ready
163	D5	BI	Z	Bit5 of ext. memory data bus
164	A25	BI	L	Bit25 of ext. memory address bus
165	VCC	PWR		Power supply for Pads circuits (3.15v)
166	D6	BI	Z	Bit6 of ext. memory data bus
167 167(1) 167(2)	GIOA4	BI	Z	Bit4 of general purpose I/O port A
	CS0-	O	Z	IDE chip select 0
	FX_SCK	O	Z	Message shift clock of FLEX decoder
168	D7	BI	Z	Bit7 of ext. memory data bus
169	CE0-	O	H	Ext. memory chip select 0
170 170(1) 170(2)	GIOA5	BI	Z	Bit5 of general purpose I/O port A
	IRQ	I	Z	IDE IRQ
	FX_MOSI	I	Z	Message input from FLEX decoder
171	CE1-	O	H	Ext. memory chip select 1
172	CE6-	O	H	Ext. memory chip select 6
173 173(1) 173(2)	GIOA6	BI	Z	Bit6 of general purpose I/O port A
	IOW-	O	Z	IDE IOW-
	FX_MOSO	O	Z	Message output to FLEX decoder
174	CE7-	O	H	Ext. memory chip select 7
175 175(1) 175(2)	GIOA7	BI	Z	Bit7 of general purpose I/O port A
	IOR-	O	Z	IDE IOR-
	FX_CKOUT1	O	Z	FLEX decoder clock (76.8KHz)
176	VDD	PWR		Power supply for core (2.35v)

Note:

PWR : power

A : analog pad

AI : analog input

AO : analog output

Z : high resistant

I : digital input

O : digital output

BI : bidirectional input/output

SI : schmitt input

SIU : schmitt input with int. pull-up resistant

DSU: Developing Support Unit

$xxx^{(m)}$: multiplex pin's function m

TCP: Tape Carrier Package , such as SEIKO EPSON LCD module

TCP2: ASIC2/3 LCD module

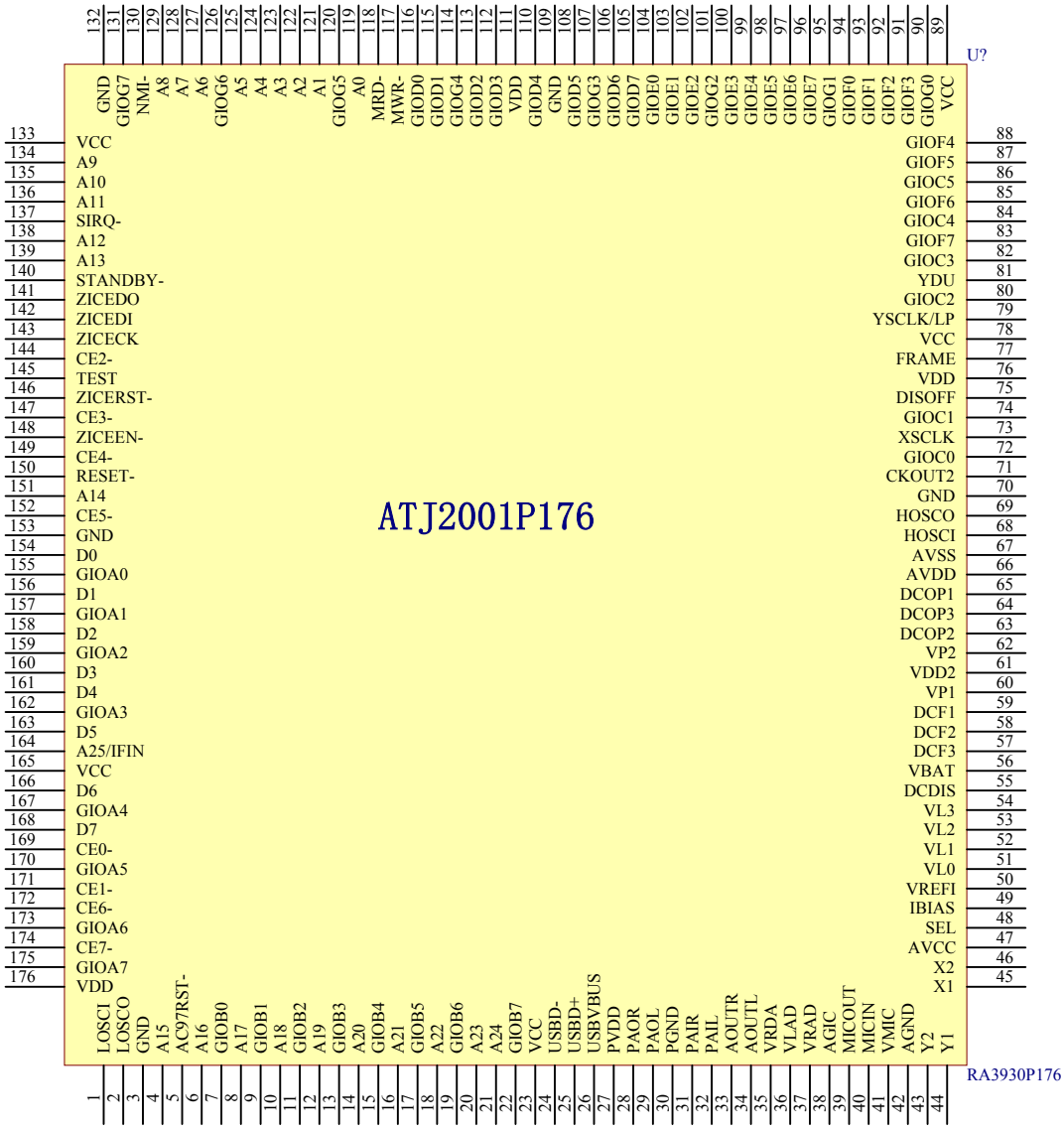
Note2: key in pads have int. pull-up resistants when key in mode enable.

note3: Avoid AC'97 ATE TEST MODE

AC'97_SYNC : output 'L' after 3 system clocks, go "Z"

AC'97_SDO : output 'L' after 3 system clocks, go "Z"

AC'97_RST- : output 'L' after 3 system clocks, go "H"



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ELECTRICAL CHARACTERISTIC

A. Absolute Maximum Ratings (TA = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	VDD	2.5V	-0.5 to +3.0	V
	VCC	3.3V	-0.5 to +3.9	V
Input voltage	Vi	VCC >= 3.3	-0.5 to +3.9	V
		VCC < 3.3	-0.5 to VCC+0.6	V
Storage temperature	Tstg		-65 to +150	℃

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings,therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.

The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

B. Capacitance (T_A = 25°C, VCC = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		15	pF

C. DC Characteristics (T_A = -10 to +70°C, VDD = 2.35 V, VCC = 3.15 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -2 mA	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
High-level input voltage	V_{IH}		0.6* VCC		VCC + 0.6	V
Low-level input voltage	V_{IL}		-0.3		0.4VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, V_I = VCC, 0 V			±10	uA
Output leakage current	I_{LO}	VCC = 3.6 V, V_I = VCC, 0 V			±5	uA
Supply Current（Two batteries		In Fullspeed mode (MCU run 24.576MHz in internal SRAM,DSP run 36MIPS)		40	60	mA

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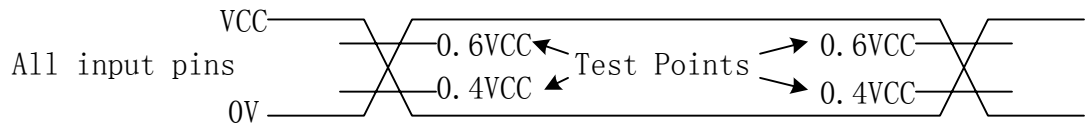
mode）	IVDD	In Standby mode	50	150	200	uA
		In Fullspeed mode (MCU run 24.576MHz in internal SRAM,DSP run 36MIPS)	9	16	40	uA
	Ivcc	In Standby mode	9	18	40	uA

Notes 1. IVDD is a total power supply current for the 2.5 V power supply. IVDD is applied to the LOGIC and PLL and OSC block.

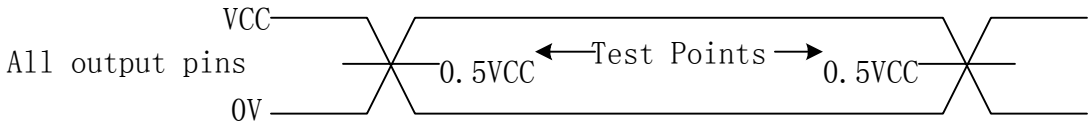
Ivcc is a total power supply current for the 3.3 V power supply. Ivcc is applied to the USB, IO, TP, and AD block.

D. AC Characteristics (TA = -10 to +70°C, VDD = 2 to 3 V, VCC = 2.7 to 3.6 V)

AC test input waveform

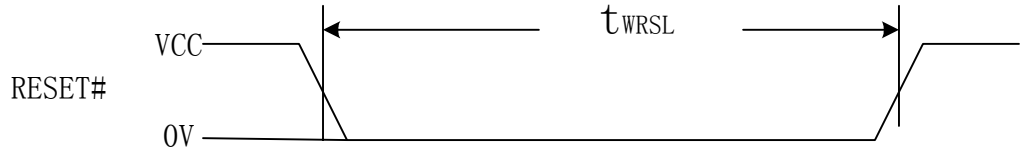


AC test output measuring points



(1) Reset parameter

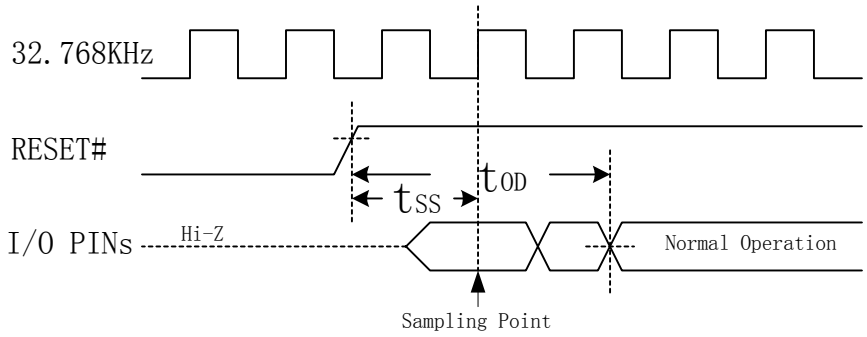
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	tWRSL	RESET# pin	160		μs



(2) Initialization parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit

Data sampling time (from RESET# ↑)	t_{SS}			61.04	μs
Output delay time (from RESET# ↑)	t_{OD}		61.04		μs



(3) GPIO interface parameter

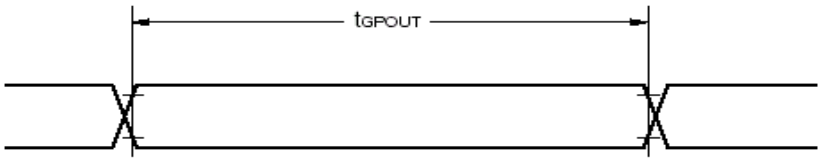
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	11/ f_{MCUclk}		μs
GPIO input rise time	t_{GPRISE}			200	ns
GPIO input fall time	t_{GPFALL}			200	ns
Output level width	t_{GPOUT}		11/ f_{MCUclk}		ns

Notes 1. f_{MCUclk} is the frequency that MCU is running upon.

(a) Input level width

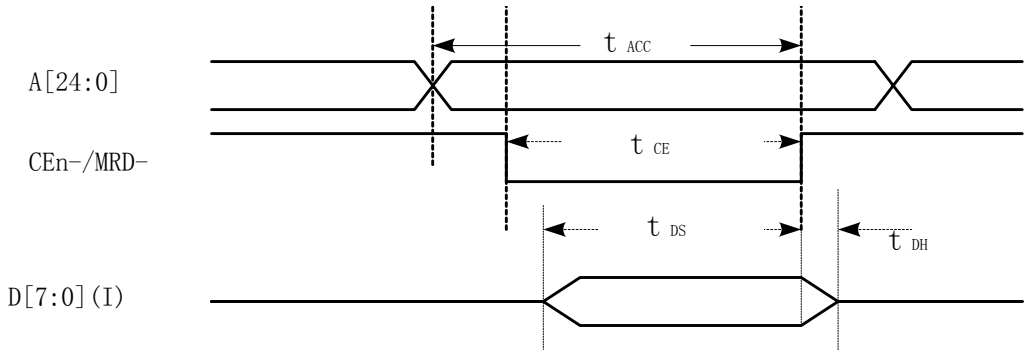
(b) Input rise/fall time

(c) Output level width



(4) Ordinary ROM parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24.576MHz	102		ns
Data access time (from CEx# ↓)Note	t_{CE}	HOSC=24.576MHz	82		ns
Data input setup time	t_{DS}	HOSC=24.576MHz	0		ns
Data input hold time	t_{DH}	HOSC=24.576MHz	0		ns



(5) External system bus parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal↓)Note 1, 2	t_{XAS}	Memory Read	0.5T		ns
	t_{XAS}	Memory Write	1.5T		ns
Address hold time (from command signal↑)Note 1, 2	t_{XAH}		0.5T		ns
Data output setup time (to command signal↓)Note 1	t_{WXDS}		0	T	ns
Data output hold time (from command signal↑)Note 1	t_{WXDH}		3	0.5T	ns
Data input setup time (to command signal↑)Note 1	t_{RXDS}		0	2T	ns
Data input hold time (from command signal↑)Note 1	t_{RXDH}		0		ns

Notes 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1000 / f_{MCUCLK}

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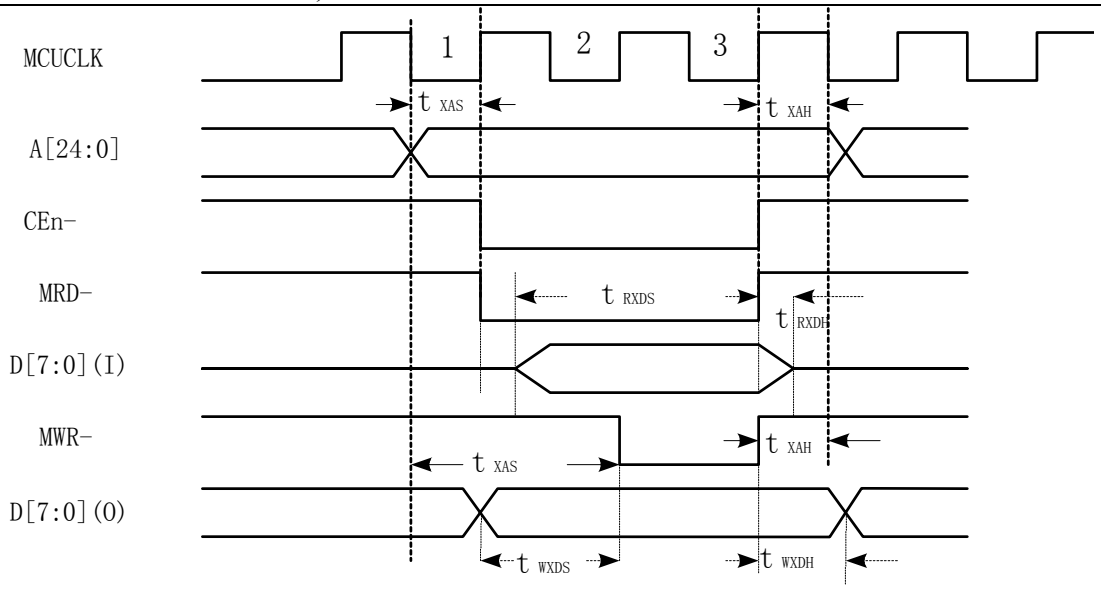
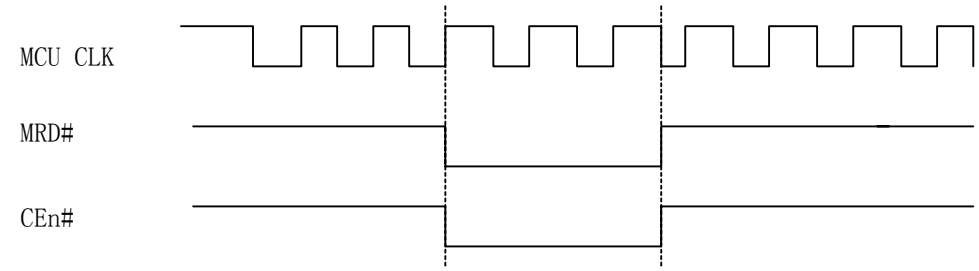
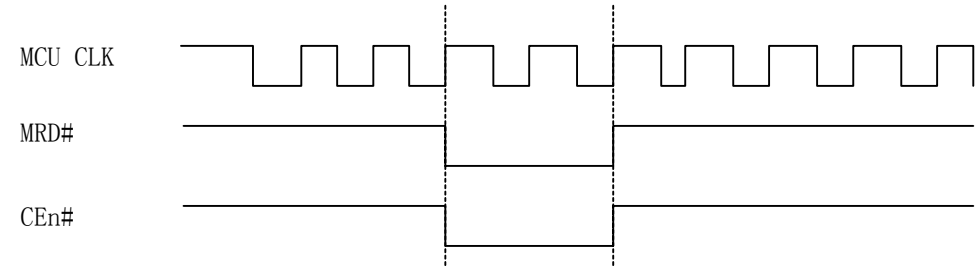


Bus Operation

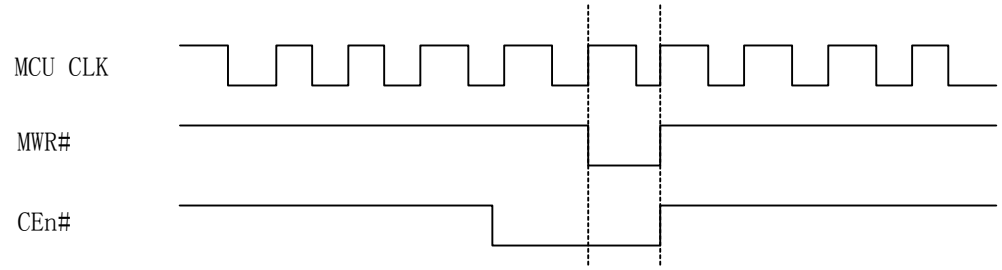
(a) Instruction fetch cycle



(b) Memory read cycle



(b) Memory write cycle



(6) Keyboard interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
KEYOUT (7:0) low-level width	t_{SCAN}	Debounce time=2.5ms	130		μs
Voltage stabilization time (KEYOUT n↑→ KEYOUT (n+1)↓)	t_{KWAIT}	Debounce time=2.5ms	0		μs
Key scan interval time	t_{KI}	Debounce time=2.5ms	130		μs
Key input delay time (from KEYOUT n↓)	t_{KS}	Debounce time=2.5ms	0		μs
Key input hold time (from KEYOUT n↑)	t_{KH}	Debounce time=2.5ms	0		μs

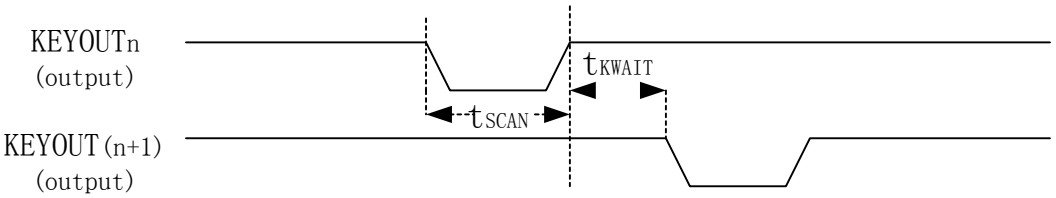
Remarks

1. KEYOUT(7:0) is multiplexed with GIOF(7:0); KEYIN(3:0) is multiplexed with GIOD(7:4); KEYIN(11:4) is multiplexed with GIOE(7:0)

2. Keyscan Debouncing time is set thru Bit(2:0) of the MFP Configuration1 Register[0xB1h]

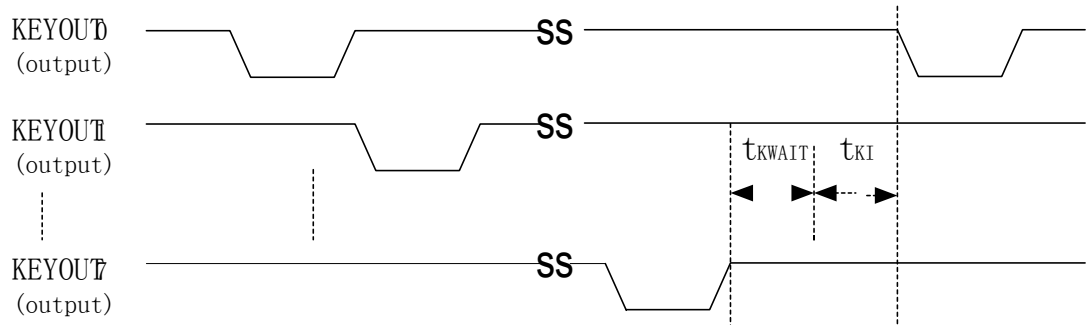
3. n = 0 to 7

(a) Keyboard scan parameter 1

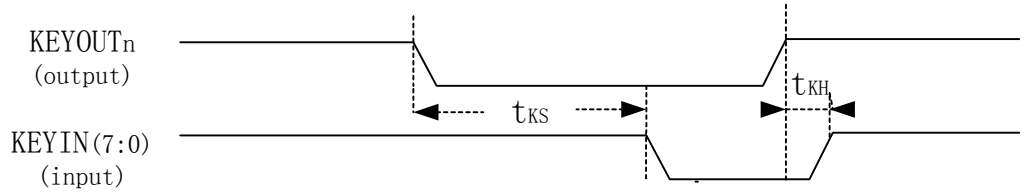


Remark n=0 to 6

(b) Keyboard scan parameter 2



(c) Keyboard port parameter



Remark n=0 to 7

(7) S/PDIF interface parameter

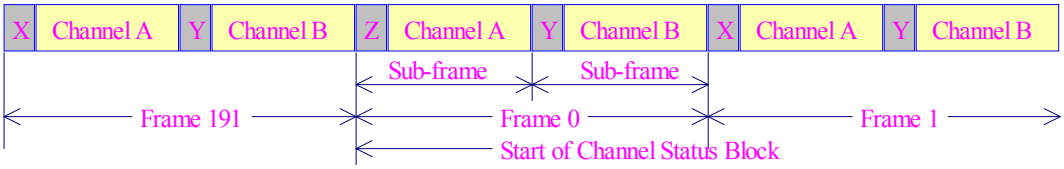


Figure 7.1. Frame/Block Format

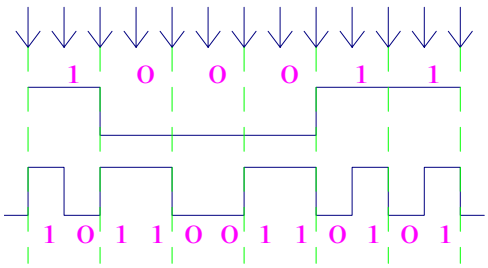


Figure 7.2. Biphase-Mark Encoding

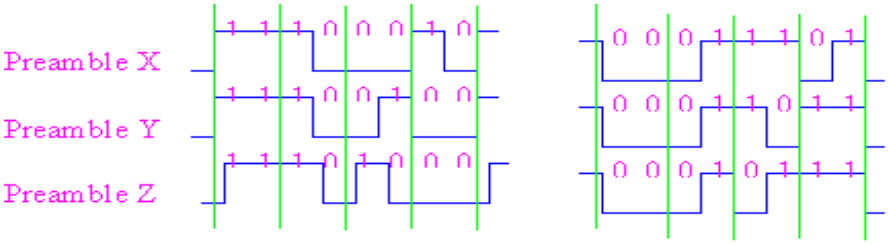


Figure 7.3. Preamble Forms

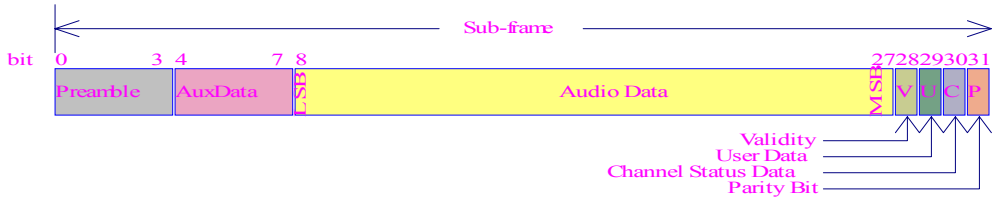


Figure 7.4. Sub-frame Format

(8) Serial interface parameter

Prescale Value	13		1.625		1	
Baud Rate	**Divisor**	**%Error**	**Divisor**	**%Error**	**Divisor**	**%Error**
600	192	0.16%	-	-	-	-
1200	96	0.16%	-	-	-	-
1800	64	0.16%	-	-	-	-
2000	58	0.53%	-	-	-	-
2400	48	0.16%	-	-	-	-
3600	32	0.16%	256	0.16%	-	-
4800	24	0.16%	192	0.16%	-	-
7200	16	0.16%	128	0.16%	208	0.16%
9600	12	0.16%	96	0.16%	156	0.16%
14400	8	0.16%	64	0.16%	104	0.16%
19200	6	0.16%	48	0.16%	78	0.16%
28800	4	0.16%	32	0.16%	52	0.16%
38400	3	0.16%	24	0.16%	39	0.16%
57600	2	0.16%	16	0.16%	26	0.16%
115200	1	0.16%	8	0.16%	13	0.16%
230400	-	-	4	0.16%	-	-
460800	-	-	2	0.16%	-	-
750000	-	-	-	-	2	0.00%
921600	-	-	1	0.16%	-	-
1500000	-	-	-	-	1	0.00%

Note :

Data transfer rate per bit, which is determined by the divisor of the baud-rate generator that is set with UART1/2 Baud Rate Registers and clock prescaler that is set with UART1/2 Control Registers.

(9) A/D Converter Characteristics (T_A = -10 to +70°C, V_{DD} = 2.0 to 3.0 V, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Zero-scale error	ZSE			±4.0		LSB
Full-scale error	RSE			±5.0		LSB
Integral linearity error	INL			±3.0		LSB
Differential linearity error	DNL			±3.0		LSB
Analog input voltage	VIAN		–0.3		AV_{DD} + 0.3	V

S/N Ratio（MAX）: 64dB

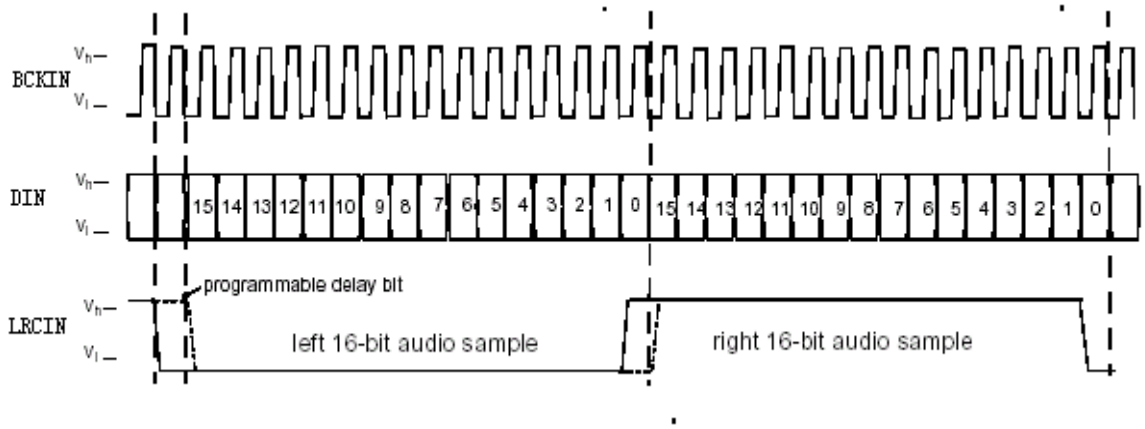
THD+N (MAX) : 55dB

(10) D/A Converter Characteristics (T_A =-10 to +70°C, V_{DD} = 2.0 to 3.0 V, V_{CC} = 2.7 to 3.6 V)

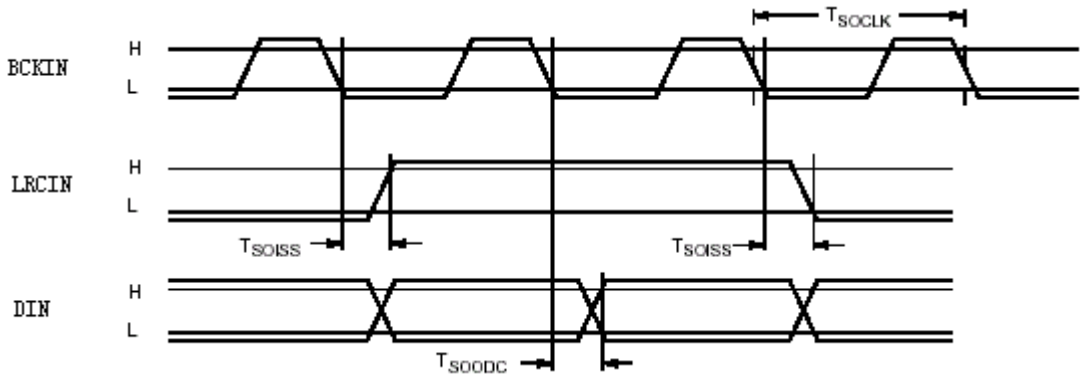
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Integral linearity error	INL			±3.0		LSB

Differential linearity error	DNL			±3.0		LSB

I²S interface parameter



Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SOCLK}	Clock Output Frequency	BCKIN		651		ns	48 kHz/s Stereo 16 bit/s
t_{SOISS}	Wordstrobe Hold Time after falling edge of clock	BCKIN, LRCIN	10		$t_{SOCLK/2}$	ns	
t_{SOODC}	Data Hold Time after falling edge of clock	BCKIN, DIN	10		$t_{SOCLK/2}$	ns	



S/N Ratio（MAX）: 90dB

THD+N (MAX) : 78dB

E. MCU/DSP Dissipation (Ivdd VS. Frequency)

1.) MCU Dissipation (Vbat=3.0V,DSP under reset, MCU runs in internal SRAM)

Clock Source	Divisor factor	Ivdd(Max)
32.768KHZ	/(1—1024)	350uA

24.576MHz	/1	8.5mA
	/2	4.7mA
	/4	2.9mA
	/8	1.8mA
	/16	1.4mA
	/32	1.1mA
	/64	0.96mA
	/128	0.88mA
	/256	0.85mA
	/512	0.84mA
	/1024	0.83mA

2.) DSP Dissipation (Vbat=3.0V,MCU in Debug mode)

DSP Speed (MIPS)	Ivdd (Max)
6	11.7mA
12	18.8mA
24	30.7mA
36	43.2mA
48	55.9mA
60	67.2mA

F. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the ATJ2001.

Table 4-1. Soldering Conditions for Surface-Mount Devices

Soldering Process	Soldering Conditions
Infrared ray reflow	Peak package's surface temperature: 235°C
	Reflow time: 30 seconds or less (210°C or more)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 3 days[Note] (10 hours of pre-baking is required at 125°C afterward).
Partial heating method	Terminal temperature: 300°C or less
	Heat time: 3 seconds or less (for one side of a device)

Note Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

NOTES FOR CMOS DEVICES

1 PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control

must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2 HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

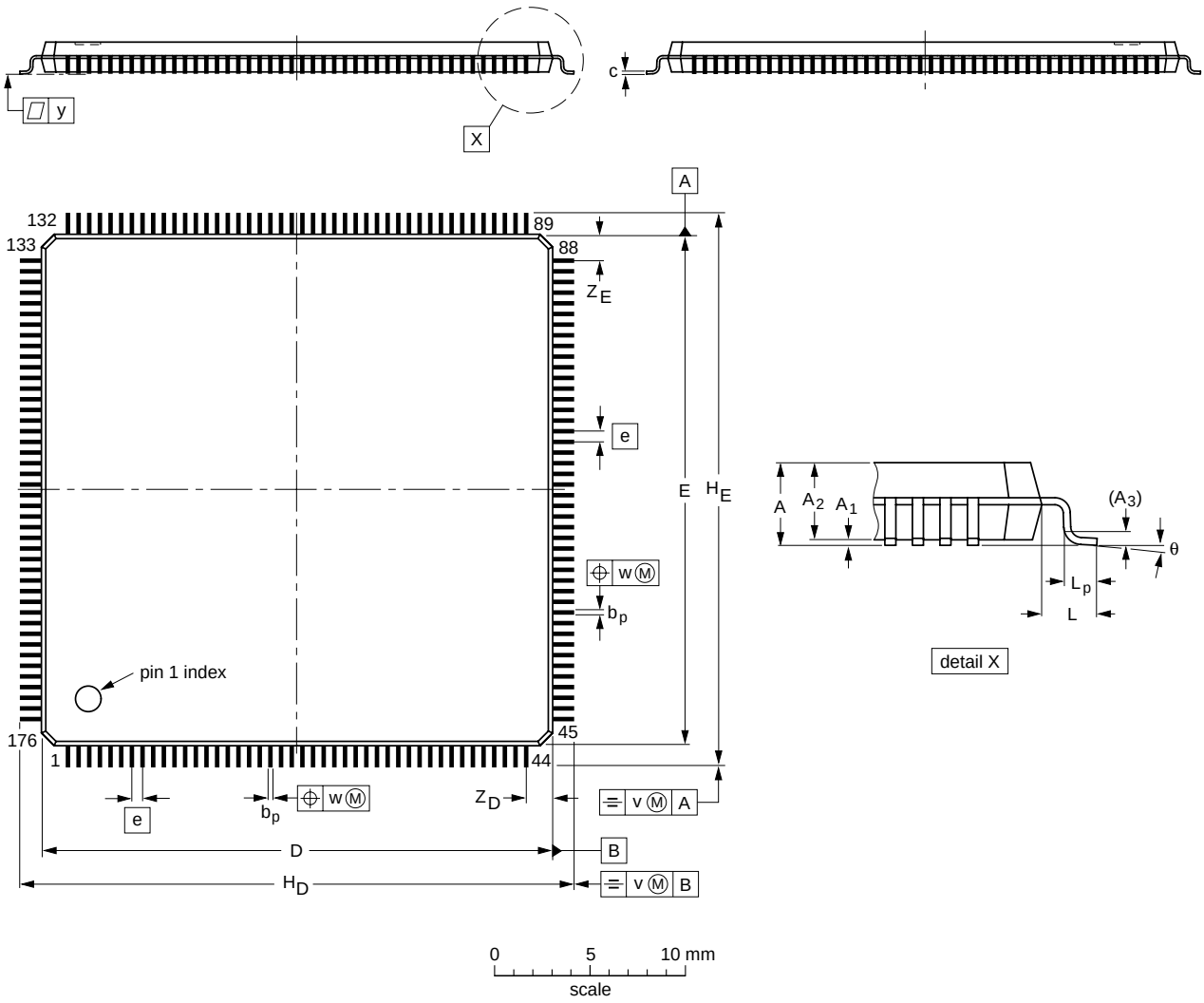
No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3 STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

LQFP176: plastic low profile quad flat package; 176 leads; body 24 x 24 x 1.4 mm **SOT506-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	24.1 23.9	24.1 23.9	0.5	26.15 25.85	26.15 25.85	1.0	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT506-1	136E25	MS-026				~~00-01-19~~ 00-02-01