

CMOS 8-Bit Microcontroller

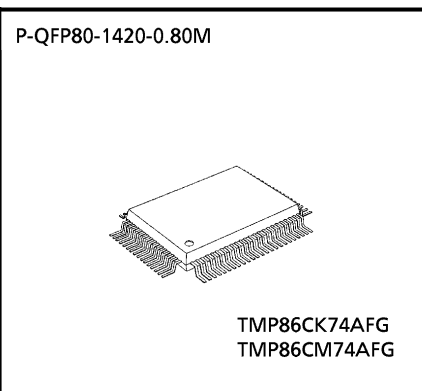
**TMP86CK74AFG/TMP86CM74AFG**

TMP86CK74A/CM74A is a low power, high-speed and high-performance 8-bit single chip microcomputer, including large capacity ROM/RAM, input/output ports, multiple timer/counter, serial interface, 8-bit AD converter and VFT (Vacume Fluorescent Tube) driver.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CK74AFG	24 K × 8 bits	1 K × 8 bits	P-QFP80-1420-0.80M	TMP86PM74AFG
TMP86CM74AFG	32 K × 8 bits	2 K × 8 bits		

**Features**

- ◆ 8-bit single chip microcomputer TLCS-870/C series
- ◆ Minimum instruction execution time : 0.25  $\mu$ S (at 16 MHz)  
122  $\mu$ S (at 32.768 kHz)
- ◆ 731 basic machine instructions : 132 types
- ◆ 17 interrupt sources (External : 6, Internal : 11 )
- ◆ Input/output ports : 70 pins
- ◆ 16-bit timer counters : 2 channels
  - TC1 : Timer, Event counter, PPG (Programmable Pulse Generator) output, Pulse width measurement, External trigger timer, and Window modes
  - TC2 : Timer, Event counter, Window modes
- ◆ 8-bit timer counters : 2 channels
  - TC3 : Timer, Event counter, Capture modes (Pulse width/duty measurement).
  - TC4 : Timer, Event counter, PWM (Pulse width modulation) Output , PDO (Programmable Divider Output)



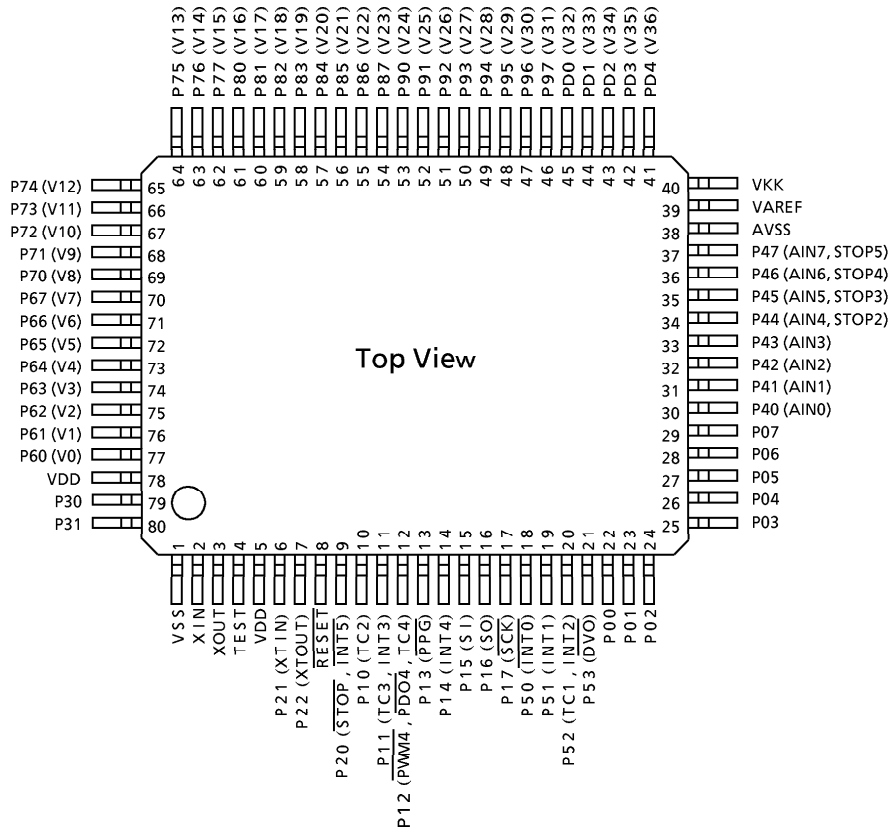
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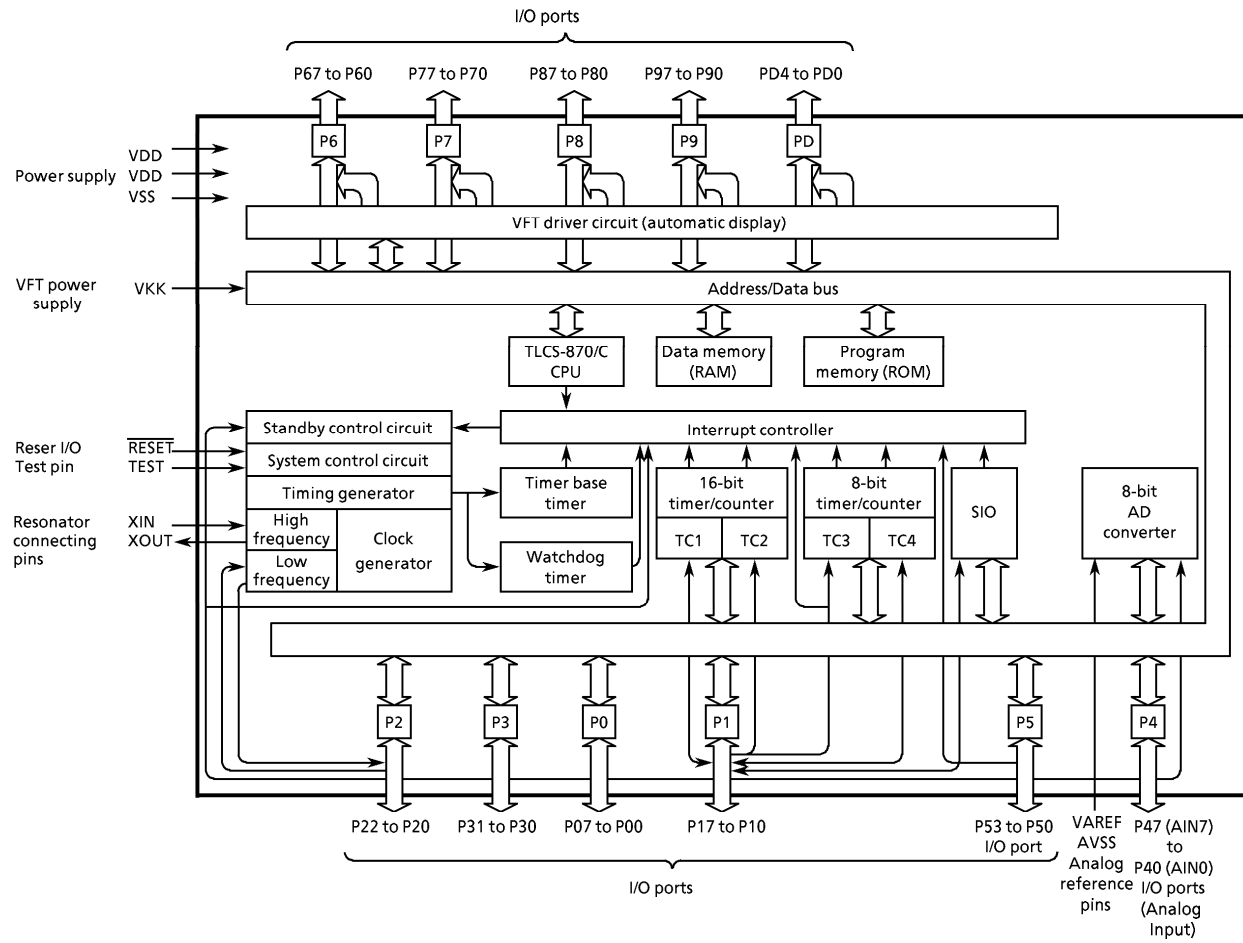
- ◆ Time base timer
- ◆ Watchdog timer
  - Interrupt source
- ◆ Divider output function
- ◆ 4 Key-on wake up pins
- ◆ Serial interface
  - 8-bit SIO : 1 channel (with 32 bytes Buffer)
- ◆ 8-bit successive approximation type AD converter
  - Analog input : 8 channels
- ◆ Vacuum fluorescent tube driver (automatic display)
  - Programmable grid scan
  - High breakdown voltage ports (max 40 V × 37 bits)
- ◆ Low consumption power (9 modes)
  - STOP mode : Oscillation stop (Battery/Capacitor back-up).
  - SLOW1 mode : Low consumption power operation by low-frequency clock (High-frequency clock stop.)
  - SLOW2 mode : Low consumption power operation by low-frequency clock (High-frequency clock oscillate.)
  - IDLE0 mode : CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer.  
Release by INTTBT interrupt.
  - IDLE1 mode : CPU stops, and peripherals operate using high-frequency clock.  
Release by interrupts.
  - IDLE2 mode : CPU stops, and peripherals operate using high and low-frequency clock.  
Release by interrupts.
  - SLLEP0 mode : CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer.  
Release by INTTBT interrupt.
  - SLEEP1 mode : CPU stops, and peripherals operate using low-frequency clock.  
Release by interrupts.
  - SLEEP2 mode : CPU stops, and peripherals operate using high and low-frequency clock.  
Release by interrupts.
- ◆ Dual clock operation
  - Single/Dual-clock mode
- ◆ Wide operating voltage : 4.5 V to 5.5 V at 16 MHz/32.768 kHz  
2.7 V to 5.5 V at 8 MHz/32.768 kHz

Pin Assignments (Top View)

P-QFP80-1420-0.80M



Block Diagram



## Pin Functions

Pin Name	I/O	Function	
P00 P01 P02 P03 P04 P05 P06 P07	I/O	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	—
P10 (TC2)	I/O (Input)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	External input for TC1
P11 (TC3/INT3)			External input for TC1 External interrupt input3
P12 (PWM4/PDO4/TC4)	I/O (Output, Output, Input)	When used as serial data input, external interrupt input, timer/counter input, the input mode is configured.	PWM output PDO output External input for TC4
P13 (PPG)	I/O (Output)	When used as PWM output, PDO output, PPG output, serial data output, serial clock Output, the latch must be set to "1" and the Output mode is configured.	PPG output
P14 (INT4)	I/O (Input)		External interrupt input4
P15 (SI)	I/O (Input)	When used as open-drain port, P1OUTCR Set to "0". When used as CMOS port, P1OUTCR set to "1".	Serial data input
P16 (SO)	I/O (Output)		Serial data input
P17 (SCK)	I/O (I/O)		Serial clock input/output
P20 (INT5/STOP)	I/O ( Input)	3-bit input/output port. Each bit of this port can be individually configured as an input or an output under software control.	External interrupt input5 STOP mode rerease signal input
P21 (XTIN)	I/O (Input)		Low resonator connection pin (32.768 kHz). For external clock, XTIN is used and XTOUT is opened
P22 (XTOUT)	I/O (Output)		
P30 P31	I/O	2-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	—
P40 (AIN0) P41 (AIN1) P42 (AIN2) P43 (AIN3)	I/O (Input)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	AD converter analog input
P44 (AIN4/STOP2) P45 (AIN5/STOP3) P46 (AIN6/STOP4) P47 (AIN7/STOP5)			I/O (Input, Input)
P50 (INT0) P51 (INT1) P52 (TC1/INT2)	I/O (Input)	4-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	External interrupt input0 External interrupt input1 External input for TC1 External interrupt input2
P53 (DVO)			I/O (Output)

Pin Name	I/O	Function	
P60 (V0) P61 (V1) P62 (V2) P63 (V3) P64 (V4) P65 (V5) P66 (V6) P67 (V7)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Grid output
P70 (V8) P71 (V9) P72 (V10) P73 (V11) P74 (V12) P75 (V13) P76 (V14) P77 (V15)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Grid output
P80 (V16) P81 (V17) P82 (V18) P83 (V19) P84 (V20) P85 (V21) P86 (V22) P87 (V23)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Segment output
P90 (V24) P91 (V25) P92 (V26) P93 (V27) P94 (V28) P95 (V29) P96 (V30) P97 (V31)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Segment output
PD0 (V32) PD1 (V33) PD2 (V34) PD3 (V35) PD4 (V36)	I/O (Output)	5-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Segment output
TEST	Input	Test pin for out-going test. Be tied to low.	
RESET	Input	Reset signal input.	
XIN	Input	Resonator connecting pins for high-frequency clock.	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
VSS	Power supply	0.0 [V] (GND)	
VDD		Power supply	
AVSS		Analog reference voltage (GND: 0.0 [V])	
VAREF		Analog reference voltage	
VKK		VFT driver power supply	

## Operational Description

### 1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

#### 1.1 Memory Address Map

The memory of TMP86CK74A/CM74A consists of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64 Kbyte address space. Figure 1-1 shows the memory address map of TMP86CK74A/CM74A. The general-purpose registers are not assigned to the RAM address space.

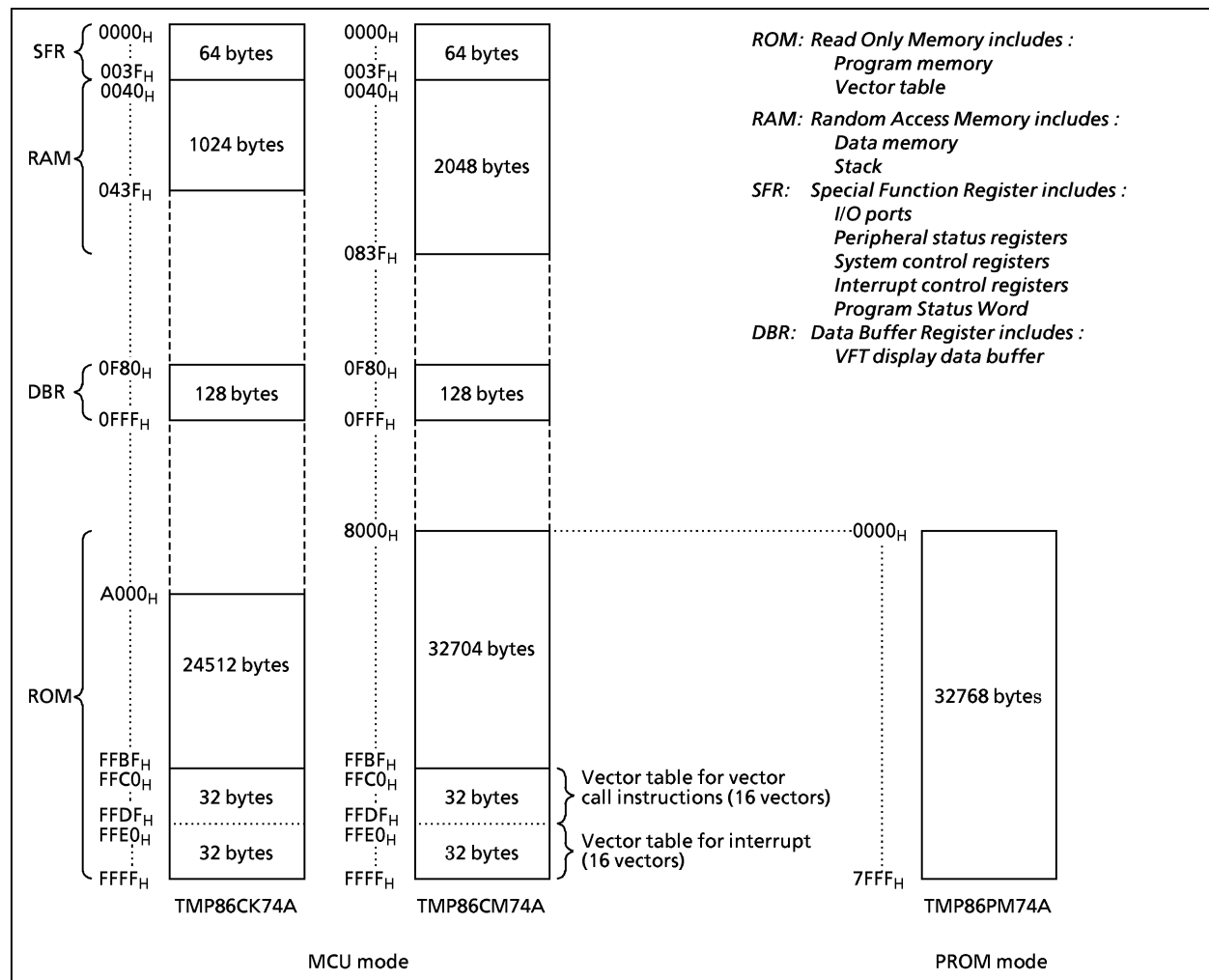


Figure 1-1. Memory Address Maps

#### 1.2 Program Memory (ROM)

The TMP86CK74A has an 24 K×8 bits (address A000H to FFFFH) of program memory, the TMP86CM74A has 32 K×8 bits (address 8000H to FFFFH) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

## Electrical Characteristics

Absolute Maximum Ratings		(VSS = 0 V)			
Parameter	Symbol	Pins	Ratings	Unit	
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	V	
Program voltage	V <sub>PP</sub>	TEST/VPP pin	- 0.3 to 13.0		
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3		
Output Voltage	V <sub>OUT1</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V	
	V <sub>OUT2</sub>	Source open drain port	V <sub>DD</sub> - 41 to V <sub>DD</sub> + 0.3		
Output Current (Per 1 pin)	IOL	I <sub>OUT1</sub>	P0, P01, P2, P4, P5 ports	5	mA
		I <sub>OUT2</sub>	P3 port	40	
	IOH	I <sub>OUT3</sub>	P0, P1, P4, P5 ports	- 3	
		I <sub>OUT4</sub>	P6, P7 ports	- 30	
		I <sub>OUT5</sub>	P8, P9, PD ports	- 20	
Output Current (Total)	IOL	ΣI <sub>OUT1</sub>	P0, P1, P2, P4, P5 ports	120	mA
	IOH	ΣI <sub>OUT4</sub>	P6, P7, P8, P9, PD ports	- 120	
Power Dissipation [Topr = 25°C]	PD		1200	mW	
Soldering Temperature (time)	Tsld		260 (10 s)	°C	
Storage Temperature	Tstg		- 55 to 125		
Operating Temperature	Topr		- 30 to 70		

**Note 1 :** The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum ratings is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products, which include this device, ensure that no absolute maximum rating value will ever be exceeded.

**Note 2 :** All VDDs should be connected externally for keeping the same voltage level.

**Note 3 :** Power Dissipation (PD); For PD, it is necessary to decrease - 14.3 mW/°C.



## Recommended Operating Conditions

Parameter	Symbol	Pins	Condition	Min	Max	Unit	
Supply Voltage	$V_{DD}$		$f_c = 16 \text{ MHz}$	NORMAL1, 2 modes	4.5	5.5	
				IDLE1, 2 modes			
			$f_c = 8 \text{ MHz}$	NORMAL1, 2 modes	2.7		
				IDLE1, 2 modes			
			$f_s = 32.768 \text{ kHz}$	SLOW mode			
				SLEEP mode			
	STOP mode						
Output Voltage	$V_{OUT3}$	Source open drain pins		$V_{DD} - 38$	$V_{DD}$	V	
Input High Voltage	$V_{IH1}$	Except hysteresis input		$V_{DD} \times 0.70$	$V_{DD}$		
	$V_{IH2}$	Hysteresis input		$V_{DD} \times 0.75$			
Input Low Voltage	$V_{IL1}$	Except hysteresis input		0	$V_{DD} \times 0.30$		
	$V_{IL2}$	Hysteresis input			$V_{DD} \times 0.25$		
Clock Frequency	$f_c$	XIN, XOUT	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	1.0	8.0	MHz	
			$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$		16.0		
	$f_s$	XTIN, XTOUT		30.0	34.0	kHz	

*Note : The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products, which include this device, ensure that the recommended operating conditions for the device are always adhered to.*

### How to Calculate Power Consumption.

The share of VFT driver loss (VFT driver output loss + pull-down resistor (RK) loss) in power consumption  $P_{max}$  of

TMP86CK74/CM74 is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption  $P_d$  must not be exceeded.

Power consumption  $P_{max}$  = operating power consumption + normal output port loss + VFT driver loss.

Where,

$$\begin{aligned} \text{Operating power consumption: } & V_{DD} \times I_{DD} \\ \text{Normal output port loss} & : \Sigma I_{OUT1} \times 0.4 \\ \text{VFT driver loss} & : \text{VFT driver output loss + pull-down resistor (RK) loss} \end{aligned}$$

Example :

When  $T_a = -10$  to  $50^\circ\text{C}$  (When using a fluorescent display tube with a conventional type which can use only one grid output at the same time.) and a fluorescent display tube with segment output = 3mA, digit output = 12mA,  $V_{kk} = -34.5\text{V}$  is used.

Operating conditions ;  $V_{DD} = 5\text{V} \pm 10\%$ ,  $f_c = 8\text{MHz}$ , VFT dimmer time (DIM) =  $(14/16) \times t_{seg}$ ,

Power consumption  $P_{max} = (1) + (2) + (3)$

Where,

$$\begin{aligned} (1) \text{ Operating power consumption: } & V_{DD} \times I_{DD} = 5.5\text{V} \times 10\text{mA} = 55\text{mW} \\ (2) \text{ Normal output port loss} & : \Sigma I_{OUT2} \times 0.4 = 60\text{mA} \times 0.4\text{V} = 24\text{mW} \\ (3) \text{ VFT driver loss} & : \text{Segment pin} = 3\text{mA} \times 2\text{V} \times \text{number of segments } X = 6\text{mW} \times X \\ & \text{Grid pin} = 12\text{mA} \times 2\text{V} \times 14/16 \text{ (DIM)} \times \text{number of grids } Y \\ & = 21\text{mW} \times Y \\ & R_k \text{ loss} = (5.5\text{V} + 34.5\text{V})^2 / 50\text{k}\Omega \times (\text{number of segments } X + \\ & \text{number of grids } Y) = 32\text{mW} \times (X + Y) \end{aligned}$$

$$\begin{aligned} \text{Therefore, } P_{max} & = 55\text{mW} + 24\text{mW} + 6\text{mW} \times X + 21\text{mW} \times Y + 32\text{mW} \times (X + Y) \\ & = 132\text{mW} + 38\text{mW} \times X \dots \end{aligned}$$

Maximum power consumption  $P_d$  when  $T_a = 50^\circ\text{C}$  is determined by the following equation ;

$$P_D = 1200\text{mW} - (14.3 \times 25) = 842.5\text{mW}$$

The number of segments  $X$  that can be lit is:

$$\begin{aligned} P_D & > P_{max} \\ 842.5\text{mW} & > 132 + 38X \\ 18.69 & > X \end{aligned}$$

Thus, a fluorescent display tube with less than 18 segments can be used. If a fluorescent display tube with 18 segments or more is used, either a pull-down resistor must be attached externally, or the number of segments to be lit must be kept to less than 18 by software.

## DC Characteristics

(V<sub>DD</sub> = 5 V)

[Condition] V<sub>DD</sub> = 5.0 V ± 10%, V<sub>SS</sub> = A<sub>VSS</sub> = 0 V, T<sub>opr</sub> = -30 to 70°C  
 (Typ. : V<sub>DD</sub> = 5.0 V, T<sub>opr</sub> = 25°C, V<sub>in</sub> = 5.0 V/0V)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit		
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis input		-	0.9	-	V		
Input Current	I <sub>IN1</sub>	TEST	V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5V / 0 V	-	-	± 2	μA		
	I <sub>IN2</sub>	Sink Open-drain, Tri-st							
	I <sub>IN3</sub>	RESET, STOP							
Input resistance	R <sub>IN</sub>	RESET Pull-UP		100	220	450	kΩ		
Pull-down resistance	R <sub>K</sub>	Source Open Drain	V <sub>DD</sub> = 5.5 V, V <sub>KK</sub> = -30 V	50	80	110			
Output Leakage Current	I <sub>LO1</sub>	Sink Open-drain, Tri-st	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	-	-	± 2	μA		
	I <sub>LO2</sub>	Source Open-drain	V <sub>DD</sub> = 5.5 V, V <sub>KK</sub> = -32 V	-	-	± 2			
Output High Voltage	V <sub>OH</sub>	Tri-st	V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = -0.7 mA	4.1	-	-	V		
Output Low Voltage	V <sub>OL1</sub>	Except XOUT, P3	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA	-	-	0.4			
Output High Current	I <sub>OH1</sub>	P6, P7	V <sub>DD</sub> = 4.5 V, V <sub>OH</sub> = 2.4 V	- 18	- 28	-	mA		
	I <sub>OH2</sub>	P8, P9, PD	V <sub>DD</sub> = 4.5 V, V <sub>OH</sub> = 2.4 V	- 9	- 14	-			
Output Low Current	I <sub>OL</sub>	High-current (P3)	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	-	20	-			
Supply Current in NORMAL1, 2 modes	I <sub>DD</sub>		f <sub>c</sub> = 16.0 MHz f <sub>s</sub> = 32.768 KHz	AD converter Disable (IREF off)	-	12	18	mA	
Supply Current in IDLE0, 1, 2 modes					f <sub>c</sub> = 8.0 MHz f <sub>s</sub> = 32.768 KHz	-	6		9
			Supply Current in NORMAL1, 2 modes	f <sub>c</sub> = 16.0 MHz f <sub>s</sub> = 32.768 KHz		-	6		9
f <sub>c</sub> = 8.0 MHz f <sub>s</sub> = 32.768 KHz					AD converter Enable	-	3		4.5
			f <sub>c</sub> = 16.0 MHz f <sub>s</sub> = 32.768 KHz	AD converter Enable		-	13		19
f <sub>c</sub> = 8.0 MHz f <sub>s</sub> = 32.768 KHz					AD converter Enable	-	7		10
			Supply Current in STOP mode			T <sub>opr</sub> = to 50 °C	AD converter Disable	-	0.5
T <sub>opr</sub> = to 70 °C					-			0.5	10

Note 1 : Typical values show those at T<sub>opr</sub> = 25°C, V<sub>DD</sub> = 5V.

Note 2 : Input current (I<sub>IN1</sub>, I<sub>IN3</sub>) ; The current through pull-up or pull-down resistor is not included.

Note 3 : I<sub>DD</sub> does not include IREF current.

## DC Characteristics

(V<sub>DD</sub> = 3 V)

[Condition] V<sub>DD</sub> = 3.0 V ± 10%, V<sub>SS</sub> = A<sub>VSS</sub> = 0 V, T<sub>opr</sub> = -30 to 70°C  
 (Typ. : V<sub>DD</sub> = 3.0 V, T<sub>opr</sub> = 25°C, V<sub>in</sub> = 3.0 V/0V)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit	
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis input		-	0.4	-	V	
Input Current	I <sub>IN1</sub>	TEST	V <sub>DD</sub> = 3.3 V, V <sub>IN</sub> = 3.3 V/0 V	-	-	± 2	μA	
	I <sub>IN2</sub>	Sink Open-drain, Tri-st						
	I <sub>IN3</sub>	RESET, STOP						
Input resistance	R <sub>IN</sub>	RESET Pull-Up		100	220	450	kΩ	
Pull-down resistance	R <sub>K</sub>	Source Open Drain	V <sub>DD</sub> = 3.3 V, V <sub>KK</sub> = -30 V	45	70	105		
Output Leakage Current	I <sub>LO1</sub>	Sink Open-drain, Tr-st	V <sub>DD</sub> = 3.3 V, V <sub>OUT</sub> = 3.3 V/0 V	-	-	± 2	μA	
	I <sub>LO2</sub>	Source Open-drain	V <sub>DD</sub> = 3.3 V, V <sub>KK</sub> = -32 V	-	-	± 2		
Output High Voltage	V <sub>OH</sub>	Tri-st	V <sub>DD</sub> = 2.7 V, I <sub>OH</sub> = -0.6 mA	2.3	-	-	V	
Output Low Voltage	V <sub>OL1</sub>	Except XOUT, P3	V <sub>DD</sub> = 2.7 V, I <sub>OL</sub> = 0.9 mA	-	-	0.4		
Output High Current	I <sub>OH1</sub>	P6, P7	V <sub>DD</sub> = 2.7 V, V <sub>OH</sub> = 1.5 V	-5.5	-8	-	mA	
	I <sub>OH2</sub>	P8, P9, PD	V <sub>DD</sub> = 2.7 V, V <sub>OH</sub> = 1.5 V	-3	-4.5	-		
Output Low Current	I <sub>OL</sub>	High-current (P3)	V <sub>DD</sub> = 2.7 V, V <sub>OL</sub> = 1.0 V	-	6	-		
Supply Current in NORMAL1, 2 modes	I <sub>DD</sub>		fc = 8.0 MHz fs = 32.768 KHz	AD converter Disable (IREF off)	-	3		4.5
Supply Current in IDLE0, 1, 2 modes			fc = 8.0 MHz fs = 32.768 KHz	AD converter Enable	-	2		2.5
Supply Current in NORMAL1, 2 modes			fc = 8.0 MHz fs = 32.768 KHz	AD converter Enable	-	3.5		5
Supply Current in SLOW1, 2 modes			fs = 32.768 KHz	AD converter Disable	-	3	60	
Supply Current in SLEEP0, 1, 2 modes			T <sub>opr</sub> = to 50 °C		-	15	30	
Supply Current in STOP mode			T <sub>opr</sub> = to 70 °C		-	0.5	5	
						10		

Note 1 : Typical values show those at T<sub>opr</sub> = 25°C, V<sub>DD</sub> = 3V.

Note 2 : Input current (I<sub>IN1</sub>, I<sub>IN3</sub>) ; The current through pull-up or pull-down resistor is not included.

Note 3 : I<sub>DD</sub> does not include I<sub>REF</sub> current.

Note 4 : The supply currents of SLOW2 and SLEEP2 modes are equivalent to IDLE0, 1, 2.

## AD Characteristics

( $V_{SS} = A_{VSS} = 0\text{ V}$ ,  $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	$V_{AREF}$		$V_{DD} - 1.5$	–	$V_{DD}$	V
Analog Reerence Voltage Range	$\Delta V_{AREF}$		3.0	–	–	
Analog Input Voltage	$V_{AIN}$		0	–	$V_{AREF}$	V
Analog Supply Current	$I_{REF}$	$V_{DD} = V_{AREF} = 5.5\text{ V}$ , $V_{SS} = 0.0\text{ V}$	–	0.6	1.0	mA
Non linearity Error		$V_{DD} = V_{AREF} = 4.5\text{ to }5.5\text{ V}$ , $V_{SS} = 0\text{ V}$	–	–	$\pm 1$	LSB
Zero Point Error			–	–	$\pm 1$	
Full Scale Error			–	–	$\pm 1$	
Total Error			–	–	$\pm 2$	

( $V_{SS} = A_{VSS} = 0\text{ V}$ ,  $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	$V_{AREF}$		$V_{DD} - 1.5$	–	$V_{DD}$	V
Analog Reerence Voltage Range	$\Delta V_{AREF}$		2.5	–	–	
Analog Input Voltage	$V_{AIN}$		0	–	$V_{AREF}$	V
Analog Supply Current	$I_{REF}$	$V_{DD} = V_{AREF} = 4.5\text{ V}$ , $V_{SS} = 0.0\text{ V}$	–	0.5	0.8	mA
Non linearity Error		$V_{DD} = V_{AREF} = 2.7\text{ to }4.5\text{ V}$ , $V_{SS} = 0\text{ V}$	–	–	$\pm 1$	LSB
Zero Point Error			–	–	$\pm 1$	
Full Scale Error			–	–	$\pm 1$	
Total Error			–	–	$\pm 2$	

**Note 1 :** Total errors includes all errors, except quantization error, and is defined as a maximum deviation from the ideal conversion line.

**Note 2 :** Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".

**Note 3 :** Please use input voltage to AIN input pin in limit of  $V_{AREF} - V_{SS}$ . When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

**Note 4 :** Analog Reference Voltage Range;  $\Delta V_{AREF} = V_{AREF} - V_{SS}$

## AC Characteristics

( $V_{SS} = 0\text{ V}$ ,  $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcyc	NORMAL1,2 mode	0.25	-	4	$\mu\text{s}$
		IDLE0,1,2 mode				
		SLOW1,2 mode	117.6	-	133.3	
		SLEEP0,1,2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)	-	31.25	-	ns
Low Level Clock Pulse Width	twcL	fc = 16 MHz	-	15.26	-	$\mu\text{s}$
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	-	15.26	-	$\mu\text{s}$
Low Level Clock Pulse Width	twcL	fs = 32.768 kHz	-	15.26	-	$\mu\text{s}$

( $V_{SS} = 0\text{ V}$ ,  $2.7\text{ V} \leq V_{DD} \leq 4.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70^\circ\text{C}$ )

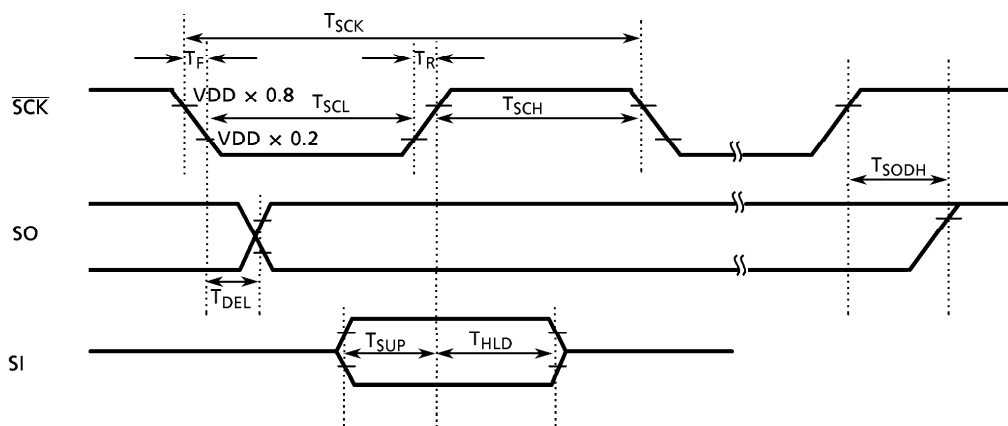
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcyc	NORMAL1,2 mode	0.5	-	8	$\mu\text{s}$
		IDLE0,1,2 mode				
		SLOW1,2 mode	117.6	-	133.3	
		SLEEP0,1,2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)	-	62.5	-	ns
Low Level Clock Pulse Width	twcL	fc = 8 MHz	-	15.26	-	$\mu\text{s}$
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	-	15.26	-	$\mu\text{s}$
Low Level Clock Pulse Width	twcL	fs = 32.768 kHz	-	15.26	-	$\mu\text{s}$

HSIO AC Characteristics

( $V_{SS} = 0\text{ V}$ ,  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit	
$\overline{\text{SCK}}$ output period (internal clock)	$T_{\text{SCK1}}$	$8\text{ MHz} < f_c \leq 16\text{ MHz}$ $V_{DD} = 4.5\text{ V to }5.5\text{ V}$	16/fc	-	-	s	
$\overline{\text{SCK}}$ output low width (internal clock)	$T_{\text{SCL1}}$		8/fc - 100ns	-	-		
$\overline{\text{SCK}}$ output high width (internal clock)	$T_{\text{SCH1}}$		8/fc - 100ns	-	-		
$\overline{\text{SCK}}$ output period (internal clock)	$T_{\text{SCK2}}$	$4\text{ MHz} < f_c \leq 8\text{ MHz}$ $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	8/fc	-	-		
$\overline{\text{SCK}}$ output low width (internal clock)	$T_{\text{SCL2}}$		4/fc - 100ns	-	-		
$\overline{\text{SCK}}$ output high width (internal clock)	$T_{\text{SCH2}}$		4/fc - 100ns	-	-		
$\overline{\text{SCK}}$ output period (internal clock)	$T_{\text{SCK3}}$	$f_c \leq 4\text{ MHz}$ $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	4/fc	-	-		
$\overline{\text{SCK}}$ output low width (internal clock)	$T_{\text{SCL3}}$		2/fc - 100ns	-	-		
$\overline{\text{SCK}}$ output high width (internal clock)	$T_{\text{SCH3}}$		2/fc - 100ns	-	-		
$\overline{\text{SCK}}$ input period (external clock)	$T_{\text{SCK4}}$	$f_c \leq 8\text{ MHz}$ ( $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ )	1000	-	-	ns	
$\overline{\text{SCK}}$ input low width (external clock)	$T_{\text{SCL4}}$		$f_c \leq 16\text{ MHz}$ ( $V_{DD} = 4.4\text{ V to }5.5\text{ V}$ )	400	-		-
$\overline{\text{SCK}}$ input low width (external clock)	$T_{\text{SCH4}}$			400	-		-
SI input setup time	$T_{\text{SUP}}$		200	-	-		
SI input hold time	$T_{\text{HLD}}$		200	-	-		
SO output delay time	$T_{\text{DEL}}$		-	-	200		
Rising time	$T_{\text{R}}$	$V_{DD} = 3.0\text{ V}$ , $CL = 50\text{ pF}$ (Note)	-	-	100		
Falling time	$T_{\text{F}}$		-	-	100		
SO last bit hold time	$T_{\text{SODH}}$		16.5/fc	-	32.5/fc		

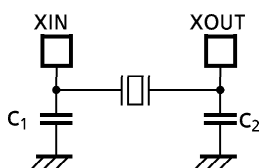
Note: CL, External Capacitance



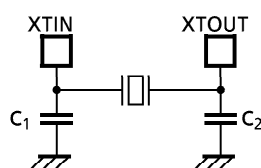
**Recommended Oscillating Conditions**

(V<sub>SS</sub> = 0 V, Topr = - 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant	
					C <sub>1</sub>	C <sub>2</sub>
High-frequency Oscillation	Ceramic Resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040	10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
4.19 MHz	2.7 V to 5.5 V	MURATA CSA4.19MG	30 pF	30 pF		
		CST4.19MGW	30 pF (built-in)	30 pF (built-in)		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	2.7 V to 5.5 V	SII VT-200	6 pF	6 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

*Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.*

*Note2: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.*

*Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.*

*For up-to-date information, please refer to the following URL;*

*<http://www.murata.co.jp/search/index.html>*