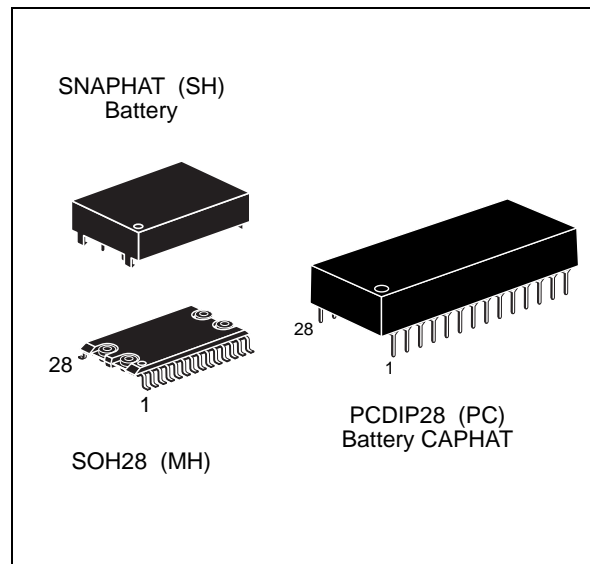


## 64Kb (8K x 8) ZEROPOWER<sup>®</sup> SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- MICROPROCESSOR POWER-ON RESET (Valid even during battery back-up mode)
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES ( $V_{PFD}$  = Power-fail Deselect Voltage):
  - M48Z59:  $4.50V \leq V_{PFD} \leq 4.75V$
  - M48Z59Y:  $4.20V \leq V_{PFD} \leq 4.50V$
- SELF-CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- PACKAGING INCLUDES a 28-LEAD SOIC and SNAPHAT<sup>®</sup> TOP (to be Ordered Separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT TOP which CONTAINS the BATTERY and CRYSTAL
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs



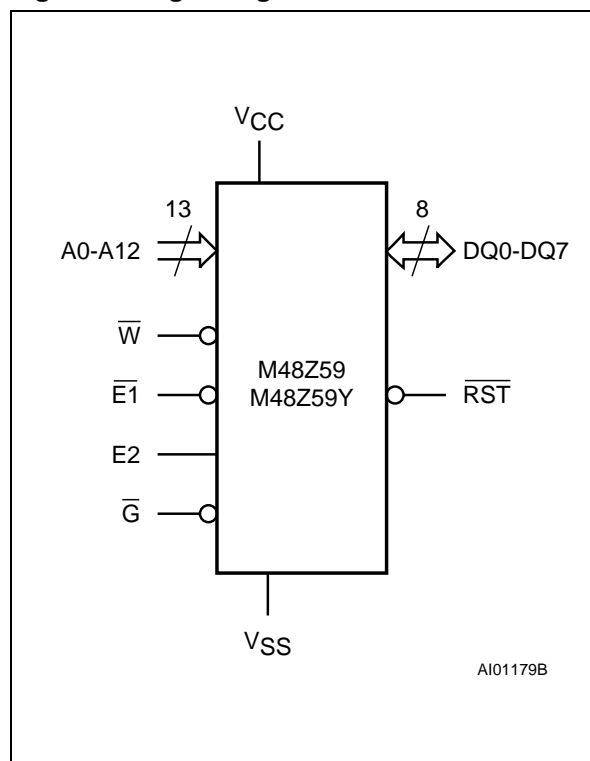
### DESCRIPTION

The M48Z59/59Y ZEROPOWER<sup>®</sup> RAM is an 8K x 8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

**Table 1. Signal Names**

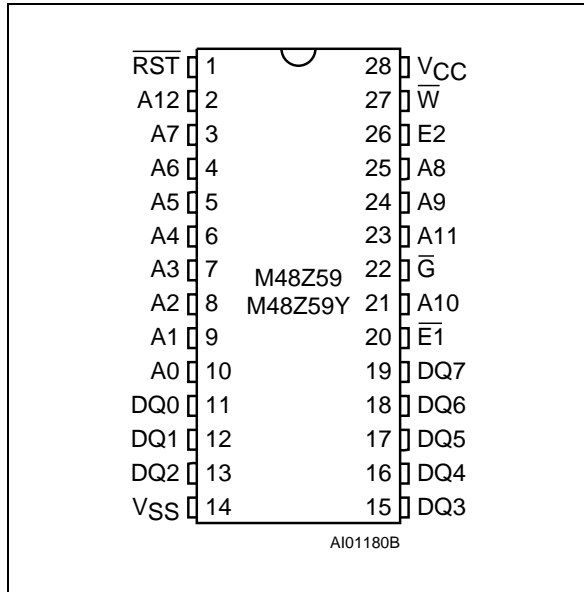
A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{RST}$	Power Fail Reset Output (Open Drain)
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground

**Figure 1. Logic Diagram**

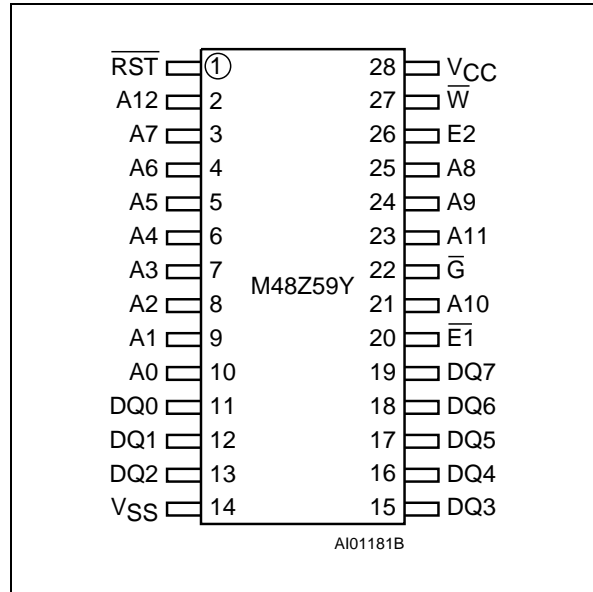


# M48Z59, M48Z59Y

**Figure 2A. DIP Pin Connections**



**Figure 2B. SOIC Pin Connections**



**Table 2. Absolute Maximum Ratings (1)**

Symbol	Parameter	Value	Unit
$T_A$	Ambient Operating Temperature	0 to 70	°C
$T_{STG}$	Storage Temperature ( $V_{CC}$ Off)	-40 to 85	°C
$T_{SLD}^{(2)}$	Lead Solder Temperature for 10 seconds	260	°C
$V_{IO}$	Input or Output Voltages	-0.3 to 7	V
$V_{CC}$	Supply Voltage	-0.3 to 7	V
$I_O$	Output Current	20	mA
$P_D$	Power Dissipation	1	W

**Notes:** 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.  
 2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

**CAUTION:** Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

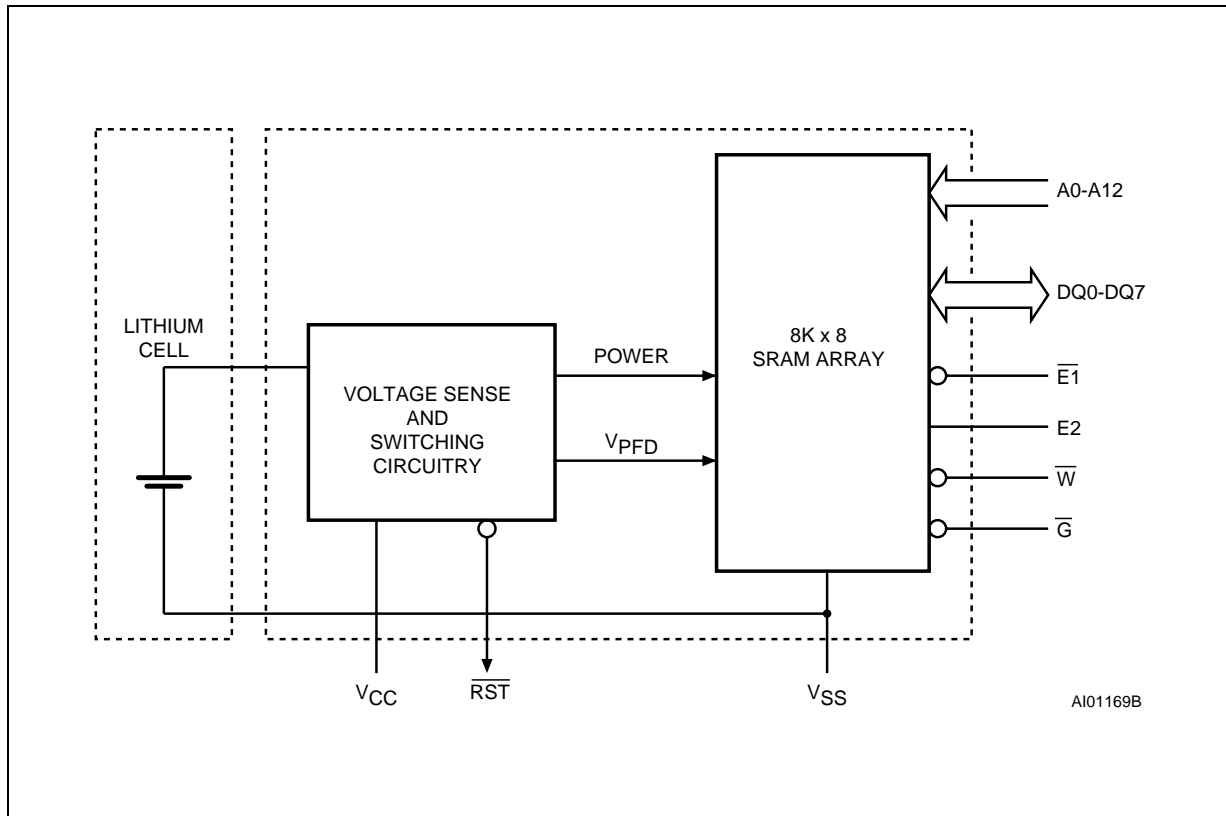
**CAUTION:** Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

**Table 3. Operating Modes (1)**

Mode	$V_{CC}$	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	$V_{IH}$	X	X	X	High Z	Standby
Deselect		X	$V_{IL}$	X	X	High Z	Standby
Write		$V_{IL}$	$V_{IH}$	X	$V_{IL}$	$D_{IN}$	Active
Read		$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$	Active
Read		$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IH}$	High Z	Active
Deselect	$V_{SO}$ to $V_{PFD}$ (min) (2)	X	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	X	High Z	Battery Back-up Mode

**Notes:** 1. X =  $V_{IH}$  or  $V_{IL}$ ;  $V_{SO}$  = Battery Back-up Switchover Voltage.  
 2. See Table 7 for details.

Figure 3. Block Diagram



**DESCRIPTION (cont'd)**

The M48Z59/59Y is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z59/59Y silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

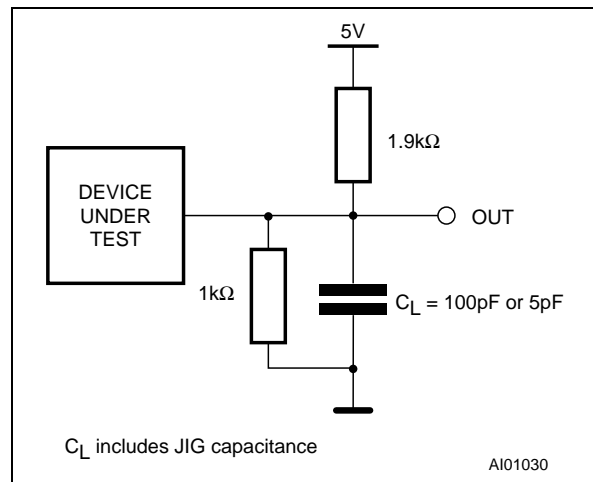
The SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form.

**Table 4. AC Measurement Conditions**

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

**Figure 4. AC Testing Load Circuit**



## M48Z59, M48Z59Y

**Table 5. Capacitance** <sup>(1, 2)</sup>  
(T<sub>A</sub> = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V		10	pF
C <sub>IO</sub> <sup>(3)</sup>	Input / Output Capacitance	V <sub>OUT</sub> = 0V		10	pF

**Notes:** 1. Effective capacitance measured with power supply at 5V.  
2. Sampled only, not 100% tested.  
3. Outputs deselected.

**Table 6. DC Characteristics**  
(T<sub>A</sub> = 0 to 70°C; V<sub>CC</sub> = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>LI</sub> <sup>(1)</sup>	Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		±1	μA
I <sub>LO</sub> <sup>(1)</sup>	Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>		±5	μA
I <sub>CC</sub>	Supply Current	Outputs open		50	mA
I <sub>CC1</sub>	Supply Current (Standby) TTL	$\overline{E1} = V_{IH}, E2 = V_{IL}$		3	mA
I <sub>CC2</sub>	Supply Current (Standby) CMOS	$\overline{E1} = V_{CC} - 0.2V,$ $E2 = V_{SS} + 0.2V$		3	mA
V <sub>IL</sub>	Input Low Voltage		-0.3	0.8	V
V <sub>IH</sub>	Input High Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		0.4	V
	Output Low Voltage ( $\overline{RST}$ ) <sup>(2)</sup>	I <sub>OL</sub> = 10mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.4		V

**Notes:** 1. Outputs Deselected.  
2. The  $\overline{RST}$  pin is Open Drain.

**Table 7. Power Down/Up Trip Points DC Characteristics** <sup>(1)</sup>  
(T<sub>A</sub> = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>PFD</sub>	Power-fail Deselect Voltage (M48Z59/59Y)	4.5	4.6	4.75	V
V <sub>PFD</sub>	Power-fail Deselect Voltage (M48Z59/59YY)	4.2	4.35	4.5	V
V <sub>SO</sub>	Battery Back-up Switchover Voltage		3.0		V
t <sub>DR</sub> <sup>(2)</sup>	Expected Data Retention Time	10			YEARS

**Notes:** 1. All voltages referenced to V<sub>SS</sub>.  
2. At 25 °C.

### DESCRIPTION (cont'd)

For the 28 lead SOIC, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

A power-on reset output provides a reset pulse to the microprocessor. The reset pulls low (open drain) an power-down and remains low on power-up for 40ms to 200ms after V<sub>CC</sub> passes V<sub>PFD</sub>. The M48Z59/59Y also has its own Power-fail Detect

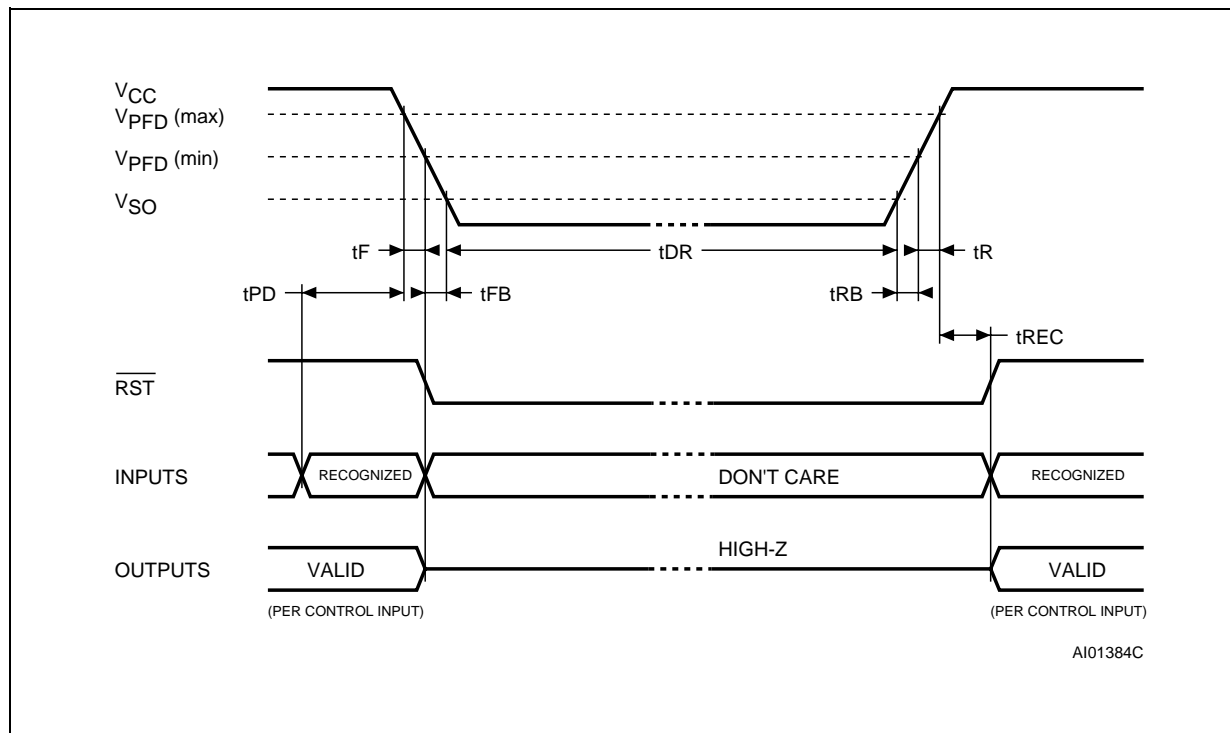
circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V<sub>CC</sub> is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V<sub>CC</sub>. As V<sub>CC</sub> falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

**Table 8. Power Down/Up Mode AC Characteristics**  
( $T_A = 0$  to  $70^\circ\text{C}$ )

Symbol	Parameter	Min	Max	Unit
$t_{PD}$	$\overline{E1}$ or $\overline{W}$ at $V_{IH}$ or E2 at $V_{IL}$ before Power Down	0		$\mu\text{s}$
$t_F^{(1)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ $V_{CC}$ Fall Time	300		$\mu\text{s}$
$t_{FB}^{(2)}$	$V_{PFD}(\text{min})$ to $V_{SO}$ $V_{CC}$ Fall Time	10		$\mu\text{s}$
$t_R$	$V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ $V_{CC}$ Rise Time	10		$\mu\text{s}$
$t_{RB}$	$V_{SO}$ to $V_{PFD}(\text{min})$ $V_{CC}$ Rise Time	1		$\mu\text{s}$
$t_{REC}$	$V_{PFD}(\text{max})$ to $\overline{RST}$ High	40	200	ms

**Notes:** 1.  $V_{PFD}(\text{max})$  to  $V_{PFD}(\text{min})$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until  $200 \mu\text{s}$  after  $V_{CC}$  passes  $V_{PFD}(\text{min})$ .  
2.  $V_{PFD}(\text{min})$  to  $V_{SO}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

**Figure 5. Power Down/Up Mode AC Waveforms**



### READ MODE

The M48Z59/59Y is in the Read Mode whenever  $\overline{W}$  (Write Enable) is high,  $\overline{E1}$  (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. Valid data will be available at the Data I/O pins within Address Access time ( $t_{AVQV}$ ) after the last address input signal is stable, providing that the  $\overline{E1}$ , E2, and  $\overline{G}$  access times are also satisfied. If the  $\overline{E1}$ , E2 and  $\overline{G}$  access times are not met, valid data will be available after

the latter of the Chip Enable Access times ( $t_{E1LQV}$  or  $t_{E2HQV}$ ) or Output Enable Access time ( $t_{GLQV}$ ).

The state of the eight three-state Data I/O signals is controlled by  $\overline{E1}$ , E2 and  $\overline{G}$ . If the outputs are activated before  $t_{AVQV}$ , the data lines will be driven to an indeterminate state until  $t_{AVQV}$ . If the Address Inputs are changed while  $\overline{E1}$ , E2 and  $\overline{G}$  remain active, output data will remain valid for Output Data Hold time ( $t_{AXQX}$ ) but will go indeterminate until the next Address Access.

## M48Z59, M48Z59Y

**Table 9. Read Mode AC Characteristics**

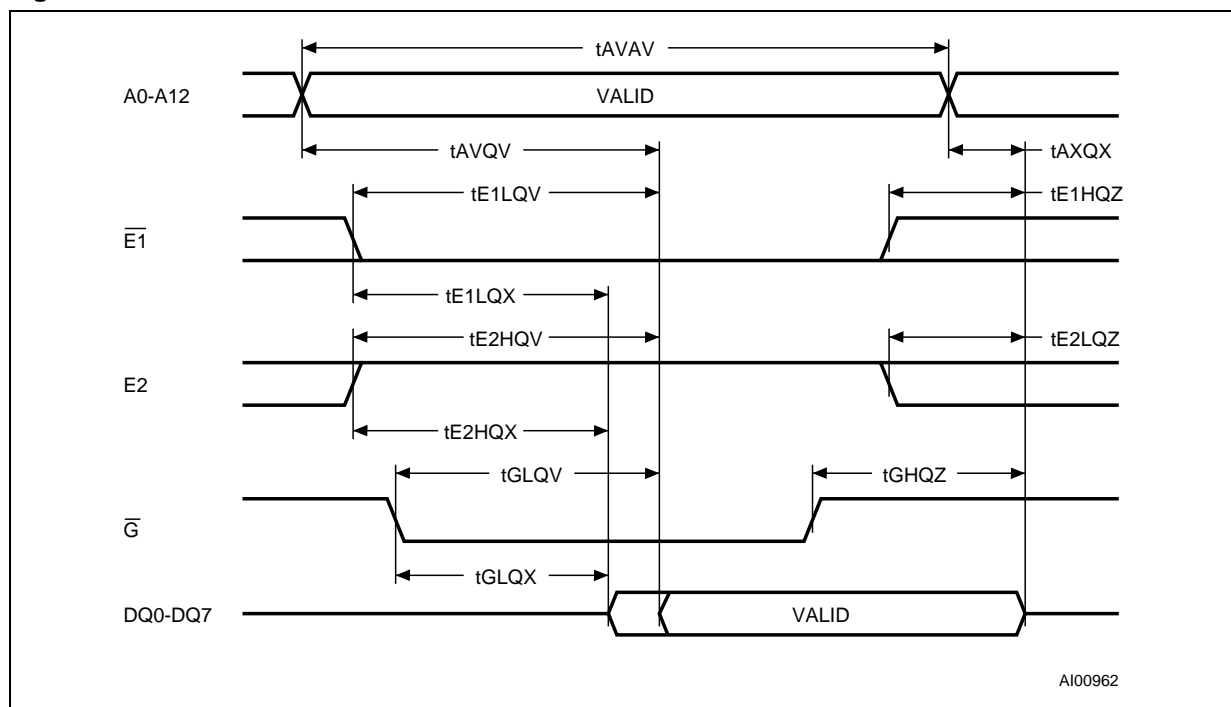
( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 4.75\text{V}$  to  $5.5\text{V}$  or  $4.5\text{V}$  to  $5.5\text{V}$ )

Symbol	Parameter	M48Z59 / M48Z59Y		Unit
		-70		
		Min	Max	
$t_{AVAV}$	Read Cycle Time	70		ns
$t_{AVQV}^{(1)}$	Address Valid to Output Valid		70	ns
$t_{E1LQV}^{(1)}$	Chip Enable 1 Low to Output Valid		70	ns
$t_{E2HQV}^{(1)}$	Chip Enable 2 High to Output Valid		70	ns
$t_{GLQV}^{(1)}$	Output Enable Low to Output Valid		35	ns
$t_{E1LQX}^{(2)}$	Chip Enable 1 Low to Output Transition	5		ns
$t_{E2HQX}^{(2)}$	Chip Enable 2 High to Output Transition	5		ns
$t_{GLQX}^{(2)}$	Output Enable Low to Output Transition	5		ns
$t_{E1HQZ}^{(2)}$	Chip Enable 1 High to Output Hi-Z		25	ns
$t_{E2LQZ}^{(2)}$	Chip Enable 2 Low to Output Hi-Z		25	ns
$t_{GHQZ}^{(2)}$	Output Enable High to Output Hi-Z		25	ns
$t_{AXQX}^{(1)}$	Address Transition to Output Transition	10		ns

Notes: 1.  $C_L = 100\text{pF}$  (see Figure 4).

2.  $C_L = 5\text{pF}$  (see Figure 4).

**Figure 6. Read Mode AC Waveforms**



Note: Write Enable ( $\overline{W}$ ) = High.

**Table 10. Write Mode AC Characteristics**  
 ( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 4.75\text{V}$  to  $5.5\text{V}$  or  $4.5\text{V}$  to  $5.5\text{V}$ )

Symbol	Parameter	M48Z59 / M48Z59Y		Unit
		-70		
		Min	Max	
$t_{AVAV}$	Write Cycle Time	70		ns
$t_{AVWL}$	Address Valid to Write Enable Low	0		ns
$t_{AVE1L}$	Address Valid to Chip Enable 1 Low	0		ns
$t_{AVE2H}$	Address Valid to Chip Enable 2 High	0		ns
$t_{WLWH}$	Write Enable Pulse Width	50		ns
$t_{E1LE1H}$	Chip Enable 1 Low to Chip Enable 1 High	55		ns
$t_{E2HE2L}$	Chip Enable 2 High to Chip Enable 2 Low	55		ns
$t_{WHAX}$	Write Enable High to Address Transition	0		ns
$t_{E1HAX}$	Chip Enable 1 High to Address Transition	0		ns
$t_{E2LAX}$	Chip Enable 2 Low to Address Transition	0		ns
$t_{DVWH}$	Input Valid to Write Enable High	30		ns
$t_{DVE1H}$	Input Valid to Chip Enable 1 High	30		ns
$t_{DVE2L}$	Input Valid to Chip Enable 2 Low	30		ns
$t_{WHDX}$	Write Enable High to Input Transition	5		ns
$t_{E1HDX}$	Chip Enable 1 High to Input Transition	5		ns
$t_{E2LDX}$	Chip Enable 2 Low to Input Transition	5		ns
$t_{WLQZ}^{(1, 2)}$	Write Enable Low to Output Hi-Z		25	ns
$t_{AVWH}$	Address Valid to Write Enable High	60		ns
$t_{AVE1H}$	Address Valid to Chip Enable 1 High	60		ns
$t_{AVE2L}$	Address Valid to Chip Enable 2 Low	60		ns
$t_{WHQX}^{(1, 2)}$	Write Enable High to Output Transition	5		ns

Notes: 1.  $C_L = 5\text{pF}$  (see Figure 4).

2. If  $\overline{E1}$  goes low or  $E2$  high simultaneously with  $\overline{W}$  going low, the outputs remain in the high impedance state.

Figure 7. Write Enable Controlled, Write AC Waveforms

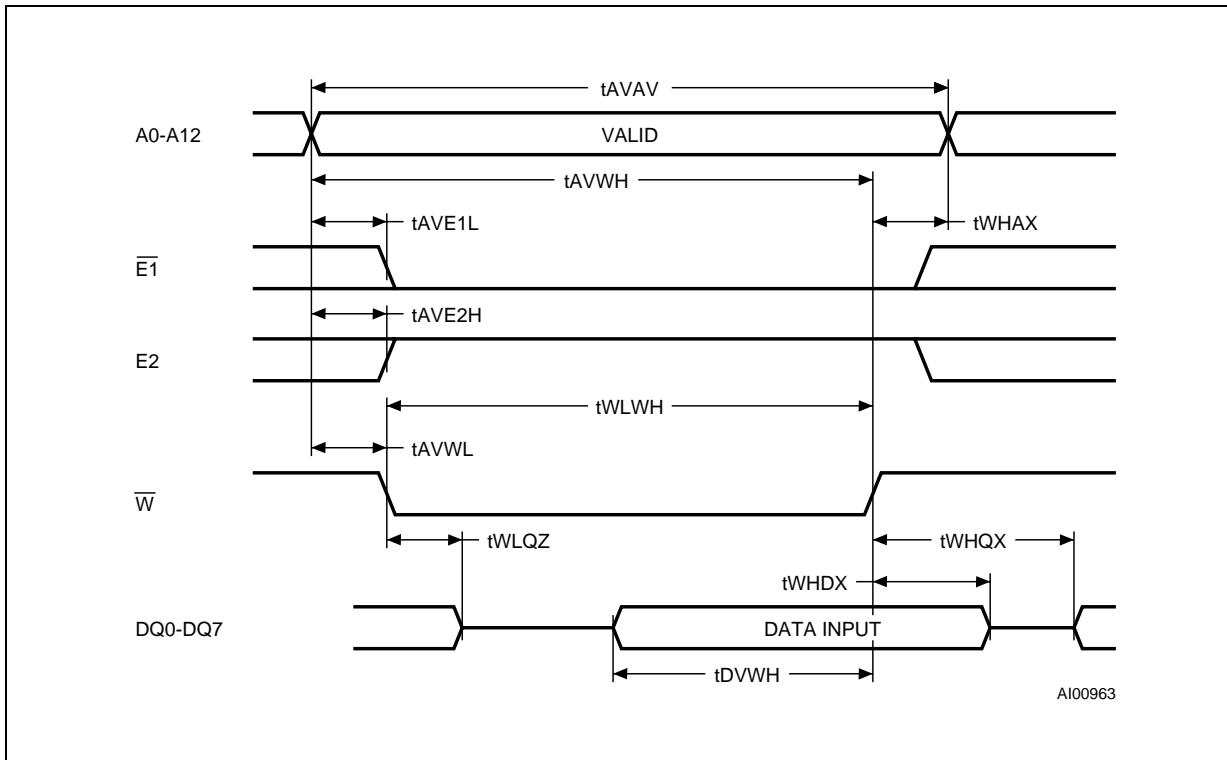
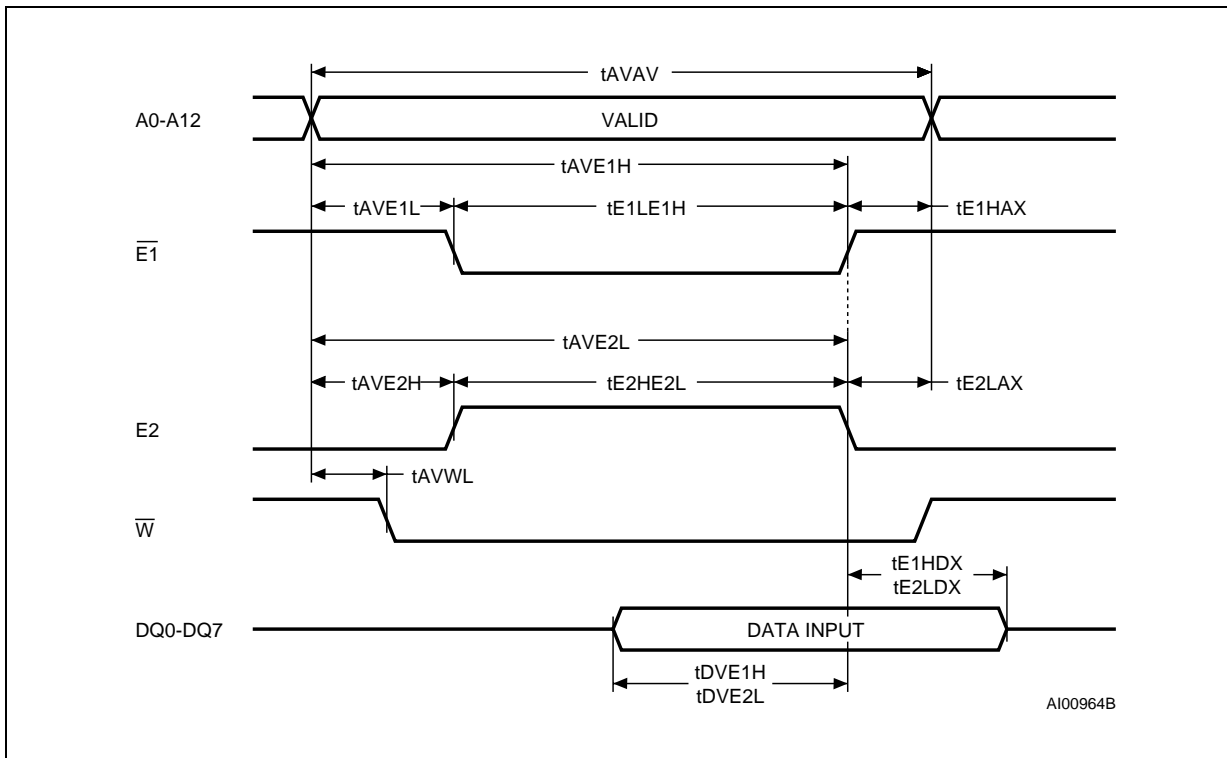


Figure 8. Chip Enable Controlled, Write AC Waveforms





## WRITE MODE

The M48Z59/59Y is in the Write Mode whenever  $\overline{W}$  and  $\overline{E1}$  are low and E2 is high. The start of a write is referenced from the latter occurring falling edge of  $\overline{W}$  or  $\overline{E1}$ , or the rising edge of E2. A write is terminated by the earlier rising edge of  $\overline{W}$  or  $\overline{E1}$ , or the falling edge of E2. The addresses must be held valid throughout the cycle.  $\overline{E1}$  or  $\overline{W}$  must return high or E2 low for a minimum of  $t_{E1HAX}$  or  $t_{E2LAX}$  from Chip Enable or  $t_{WHAX}$  from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid  $t_{DVWH}$  prior to the end of write and remain valid for  $t_{WHDX}$  afterward.  $\overline{G}$  should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on  $\overline{E1}$  and  $\overline{G}$  and a high on E2, a low on  $\overline{W}$  will disable the outputs  $t_{WLQZ}$  after  $\overline{W}$  falls.

## DATA RETENTION MODE

With valid  $V_{CC}$  applied, the M48Z59/59Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when  $V_{CC}$  falls within the  $V_{PFD(max)}$ ,  $V_{PFD(min)}$  window. All outputs become high impedance, and all inputs are treated as "don't care."

**Note:** A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below  $V_{PFD(min)}$ , the user can be assured the memory will be in a write protected state, provided the  $V_{CC}$  fall time is not less than  $t_F$ . The M48Z59/59Y may respond to transient noise spikes on  $V_{CC}$  that reach into the deselect window during the time the device is sampling  $V_{CC}$ . Therefore, decoupling of the power supply lines is recommended.

When  $V_{CC}$  drops below  $V_{SO}$ , the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z59/59Y for an accumulated period of at least 10 years when  $V_{CC}$  is less than  $V_{SO}$ . As system power returns and  $V_{CC}$  rises above  $V_{SO}$ , the battery is disconnected, and the power supply is switched to external  $V_{CC}$ . Write protection continues for  $t_{REC}$  until  $V_{CC}$  reaches  $V_{PFD(min)}$ .  $\overline{E1}$  should be kept high or E2 low as  $V_{CC}$  rises past  $V_{PFD(min)}$  to prevent inadvertent write cycles prior to system stabilization. Normal RAM operation can resume  $t_{REC}$  after  $V_{CC}$  exceeds  $V_{PFD(max)}$ .

For more information on Battery Storage Life refer to the Application Note AN1012.

## POWER-ON RESET

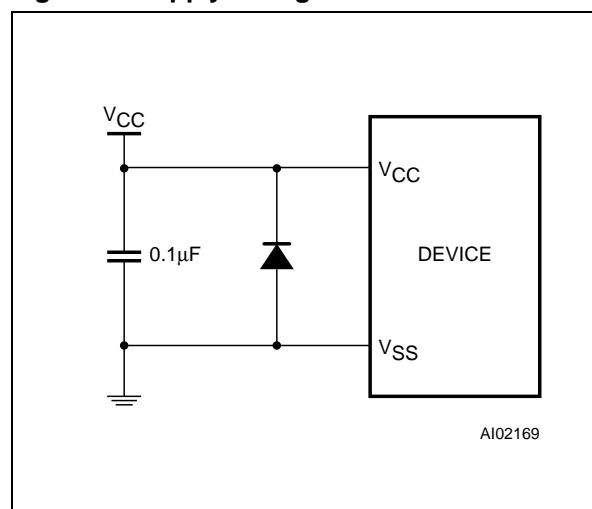
The M48Z59/59Y continuously monitors  $V_{CC}$ . When  $V_{CC}$  falls to the power fail detect trip point, the RST pulls low (open drain) and remains low on power-up for 40ms to 200ms after  $V_{CC}$  passes  $V_{PFD}$ . A 1k $\Omega$  resistor is recommended in order to control the rise-time. The reset pulse remains active with  $V_{CC}$  at  $V_{SS}$ .

## POWER SUPPLY DECOUPLING and UNDER-SHOOT PROTECTION

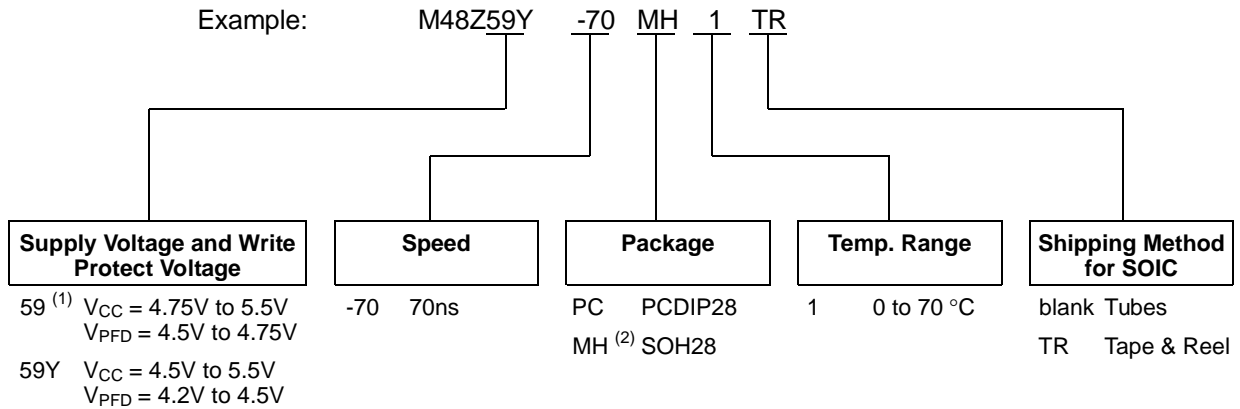
$I_{CC}$  transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the  $V_{CC}$  bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the  $V_{CC}$  bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 $\mu$ F (as shown in Figure 9) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on  $V_{CC}$  that drive it to values below  $V_{SS}$  by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from  $V_{CC}$  to  $V_{SS}$  (cathode connected to  $V_{CC}$ , anode to  $V_{SS}$ ). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 9. Supply Voltage Protection



**ORDERING INFORMATION SCHEME**



**Notes:** 1. The M48Z59 part is offered with the PCDIP28 (i.e. CAPHAT) package only.  
 2. The SOIC package (SOH28) requires the battery package (SNAPHAT) which is ordered separately under the part number "M4Z28-BR00SH1" in plastic tube or "M4Z28-BR00SH1TR" in Tape & Reel form.

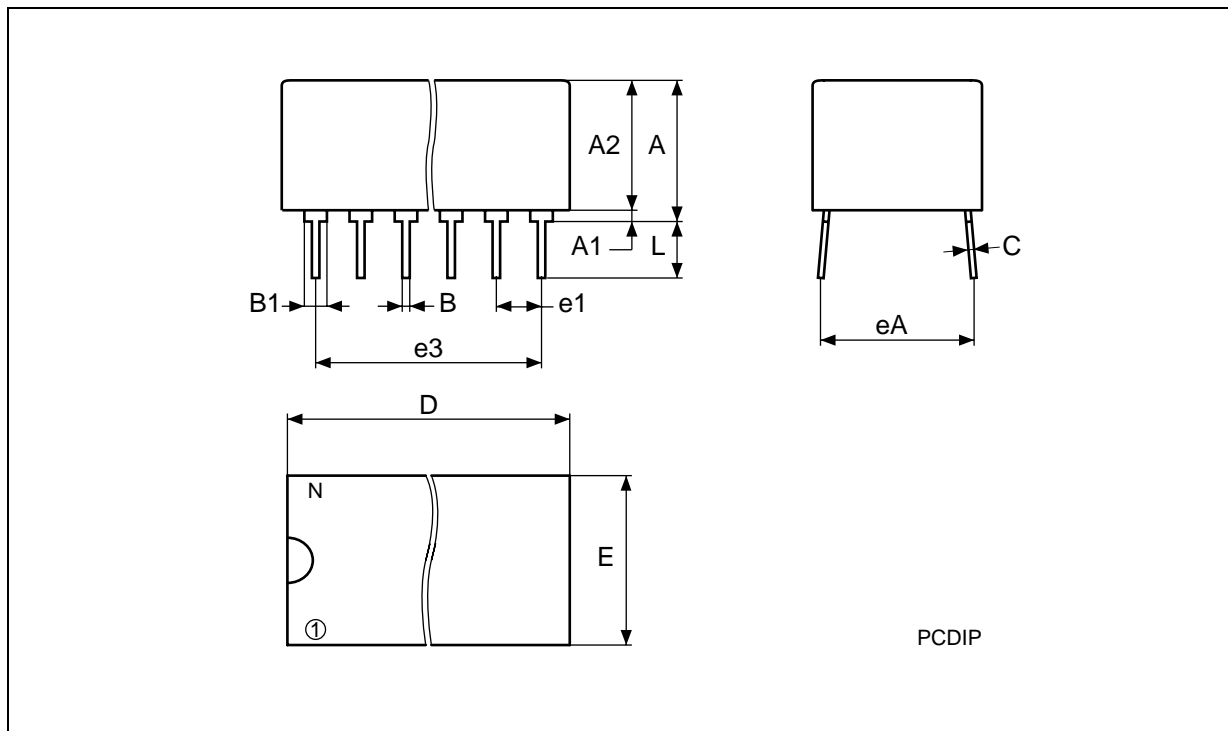
**Caution:** Do not place the SNAPHAT battery package "M4Z28-BR00SH1" in conductive foam since this will drain the lithium button-cell battery.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

## PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N		28			28	

PCDIP28

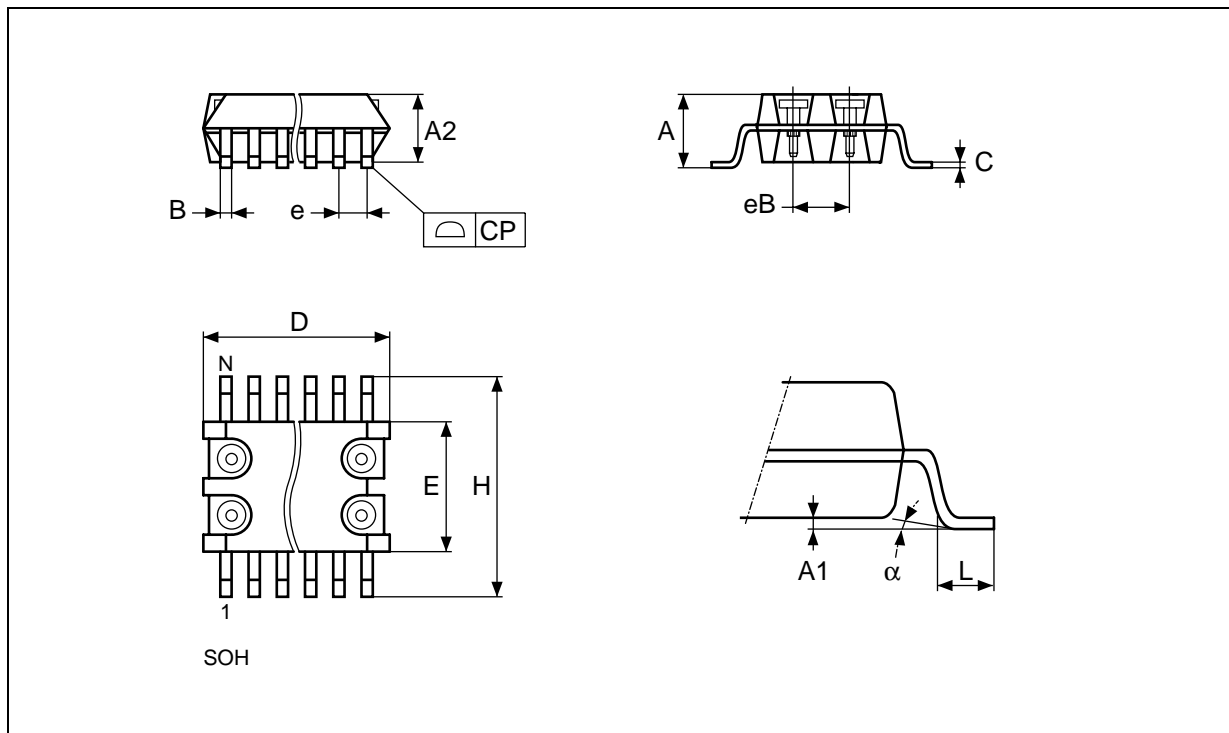


Drawing is not to scale.

**SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT**

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
$\alpha$		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28

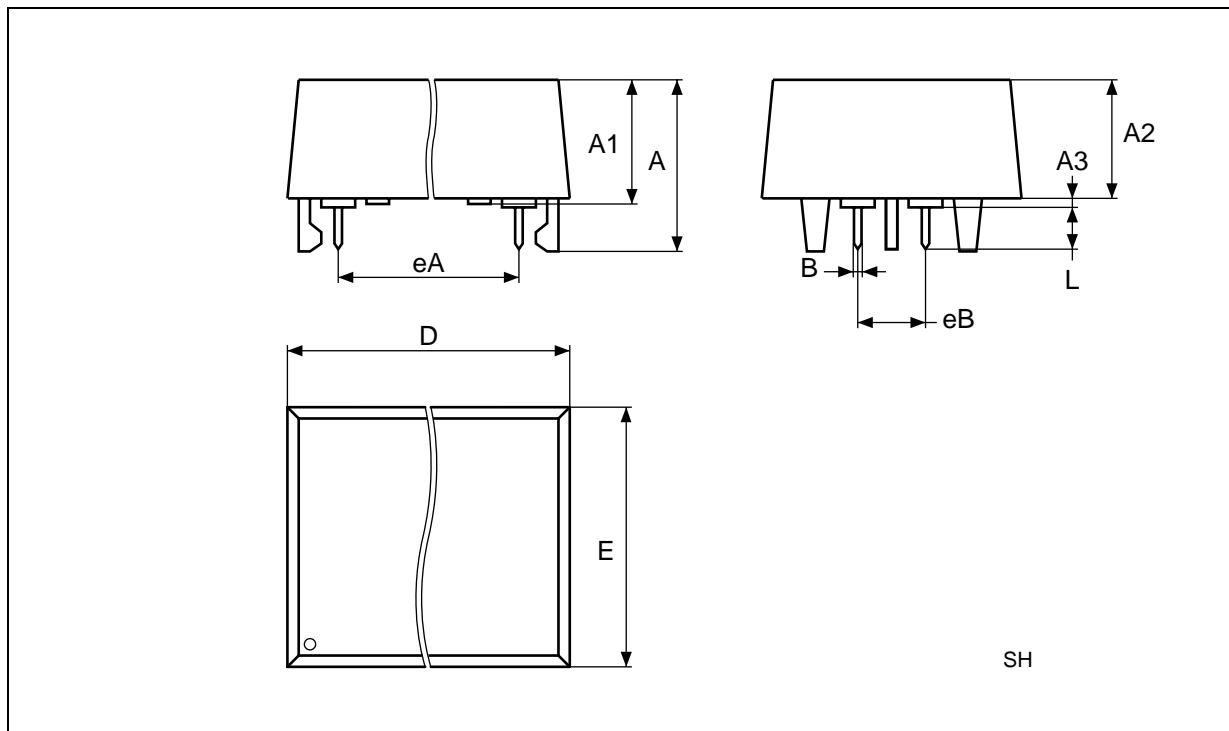


Drawing is not to scale.

### SH - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

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Drawing is not to scale.

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