

GD54/74HC113, GD54/74HCT113

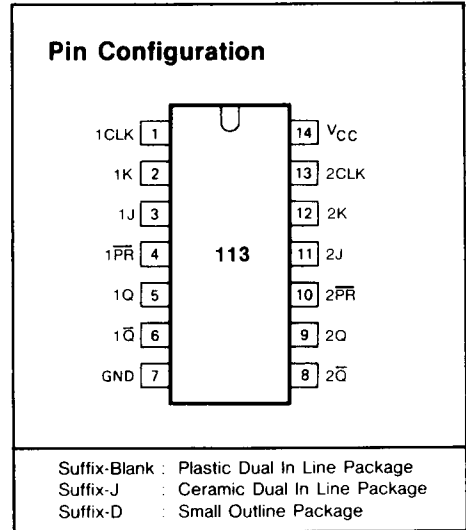
DUAL J-K FLIP-FLOPS WITH PRESET

General Description

These devices are identical in pinout to the 54/74LS113. They consist of two J-K flip-flops with individual J, K, Clock, and Preset inputs. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Both Q and \bar{Q} outputs are available from each flip-flop. Preset is independent of the Clock and accomplished by a Low level on the input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $40\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs.



Logic Symbol

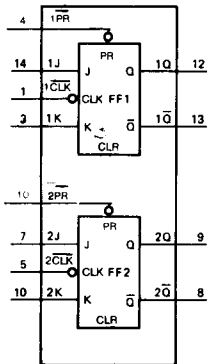


Fig. 1 Logic symbol

Function Table

INPUTS				OUTPUTS	
\overline{nPR}	nCLK	nJ	nK	nQ	\overline{nQ}
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q_0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q_0}$

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

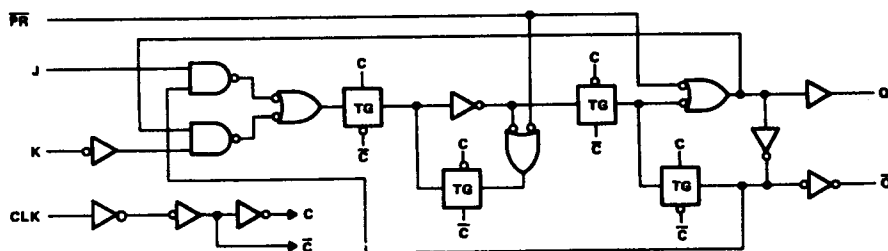


Fig. 2 Logic diagram (one flip flop)

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC113		GD54HC113		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage		2.0	1.5			1.5		1.5		V	
			4.5	3.15			3.15		3.15			
			6.0	4.2			4.2		4.2			
V _{IL}	LOW level input voltage		2.0			0.3		0.3		0.3	V	
			4.5			0.9		0.9		0.9		
			6.0			1.2		1.2		1.2		
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0	1.9	2.0		1.9		1.9	V	
				4.5	4.4	4.5		4.4		4.4		
				6.0	5.9	6.0		5.9		5.9		
	I _{OH} =-4mA I _{OH} =-5.2mA	4.5	3.98	4.3		3.84		3.7				
		6.0	5.48	5.2		5.34		5.2				
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0			0.1		0.1		V	
				4.5			0.1		0.1			0.1
				6.0			0.1		0.1			0.1
	I _{OL} =4mA I _{OL} =5.2mA	4.5		0.17	0.26		0.33		0.4			
		6.0		0.15	0.26		0.33		0.4			
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA	

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT113		GD54HCT113		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V	
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V	
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V
				4.5	3.98	4.3		3.84		3.7		
				4.5								
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1		0.1		0.1	V
				4.5		0.17	0.26		0.33		0.4	
				4.5								
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA	

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50 pF$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD54HC113		GD54HC113		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	P̄R	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t _{su}	Setup time	Data to CLK	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t _{rec}	Recovery time	P̄R to CLK	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t _h	Hold time	CLK to Data	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50 pF$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC113		GD54HC113		UNIT
				MIN.	TPY.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Muximum Clock Pulse Frequency	2.0	6	20		5		4		MHz	
		4.5	30	65		25		20			
		6.0	35	75		30		25			
t _{PLH} / t _{PHL}	Propagation Delay Time nCLK to nQ	2.0		46	160		200		240	ns	
		4.5		15	30		40		45		
		6.0		14	28		35		50		
t _{PLH} / t _{PHL}	Propagation Delay Time nCLK to nQ̄	2.0		50	160		200		240	ns	
		4.5		17	30		40		50		
		6.0		16	28		35		45		
t _{PLH} / t _{PHL}	Propagation Delay Time nP̄R to nQ, nQ̄	2.0		45	155		190		230	ns	
		4.5		15	28		38		45		
		6.0		14	26		34		40		
t _{TLH} / t _{THL}	Output Transition Time	2.0		25	70		85		100	ns	
		4.5		8	15		18		22		
		6.0		7	13		16		19		

GD54/74HC113, GD54/74HCT113

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HCT113		GD54HCT113		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	$\overline{\text{PR}}$	4.5	18	10		20		25		ns
		CLK	4.5	16	10		20		25		ns
t _{su}	Setup time	Data to CLK	4.5	15	10		18		20		ns
t _{rec}	Recovery time	$\overline{\text{PR}}$ to CLK	4.5	5	0		5		5		ns
t _h	Hold time	CLK to Data	4.5	3	0		3		3		ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HCT113		GD54HCT113		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency		4.5	27	54		22		18		MHz
t _{PLH} / t _{PHL}	Propagation Delay Time nCLK to nQ		4.5		17	30		40		50	ns
t _{PLH} / t _{PHL}	Propagation Delay Time nCLK to n $\overline{\text{Q}}$		4.5		17	30		40		50	ns
t _{PLH} / t _{PHL}	Propagation Delay Time n $\overline{\text{PR}}$ to nQ, n $\overline{\text{Q}}$		4.5		15	28		38		45	ns
t _{TLH} / t _{THL}	Output Transition Time		4.5		8	15		18		22	ns

AC Waveforms

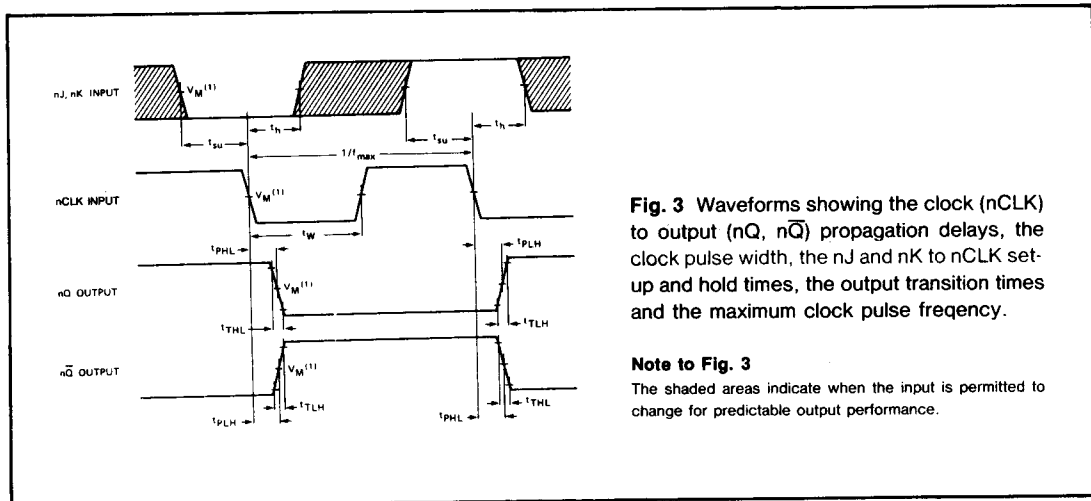


Fig. 3 Waveforms showing the clock (nCLK) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ and nK to nCLK set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 3

The shaded areas indicate when the input is permitted to change for predictable output performance.

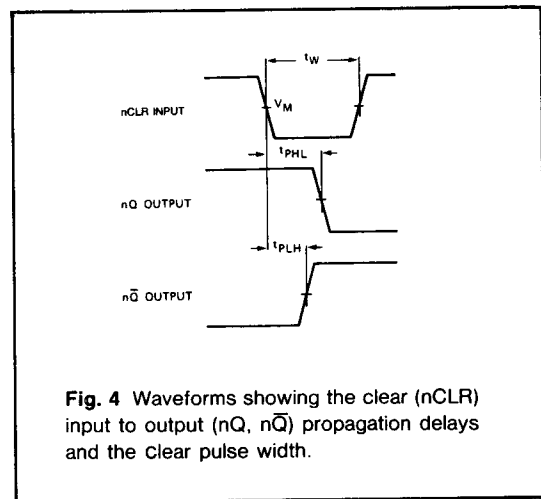


Fig. 4 Waveforms showing the clear (nCLR) input to output (nQ, nQ̄) propagation delays and the clear pulse width.

Note to AC waveforms

(1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
 HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.