Double Density CD-ROM/-R/-RW Encoder/Decoder

FEATURES

- — Fully-compatible with the *1.3 GB Double Density CD-ROM/-R/-RW* specification
- — Up to 16x write speeds and 50x read speeds
- — Integrates CD-ROM decoder, CD-ROM encoder, CIRC encoder, EFM modulator, ATIP decoder, buffer manager, and interface to SCSI protocol ICs
- — Firmware backward compatible with previous generations of CD-RW encoder/decoder
- — High-performance ATAPI interface supports synchronous DMA/33 protocol
- — Automatic power-down interfaces when idle
- — Built-in clock synthesizer
- — Available in 128-pin LQFP package

■ CD-R/CD-RW encoder

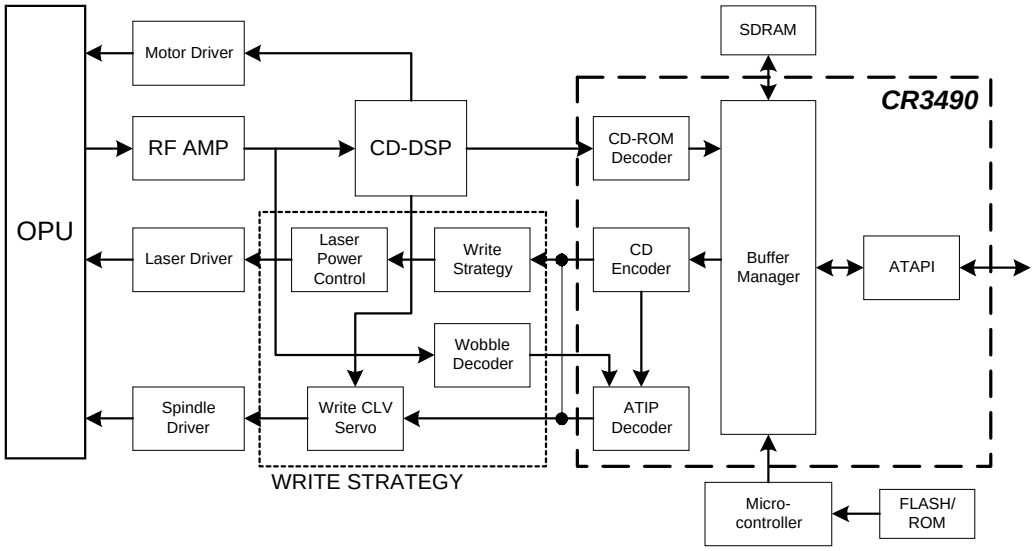
- — Supports all write methods:
  - Disc at once
  - Track at once
  - Packet recording
  - Multi-session at once
- — Highly automated CD-R/CD-RW formatter eliminates the sector-by-sector intervention by the microcontroller
- — Supports CD-RW logical erase
- — Supports up to 16x encoding
- — Supports subcode R-W encode
- — Integrated CIRC encoder
- — Integrated EFM modulation circuitry
- — Integrated ATIP decoder with target ATIP search function
- — Provides timing for laser power on/off control

■ CD-ROM decoder

- — Supports Sony-Philips® CD-ROM, CD-I, and CD-Digital Audio (CD-DA™) formats
- — Supports various compact disc DSP (digital signal processor) controllers
- — Read speeds up to 50x
- — Supports programmable pseudo-sync-mark insertion for CD-ROM sector synchronization
- — Supports automatic target sector header search for CD-ROM

(cont. page 2)

System Block Diagram



FEATURES (cont.)

- **CD-ROM decoder *(cont.)***
  - — Supports CD-Text mode format
  - — Sector header validity check is done by hardware during data transfers
  - — Realtime CD-ROM layered ECC error correction with programmable number of sets of P-word and Q-word corrections per sector (up to 64 total)
  - — Supports realtime subcode R-W correction in CD-DA (digital audio) mode
  - — Automated CD-R packet disc read Method-1 and Method-2
- **DAC interface**
  - — Audio Data Buffering (ADB) supports electronic shock proof CD-DA audio play mode
  - — Supports buffer streaming during buffer-to-DAC data transfer
  - — Supports various DACs
- **ATAPI host interface**
  - — Fully compatible with the ATAPI specification SFF-8020
  - — True realtime hardware/software ATAPI compatibility
  - — Hardware implementation of ATAPI packet command ATAPI reset command
  - — Automated protocol control on block data transfer for ATAPI read/write commands
  - — Supports Synchronous DMA/33 data transfer protocol with data rates up to 33.3 Mbytes/sec.
  - — Direct interface to ATAPI bus with 4-mA or 12-mA drivers
  - — Supports any host speed with programmable and auto wait-state generation
  - — Supports fast ATA transfer speed; up to PIO mode 4, single-word DMA mode 2, and multi-word DMA mode 2
  - — Provision to daisy-chain two ATA or ATAPI embedded drives
- **Buffer manager**
  - — Direct addressing of up to 8 Mbytes of SDRAM
  - — Supports 8-bit SDRAMs
  - — Dual-port circular buffer control with access-priority resolver
  - — Supports variable buffer segmentation
  - — Supports streaming mode: hardware automation of concurrent host and disc transfer from different buffer segments, with a pacing mechanism to prevent buffer overrun and underrun conditions
  - — Programmable timing control for SDRAM
- **Microcontroller interface**
  - — Supports high-speed Intel®-type microcontrollers
  - — Supports non-multiplexed address and data buses
  - — Interrupt- or polled-microcontroller interface
  - — Supports Intel®-type byte ordering for word-wide microcontroller instructions
  - — Supports direct microcontroller access to buffer memory
- **SCSI interface**
  - — Supports data transfer to/from SCSI protocol devices, such as Symbios Logic® 53CF94/96-2 and 53CF92A Fast SCSI controllers
- **Absolute maximum ratings**
  - — Ambient temperature under bias: 0°C to 70°C
  - — Storage temperature: -65°C to 150°C
  - — Voltage on any pin with respect to ground: (GND –0.3 V) to (V_{CC} +0.3 V)
  - — Power dissipation: 0.40 W
  - — Power supply voltage: 3.0 to 3.6V
  - — Core power supply voltage: 2.25 to 2.75V

OVERVIEW

The CL-CR3490 is the first encoder/decoder chip to support the Double Density CD-ROM/-R/-RW standard, increasing the capacity of a 120mm CD to 1.3 Gbyte. This high-performance, highly integrated ATAPI interface device provides drive manufacturers the ability to design and deliver a high-performance CD-R/CD-RW (CD-Recordable/ CD-ReWritable) drive for this market. The CL-CR3490 supports up to 16x record/50x read speeds and integrates a CD-ROM decoder, CIRC encoder, EFM modulation, ATIP decoder, buffer manager, and ATAPI interface logic.

The CL-CR3490 allows customers to preserve all CD-R/CD-RW encode/decode firmware and electronics due to backward compatibility with previous Cirrus Logic devices. This feature becomes more important as write speed requirements increase and drive development cycles shorten.

All write methods are supported by the CL-CR3490: disc-at-once, track-at-once, packet recording, and multi-session-at-once. The device incorporates the most comprehensive error correction available in the industry, using realtime CD-ROM–layered ECC error correction with a programmable number of P- and Q-word corrections per sector (up to 64). The CL-CR3490 also supports realtime subcode R-W correction in CD-DA mode.

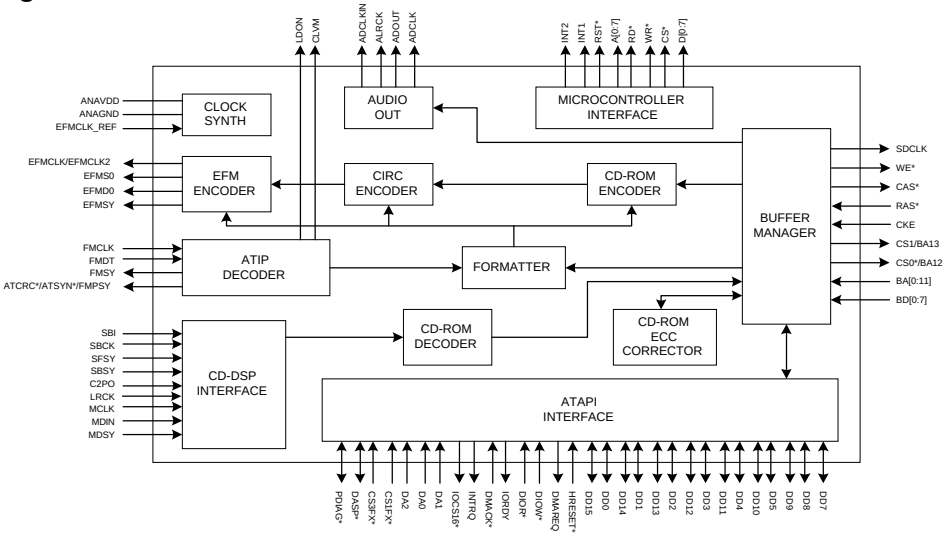
The DSP interface of the CL-CR3490 supports various CD-ROM DSPs from numerous manufacturers. The DSP interface includes three types of interface signals: main data channel, subcode channel, and serial DSP programming signals.

The integrated CD-R/-RW formatter is a built-in control processor that executes formatter instructions stored in the buffer memory, controls the CD-ROM encoder, and specifies how each block is generated/encoded through an entire recording operation. The built-in high-performance buffer manager controls the flow of data between the external DRAM data buffer and all other internal blocks.

In addition, the CL-CR3490 supports streaming mode, or the hardware automation of concurrent host and disc transfers from the same buffer segment. These features ease firmware programming and decrease microcontroller intervention.

The highly automated and optimized ATAPI interface is designed to comply with the ATAPI specification. The ATAPI Command and Control Block registers contained in the CL-CR3490 register set allow both the host and the local microcontroller access.

Chip Block Diagram



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