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Memory Products	

27HC641

64K-bit CMOS EPROM (8K × 8)

DESCRIPTION

Philips Components-Signetics 27HC641 CMOS EPROM is a high-speed electrically programmable Read Only Memory. It is organized as 8,192 words of 8 bits and operates from a single 5V ± 10% power supply. All outputs offer 3-State operation and are fully TTL compatible.

The 27HC641 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing simplifying the design of electronic equipment which is subject to high noise environments.

The 27HC641 is available in windowed Ceramic DIP, Plastic DIP and PLCC packages. This makes it easy to upgrade systems currently using bipolar PROMs and provides a lower power memory system solution.

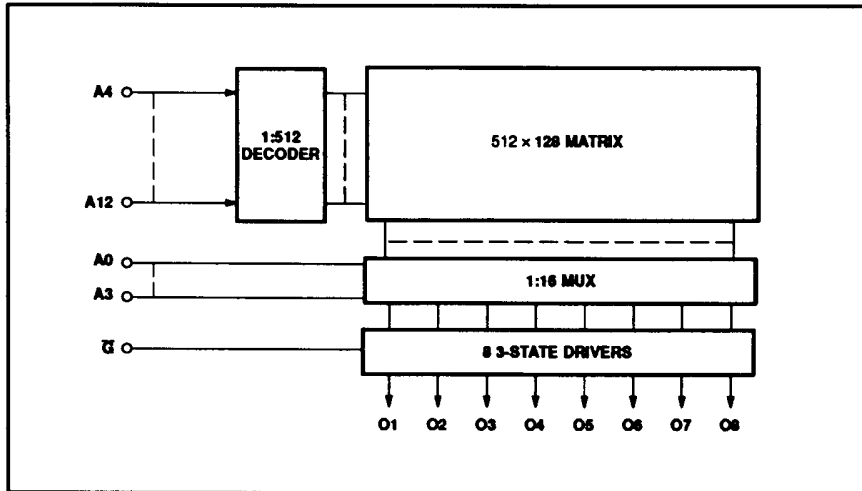
FEATURES

- High-performance speed
– 45ns maximum access time
- Operating I_{CC}: 110mA max
- 3-State outputs
- JEDEC standard 24-pin DIP and 28-pin PLCC packages
- Direct replacement for standard 64K TTL PROMs
- Fully TTL compatible

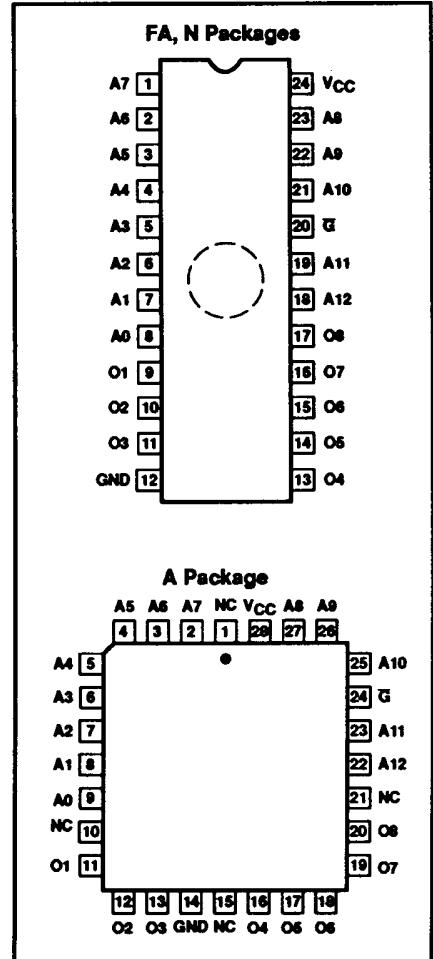
APPLICATIONS

- Prototyping and volume production
- High-performance mini- and microcomputers
- High-speed program store and look-up tables

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN DESCRIPTION

A0 - A12	Address inputs
O1 - O8	Data outputs
G	Output Enable
V _{CC}	Supply voltage
NC	No Connect
GND	Ground



64K-bit CMOS EPROM (8K × 8)**27HC641****ORDERING INFORMATION**

PACKAGE DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line w/ quartz window 600mil-wide	27HC641-45 FA 27HC641-55 FA
24-Pin Plastic Dual In-Line 600mil-wide	27HC641-45 N 27HC641-55 N
24-Pin Plastic Leaded Chip Carrier 450mil-wide	27HC641-45 A 27HC641-55 A

OPERATING TEMPERATURE RANGE

PARAMETER	RATING (°C)
Operating temperature range: T_{amb}	COMMERCIAL 0 to +70

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING	UNIT
V_I, V_O	Voltage inputs and outputs ²	-0.5 to ($V_{CC} + 1$)	V
T_{stg}	Storage temperature range	-65 to +125	°C
V_{PP}	Voltage on \bar{G} (During programming)	-0.5 to +13.5	V

NOTES:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0 for periods less than 20ns.

DC OPERATING CONDITIONS $0^{\circ}\text{C} \leq T_{amb} \leq +70^{\circ}\text{C}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply Voltage						
V_{CC}		GND = 0V	4.5	5.0	5.5	V
Input Voltage						
V_{IH}	High		2.0		$V_{CC} + 0.5$	V
V_{IL}	Low		-0.1		0.8	V

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DC ELECTRICAL CHARACTERISTICS

0°C ≤ T_{amb} ≤ +70°C, +4.5V ≤ V_{CC} ≤ +5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Input current						
I _{IH}	High	V _{IN} = V _{CC}			10	μA
I _{IL} ¹	Low	V _{IN} = 0.45V			10	μA
Output current						
I _{LO}	Leakage	V _{OUT} = 0 to V _{CC}			±10	μA
I _{OS}	Output short-circuit current ²	V _{OUT} = 0V, \bar{G} = V _{IL}	-15		-70	mA
Supply current						
I _{CC}	V _{CC} operating current	\bar{G} = V _H , O1-8 = 0mA, f = 20MHz			110	mA
Input voltage						
V _{IC}	Input clamp voltage	I _{IC} = -12mA			-1.2	V
Output voltage						
V _{OH}	High	I _{OH} = -4mA	2.4			V
V _{OL}	Low	I _{OL} = 16mA			0.45	V
Capacitance³						
C _{IN}	Input	f = 1.0MHz, T _{amb} = 25°C, V _{CC} = 5.0V, V _{IN} = 0V, V _{OUT} = 5.0V			6	pF
C _{OUT}	Output				12	pF

NOTES:

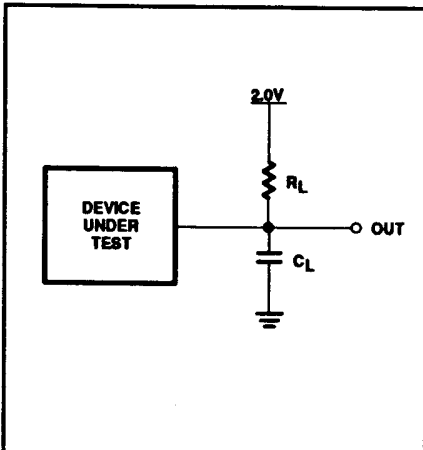
1. Input current for \bar{G} input only = -100μA.
2. Test one output at a time, duration should not exceed 1 second.
3. Capacitance limits are sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS

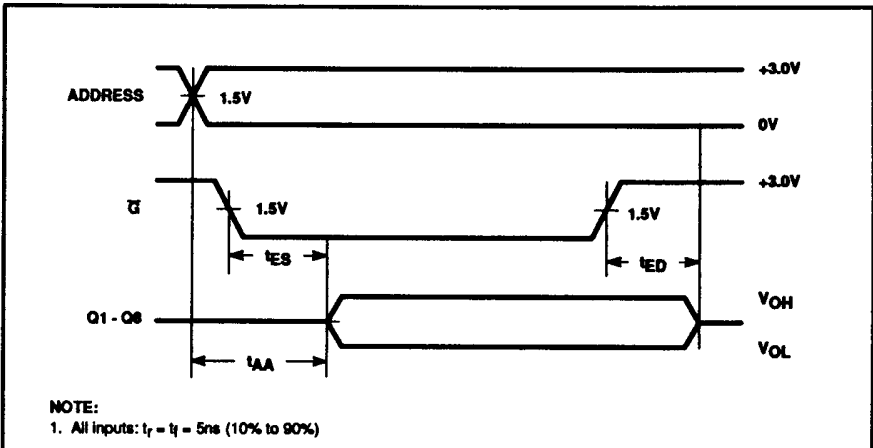
C_L = 30pF, R_L = 98Ω, 0°C ≤ T_{amb} ≤ +70°C, +4.5V ≤ V_{CC} ≤ +5.5V

SYMBOL	PARAMETER	TO	FROM	27HC641-45		27HC641-55		UNIT
				MIN	MAX	MIN	MAX	
t _{AA}	Address access time	Output	Address		45		55	ns
t _{ES}	Output Enable access time	Output	Output Enable		25		30	ns
t _{ED}	Output disable time	Output	Output Enable		25		30	ns

AC TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



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ERASURE CHARACTERISTICS

The 27HC641 is erased by exposure to ultraviolet light. The recommended erasure procedure is exposure to short-wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12,000μW/cm² power rating.

The 27HC641 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27HC641 can be exposed to without damage is 7258Wsec/cm² (1 week @ 12000μW/cm²). Exposure of this CMOS EPROM to high-intensity UV light for

longer periods may cause permanent damage. Some erasure may occur with exposure to light sources having wavelengths shorter than 4000Å such as sunlight or fluorescent light. For maximum system reliability, precautions should be taken by placing opaque labels over the quartz window when used in these environments.

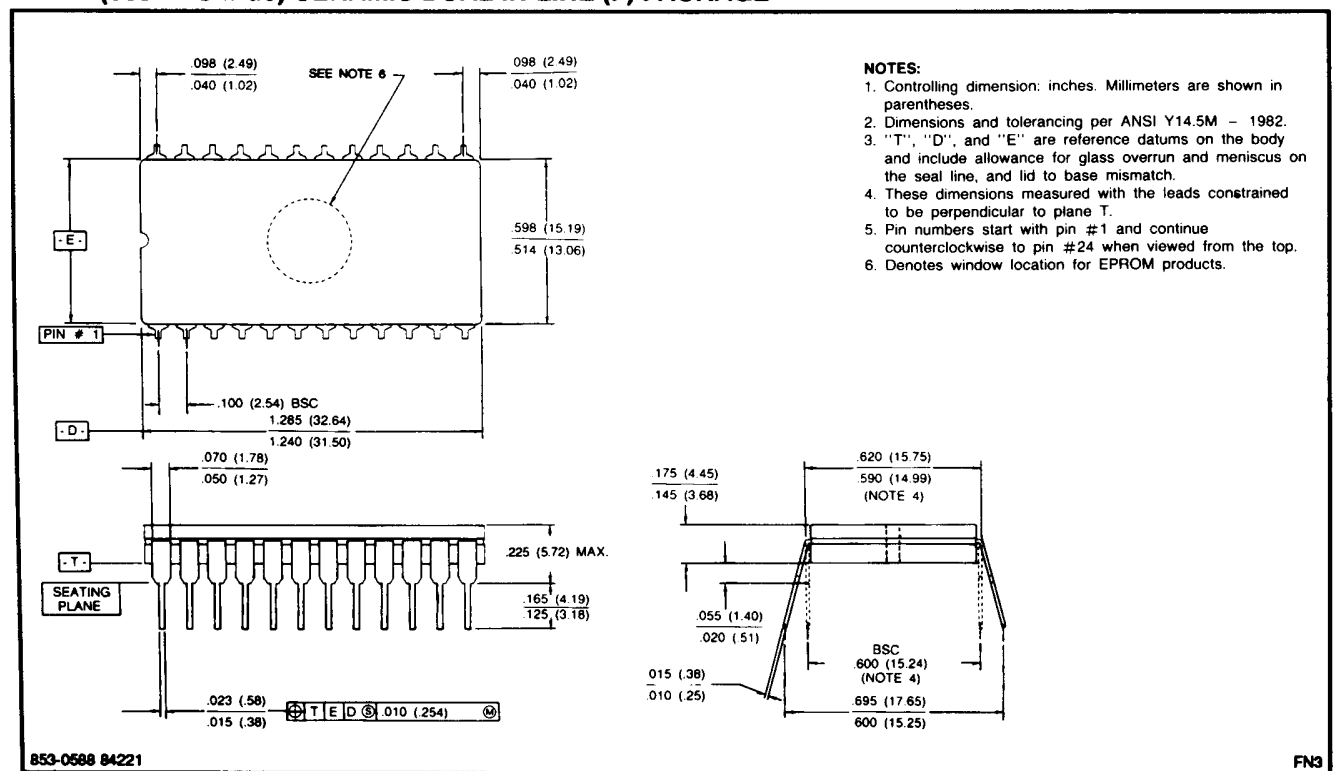
PROGRAMMING THE 27HC641

Initially, and after each erasure, all bits of the 27HC641 are in an **undefined state**. If bits in the 27HC641 are not programmed, they are in an **undefined state**, which is neither a logical "1" or a logical "0". The 27HC641 is

shipped in a fully GMSOD state, therefore, all bits must be programmed to a logical "1" or "0" state, to prevent false readings. Data is introduced by programming "1"s and "0"s into the desired bit locations. Both "1"s and "0"s must be present in the data word to define each bit. The only way to change a bit to the opposite state is by ultraviolet light erasure and programming it to the desired state.

The 27HC641 is in the programming mode when the Chip Select \bar{C} pin is at 12.5V. The data to be programmed is applied 8 bits in parallel to the data output pins, while selecting the desired address location via the address inputs. The levels required for the address and data inputs are TTL.

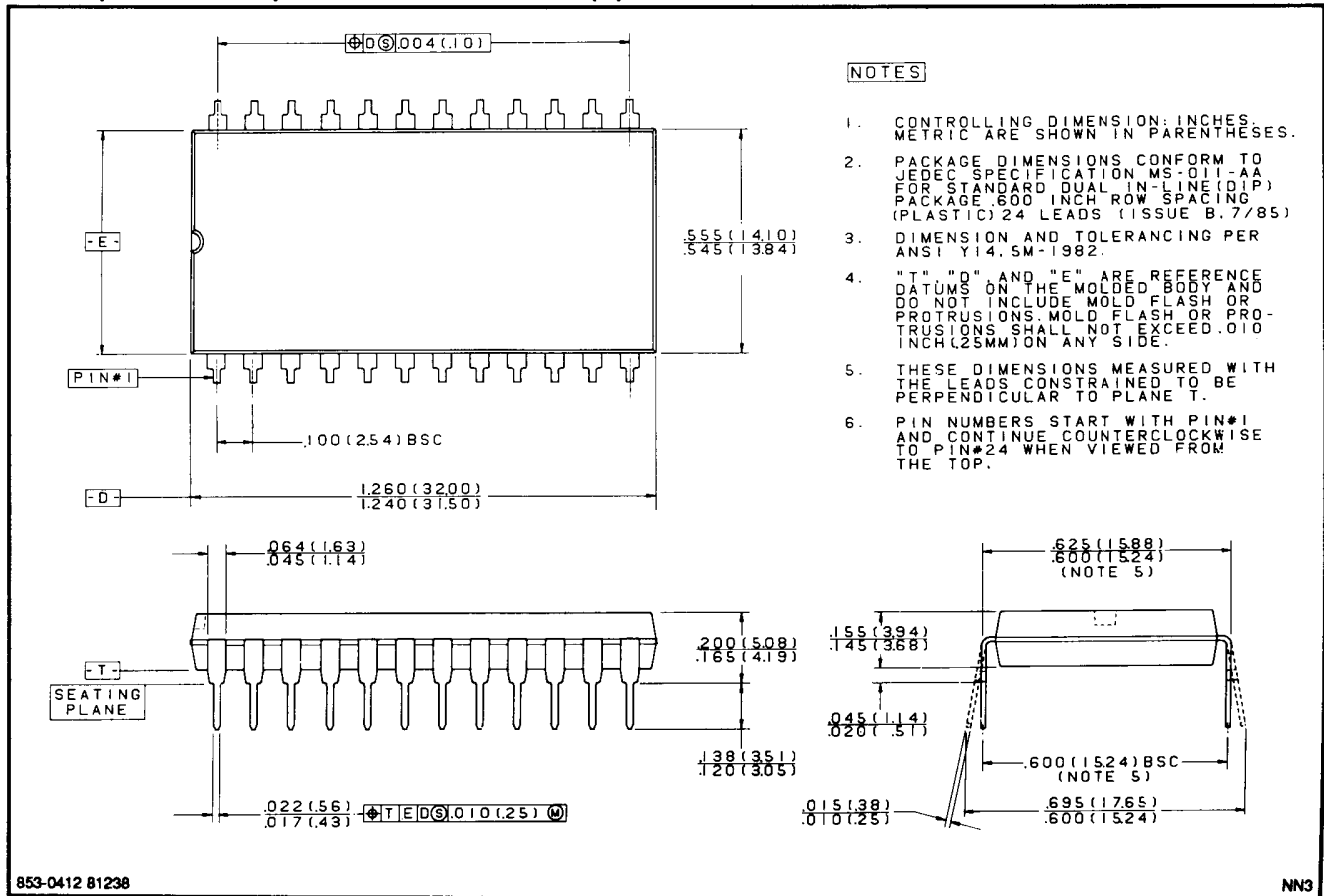
24-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE



64K-bit CMOS EPROM (8K × 8)

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24-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



853-0412 81238

NN3

64K-bit CMOS EPROM (8K × 8)

27HC641

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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