K0S Family

μPD7894xx

8-Bit Microcontrollers with LCD

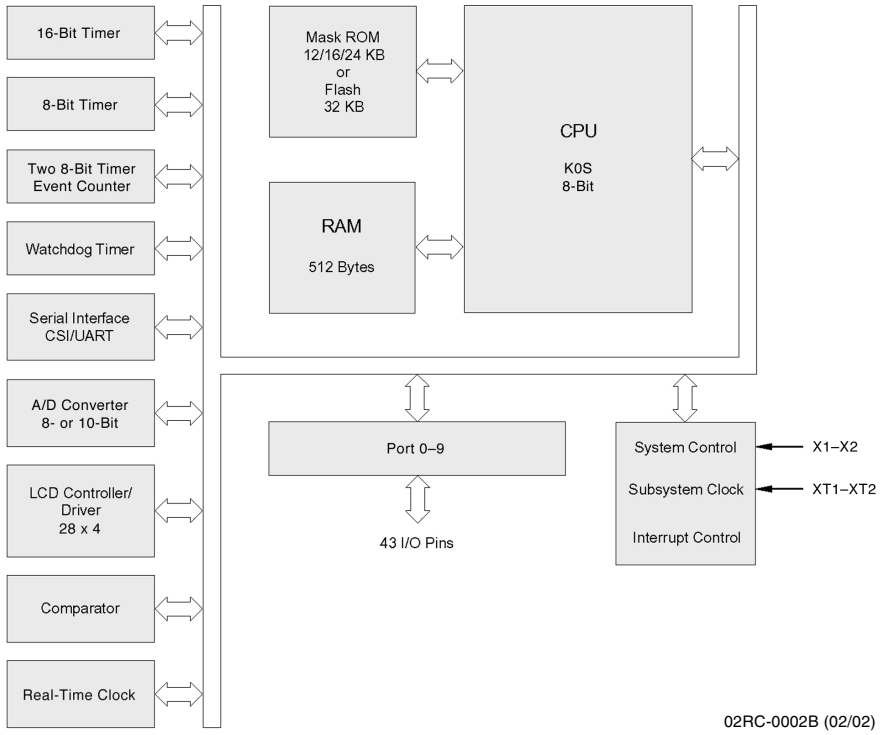
Description

The μPD7894xx single-chip microcontrollers contain an LCD controller capable of controlling and directly driving up to 112 LCD segments. With a variety of integrated peripherals, these devices have low EMI emissions and are fabricated with NEC's 0.35-micron process technology. The μPD7894xx devices also provide very low-power operating modes using two on-chip oscillator circuits. The low EMI emissions, low-power operation, and serial communications make these devices ideal for low-noise, battery-powered applications that require serial communication. A flash version is available, as is an extensive tool set consisting of a software simulator, C compiler, relocatable assembler, screen debugger, and in-circuit emulator.

Specifications

- Clock frequency: 1 to 5 MHz
- Performance: 400 ns min. instruction execution time
- Operating voltage: 1.8–5.5V
- EMI emissions: 10–15 dB lower than most microcontrollers
- Power consumption
  - Normal operation: 0.8 mW
  - Halt mode: 0.6 mW
  - Stop mode: 0.0001 mW
- Package: 80-pin QFP
  - 14 x 14 x 2.70 mm
  - 12 x 12 x 1.05 mm

Block Diagram



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Features

- 64 KB linear address space
- 12 KB–24 KB internal ROM
- 32 KB flash memory
- 512-byte RAM
- 28 segment x 4 common LCD controller
- Seven-channel 8-bit or 10-bit A/D converter with 14-µs conversion time
- One 16-bit timer/event counter
- Three 8-bit timer/event counters
- One real-time clock
- One watchdog/interval timer
- One serial channel
  - UART/synchronous channel
  - Baud rate generator
- 43 general-purpose I/O pins
- One comparator
- 0.35-micron CMOS process technology

Functional Description

CPU

The core of the K0S family is a powerful 8-bit CPU fabricated with 0.35 µm process technology that ensures an excellent power/performance ratio for the µPD7894xx. The CPU executes a set of 47 optimized instructions. Eight 8-bit general registers can be concatenated to four 16-bit registers to enable 16-bit operations. Bit manipulation operations are supported on the entire RAM address space.

Memory

The µPD7894xx devices offer a rich choice of on-chip memory combinations, including mask ROM and flash versions. The flash memory can be written even with the device mounted in the target system.

Ports

The devices have nine ports with a total of 43 I/O pins. Thirty-two CMOS I/O pins feature internal pull-up resistors that can be enabled via software when the port is used for input. Seven are CMOS input pins and four are N-channel open-drain pins.

LCD Controller/ Driver

The on-chip LCD controller/driver automatically generates up to 28 segment signal outputs and four common signal outputs. The output signals are based on automatic display data memory read. Five different display modes and four different frame frequencies can be selected via internal control registers.

A/D Converter

A seven-channel A/D converter with 10-bit (µPD78940x = 8-bit) resolution is provided on chip. An external analog value, within the reference voltage range, can be converted by successive approximation into a 10-bit (8-bit) digital value. The minimum conversion time is less than 15 µs at 5 MHz.

Functional Description

Serial Interface

All devices have a serial interface that can be operated in asynchronous serial interface (UART) mode or in three-wire clocked serial interface (CSI) mode via a dedicated baud rate generator. In addition, the baud rate can be defined by scaling the input clock. The UART also features full-duplex operation. In CSI mode, an 8-bit data transfer executes via three lines supporting simultaneous transmit and receive operations to reduce data transfer processing time.

Timer

The devices have two 8-bit timer/event counters, one 8-bit and one 16-bit timer, as well as a watchdog timer. The timers can be used as interval timers and external event counters, or to generate square waves of arbitrary frequency. The watchdog timer has interval timer functions, generates non-maskable or maskable interrupts, and is used to detect inadvertent program loops.

Clock Generator

The clock generator provides the operating frequency supplied to the CPU and peripheral hardware and requires an external crystal (1 to 5 MHz). The system clock, controlled by the processor clock control (PCC) register, uses this source to generate the internal operating frequency. Optionally the operating frequency also can be prescaled. Executing the Stop instruction stops oscillation. For power-saving purposes, the devices have a subsystem clock operating at 32.768 kHz.

Interrupt controller

The interrupt controller handles various interrupt requests issued by internal peripheral hardware or external devices. Four external and 12 internal interrupts are incorporated as maskable interrupts, with a priority of 0 to 7.

Comparator

The comparator compares an input voltage with the reference voltage. The result can be read using memory manipulation instruction.

Ordering Information

Power-Saving Features: Normal, Halt and Stop Modes

Voltage	Modes and Typical Power at 5 MHz			
	Normal Mode: Chip 100% On	Halt Mode: CPU Clock Off	Stop Mode: Main Clock Off	
	Main and subsystem clocks On	Main and subsystem clocks On	32 kHz subsystem clock On	32 kHz subsystem clock not used
5 V	28 mW	6.0 mW	0.13 mW	0.0005 mW
2 V	0.8 mW	0.6 mW	0.005 mW	0.0001 mW

Ordering Information (Continued)

Documentation

Document Number	Device	Type
U11047EJ2V0UM00	K0S	Instruction Manual
U12358EJ1V0UM00*	μPD7894xx	User' s Manual
U12240EJ1V0PM00*	μPD78940x	Data Sheet
U12302EJ1V0PM00*	μPD78941x	Data Sheet
U12321EJ1V0PM00*	μPD78F9418	Data Sheet

* Preliminary document

Ordering Information

μPD78940x			μPD78941x		
Part Number	**Internal ROM**	**8-Bit A/D**	**Part Number**	**Internal ROM**	**10-Bit A/D**
μPD789405GC/GK	12 KB mask ROM	7 channels	μPD789415GC/GK	12 KB mask ROM	7 channels
μPD789406GC/GK	16 KB mask ROM	7 channels	μPD789416GC/GK	16 KB mask ROM	7 channels
μPD789407GC/GK	24 KB mask ROM	7 channels	μPD789417GC/GK	24 KB mask ROM	7 channels
			μPD78F9418GC/GK	32 KB mask ROM	7 channels

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