11
ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the MC68HC05B6.

11.1 Absolute maximum ratings

Table 11-1 Absolute maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage (Except V_{PP1})	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Self-check mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to 2V_{DD} + 0.5	V
Operating temperature range – Standard (MC68HC05B6) – Extended (MC68HC05B6C) – Automotive (MC68HC05B6M)	T_A	T_L to T_H 0 to +70 –40 to +85 –40 to +125	°C
Storage temperature range	T_{STG}	– 65 to +150	°C
Current drain per pin (excluding VDD and VSS)(2) – Source – Sink	 I_D I_S	 25 45	 mA mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

11.2 DC electrical characteristics

Table 11-2 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 1.6mA) TDO, SCLK, PLMA, PLMB	 V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 V_{DD} – 0.4 V_{DD} – 0.4	 — —	V
Output low voltage (I_{LOAD} = 1.6mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6mA) $\overline{RESET}$	 V_{OL} V_{OL}	 — 	 0.1 0.4	 0.4 1	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$,TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] RUN (SM = 0) (See Figure 11-1) RUN (SM = 1) (See Figure 11-2) WAIT (SM = 0) (See Figure 11-3) WAIT (SM = 1) (See Figure 11-4) STOP 0 to 70 (standard) – 40 to 85 (extended) – 40 to 105 (extended) – 40 to 125 (automotive)	 I_{DD}	 — — — — — — — —	 3.5 0.5 1 0.35 2 	 6 1.5 2 1 10 20 60 60	 mA mA mA mA µA µA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	±0.2	±1	µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	±0.2 ±0.2	±1 ±1	mA
Input current (– 40 to 125) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI,	I_{IN}	—	—	±5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{IN} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 — —	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25°C only.

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 4.2MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD}$ – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

11.2.1 I_{DD} trends for 5V operation

For the examples below, typical values are at the mid-point of the voltage range and at a temperature of 25°C only.

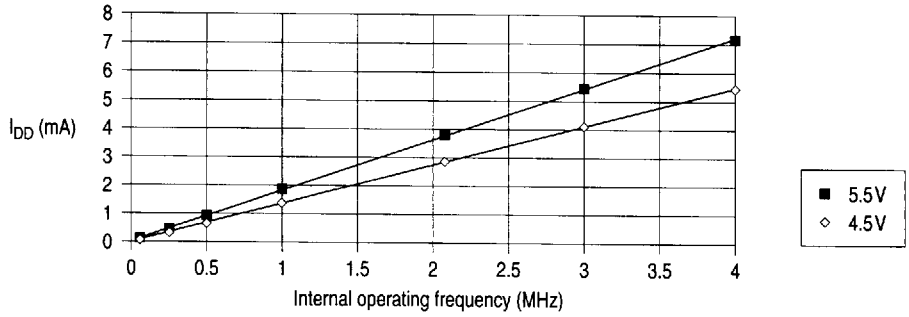


Figure 11-1 Run I_{DD} vs internal operating frequency (4.5V, 5.5V)

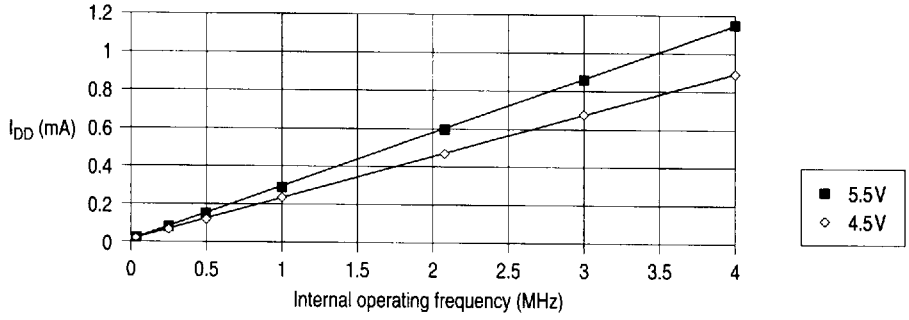


Figure 11-2 Run I_{DD} (SM = 1) vs internal operating frequency (4.5V, 5.5V)

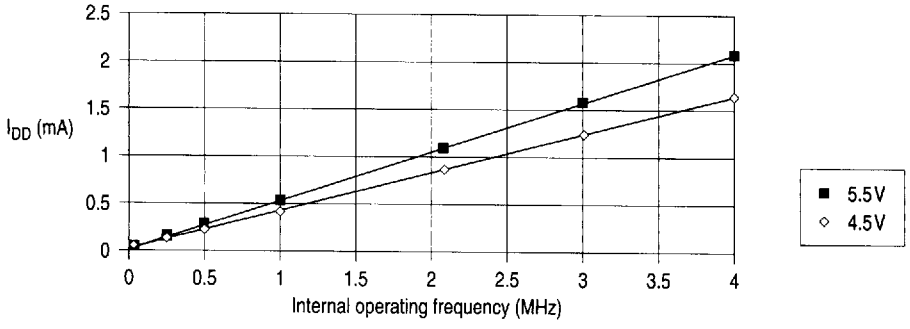


Figure 11-3 Wait I_{DD} vs internal operating frequency (4.5V, 5.5V)

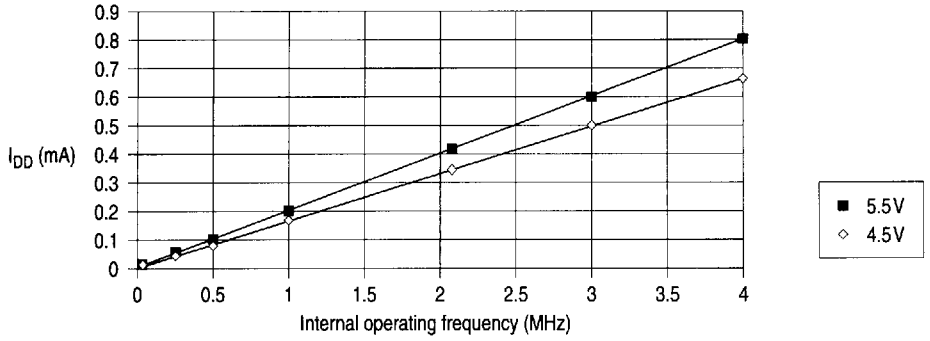


Figure 11-4 Wait I_{DD} (SM = 1) vs internal operating frequency (4.5V, 5.5V)

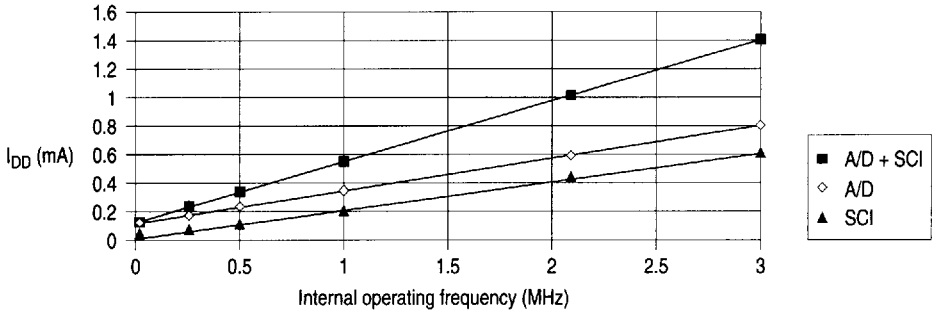


Figure 11-5 Increase in I_{DD} vs frequency for A/D, SCI systems active, VDD = 5.5V

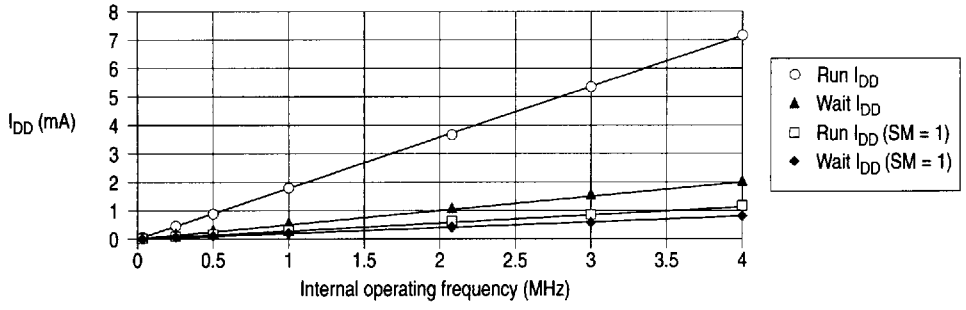


Figure 11-6 I_{DD} vs mode vs internal operating frequency, V_{DD} = 5.5V

Table 11-3 DC electrical characteristics for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.2mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 0.4mA) TDO, SCLK, PLMA, PLMB	 V_{OH} V_{OH}	 V_{DD} – 0.3 V_{DD} – 0.3	 V_{DD} – 0.1 V_{DD} – 0.1	 — —	V
Output low voltage (I_{LOAD} = 0.4mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 0.4mA) $\overline{RESET}$	 V_{OL} V_{OL}	 — 	 0.1 0.2	 0.3 0.6	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] RUN (SM = 0) (See Figure 11-1) RUN (SM = 1) (See Figure 11-2) WAIT (SM = 0) (See Figure 11-3) WAIT (SM = 1) (See Figure 11-4) STOP 0 to 70 (standard) – 40 to 85 (extended) – 40 to 105 (extended) – 40 to 125 (automotive)	 I_{DD}	 — — — — — — — —	 1.2 0.2 0.4 0.15 1 — — —	 3 1 1.5 0.5 10 10 40 40	 mA mA mA mA µA µA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	±0.2	±1	µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	±0.2 ±0.2	±1 ±1	µA
Input current (– 40 to 125) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI,	I_{IN}	—	—	±5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{IN} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 — —	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25°C only.

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 2.0MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD}$ – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

11.2.2 I_{DD} trends for 3.3V operation

For the examples below, typical values are at the mid-point of the voltage range and at a temperature of 25°C only.

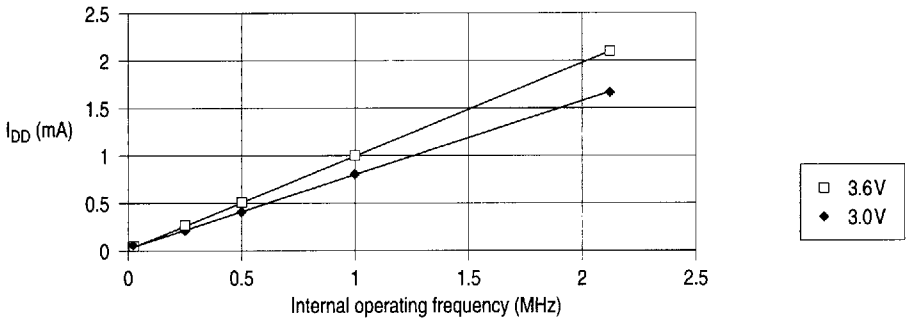


Figure 11-7 Run I_{DD} vs internal operating frequency (3 V, 3.6 V)

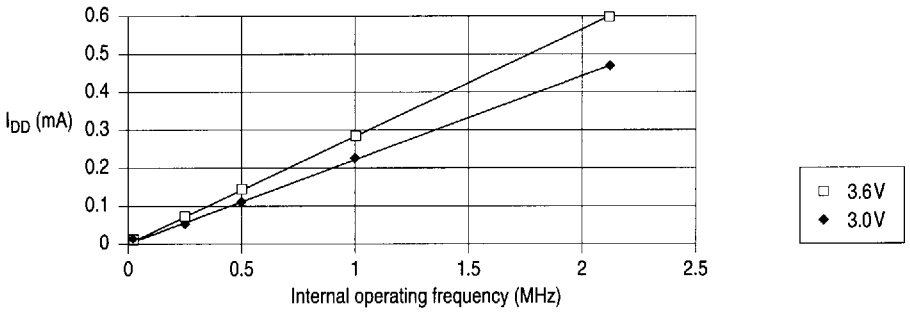


Figure 11-8 Run I_{DD} (SM = 1) vs internal operating frequency (3V,3.6V)

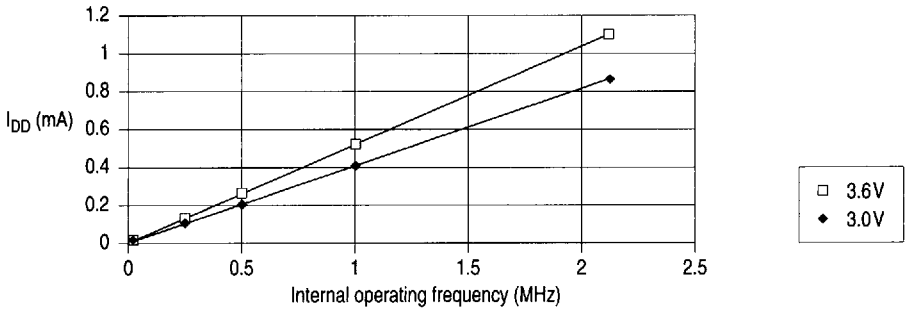


Figure 11-9 Wait I_{DD} vs internal operating frequency (3V, 3.6V)

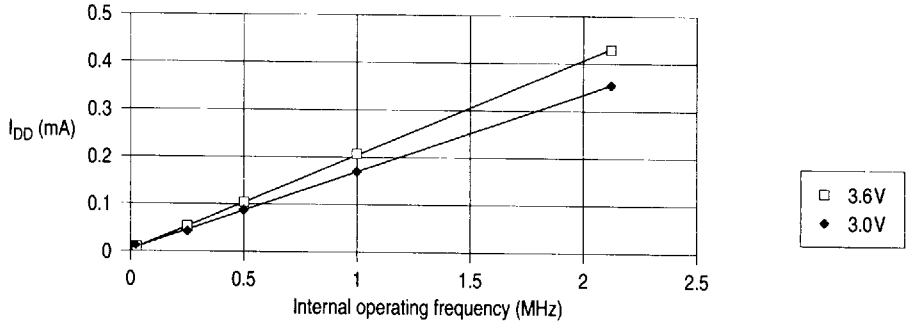


Figure 11-10 Wait I_{DD} (SM = 1) vs internal operating frequency (3V, 3.6V)

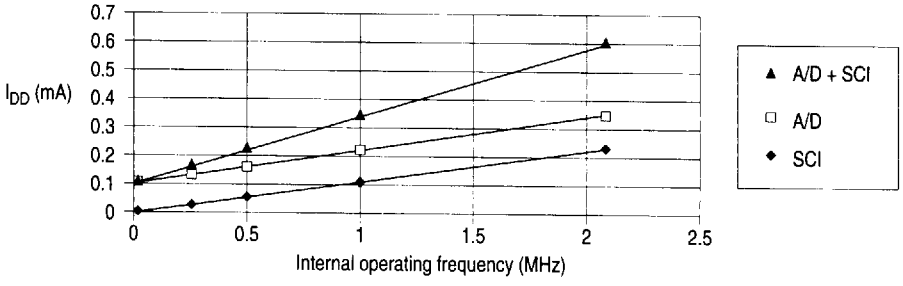


Figure 11-11 Increase in I_{DD} vs frequency for A/D, SCI systems active, V_{DD} = 3.6V

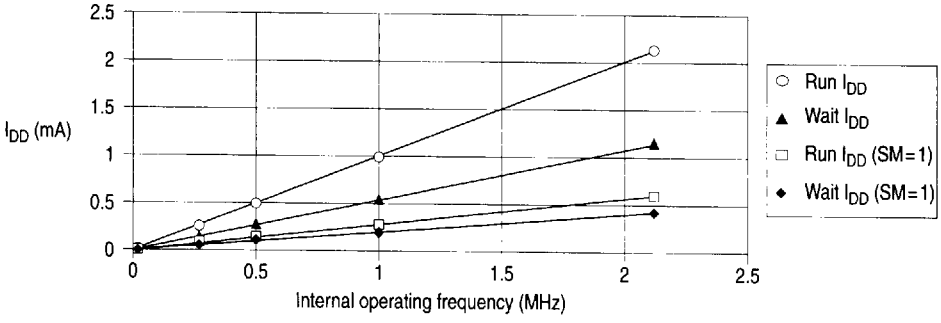


Figure 11-12 I_{DD} vs mode vs internal operating frequency, V_{DD} = 3.6V

11.3 A/D converter characteristics

Table 11-4 A/D characteristics for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	± 0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	± 0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	± 1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
ΔV_R(1)	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(2)	 — —	 12 12	 t_{CYC} µs
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(3)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Performance verified down to 2.5V ΔVR, but accuracy is tested and guaranteed at ΔVR = 5V±10%.

(2) Source impedances greater than 10kΩ will adversely affect internal charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

11

Table 11-5 A/D characteristics for 3.3V operation

(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	± 1	LSB
Quantization error	Uncertainty due to converter resolution	—	± 1	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	± 2	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion Internal RC oscillator	—	32	µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling Internal RC oscillator(1)	—	12	µs
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(2)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Source impedances greater than 10kΩ will adversely affect internal charging time during input sampling.

(2) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

11.4 Control timing

Table 11-6 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	4.2	MHz
External clock option	f_{OSC}	dc	4.2	MHz
Internal operating frequency ($f_{OSC}/2$)				
Using crystal	f_{OP}	dc	2.1	MHz
Using external clock	f_{OP}	dc	2.1	MHz
Cycle time (see Figure 9-1)	t_{CYC}	476	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	10	—	ms
– 40 to 85 (extended)	t_{ERA}	10	—	ms
– 40 to 125 (automotive)	t_{ERA}	10	—	ms
EEPROM byte program time[1]				
0 to 70 (standard)	t_{PROG}	10	—	ms
– 40 to 85 (extended)	t_{PROG}	10	—	ms
– 40 to 125 (automotive)	t_{PROG}	20	—	ms
Timer (see Figure 11-13)				
Resolution[2]	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—[3]	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—[4]	—	t_{CYC}
OSC1 pulse width[5]	t_{OH}, t_{OL}	90	—	ns
Write/Erase endurance[6][7]	—	10000		cycles
Data retention[6][7]	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

(5) t_{OH} and t_{OL} should not total less than 238ns.

(6) At a temperature of 85°C

(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

Table 11-7 Control timing for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)				
Using crystal	f_{OP}	—	1.0	MHz
Using external clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure 11-13)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	200	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

(5) t_{OH} and t_{OL} should not total less than 500ns.

(6) At a temperature of 85°C

(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

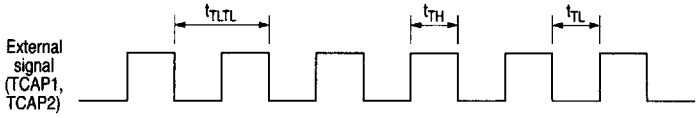
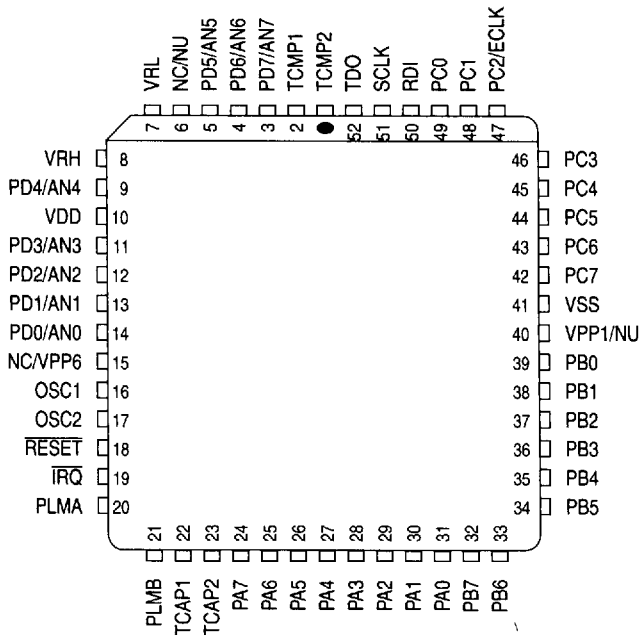


Figure 11-13 Timer relationship

12
MECHANICAL DATA

12.1 MC68HC05B family pin configurations

12.1.1 52-pin plastic leaded chip carrier (PLCC)



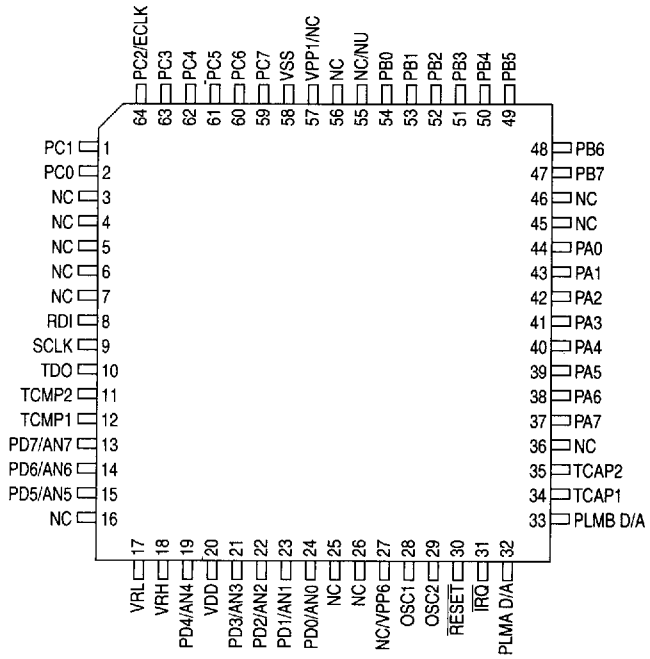
Device	Pin 6	Pin 15	Pin 40
MC68HC05B4	NC	NC	NU
MC68HC05B6	NC	NC	VPP1
MC68HC05B8	NC	NC	VPP1
MC68HC05B16	NC	NC	VPP1
MC68HC05B32	NC	NC	VPP1
MC68HC705B5	NC	VPP6	NU
MC68HC705B16	NU	VPP6	VPP1
MC68HC705B16N	NU	VPP6	VPP1
MC68HC705B32	NU	VPP6	VPP1

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-1 52-pin PLCC pinout for the MC68HC05B6

12.1.2 64-pin quad flat pack (QFP)



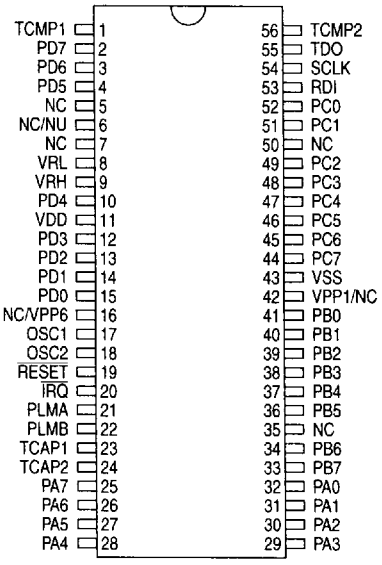
Device	Pin 27	Pin 55	Pin 57
MC68HC05B4	NC	NC	NC
MC68HC05B6 MC68HC05B8 MC68HC05B16 MC68HC05B32	NC	NC	VPP1
MC68HC705B5	Not available in this package		
MC68HC705B16	VPP6	NU	VPP1
MC68HC705B16N	VPP6	NU	VPP1
MC68HC705B32	VPP6	NC	VPP1

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-2 64-pin QFP pinout for the MC68HC05B6

12.1.3 56-pin shrink dual in line package (SDIP)



Device	Pin 6	Pin 16	Pin 42
MC68HC05B4	NC	NC	NC
MC68HC05B6	NC	NC	VPP1
MC68HC05B8	NC	NC	VPP1
MC68HC05B16	NC	NC	VPP1
MC68HC05B32	NC	NC	VPP1
MC68HC705B5	NC	VPP6	NC
MC68HC705B16	Not available in this package		
MC68HC705B16N	Contact Sales		
MC68HC705B32	NU	VPP6	VPP1

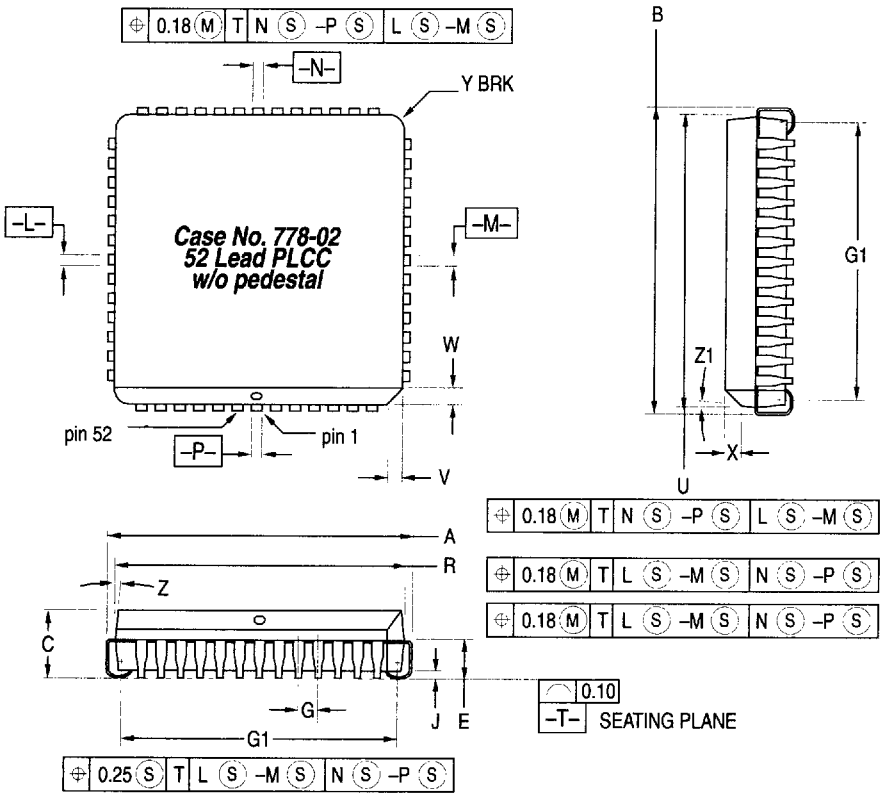
NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-3 56-pin SDIP pinout for the MC68HC05B6

12.2 MC68HC05B6 mechanical dimensions

12.2.1 52-pin plastic leaded chip carrier (PLCC)



Dim.	Min.	Max.
A	19.94	20.19
B	19.94	20.19
C	4.20	4.57
E	2.29	2.79
F	0.33	0.48
G	1.27 BSC	
H	0.66	0.81
J	0.51	—
K	0.64	—
R	19.05	19.20

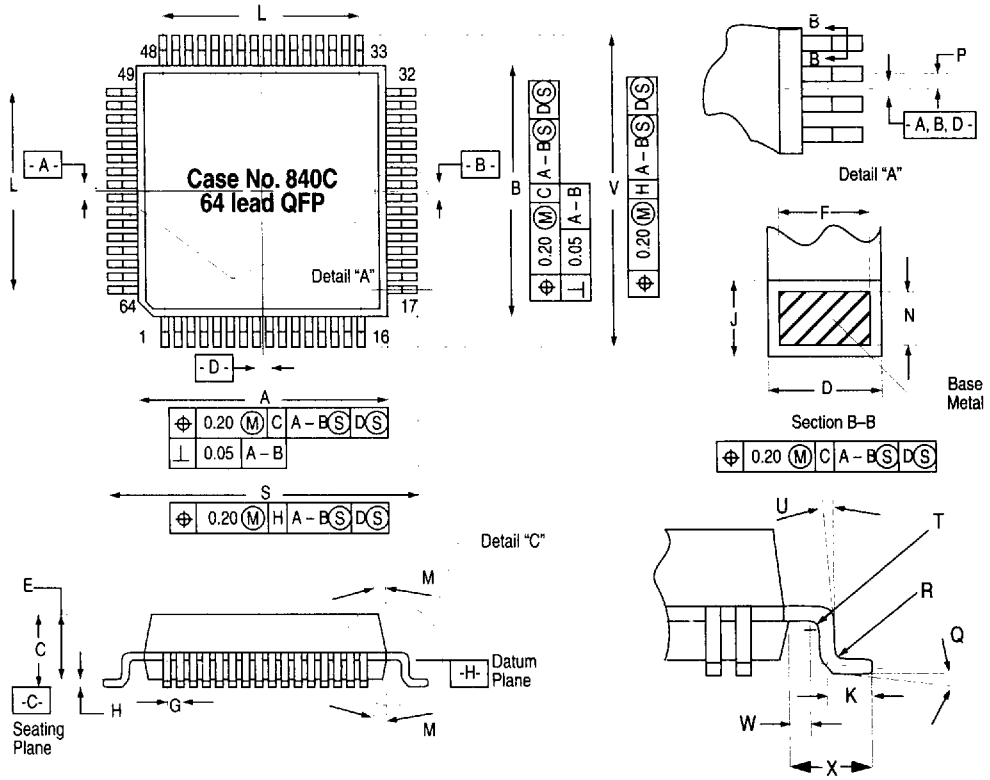
Notes

1. Datums -L-, -M-, -N- and -P- are determined where top of lead shoulder exits plastic body at mould parting line.
2. Dimension G1, true position to be measured at datum -T- (seating plane).
3. Dimensions R and U do not include mould protrusion. Allowable mould protrusion is 0.25mm per side.
4. Dimensions and tolerancing per ANSI Y 14.5M, 1982.
5. All dimensions in mm.

Dim.	Min.	Max.
U	19.05	19.20
V	1.07	1.21
W	1.07	1.21
X	1.07	1.42
Y	—	0.50
Z	2°	10°
G1	18.04	18.54
K1	1.02	—
Z1	2°	10°

Figure 12-4 52-pin PLCC mechanical dimensions

12.2.2 64-pin quad flat pack (QFP)



Dim.	Min.	Max.
A	13.90	14.10
B	13.90	14.10
C	2.067	2.457
D	0.30	0.45
E	2.00	2.40
F	0.30	—
G	0.80 BSC	
H	0.067	0.250
J	0.130	0.230
K	0.50	0.66
L	12.00 REF	

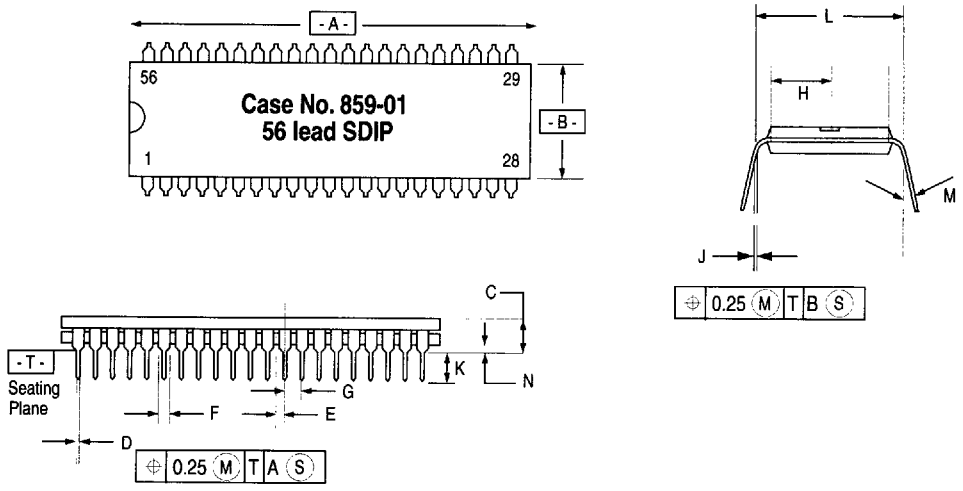
Notes

1. Datum Plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
2. Datums A–B and –D to be determined at Datum Plane –H–.
3. Dimensions S and V to be determined at seating plane –C–.
4. Dimensions A and B do not include mould protrusion. Allowable mould protrusion is 0.25 mm per side. Dimensions A and B do include mould mismatch and are determined at Datum Plane –H–.
5. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the D dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
6. Dimensions and tolerancing per ANSI Y 14.5M, 1982.
7. All dimensions in mm.

Dim.	Min.	Max.
M	5°	10°
N	0.130	0.170
P	0.40 BSC	
Q	2°	8°
R	0.13	0.30
S	16.20	16.60
T	0.20 REF	
U	9°	15°
V	16.20	16.60
W	0.042 NOM	
X	1.10	1.30

Figure 12-5 64-pin QFP mechanical dimensions

12.2.3 56-pin shrink dual in line package (SDIP)



Dim.	Min.	Max.	Notes	Dim.	Min.	Max.
A	51.69	52.45	1. **Due to space limitations, this case shall be represented by a general case outline, rather than one showing all the leads.** 2. Dimensions and tolerancing per ANSI Y 14.5 1982. 3. All dimensions in mm. 4. Dimension L to centre of lead when formed parallel. 5. Dimensions A and B do not include mould flash. Allowable mould flash is 0.25 mm.	H	7.62 BSC	
B	13.72	14.22		J	0.20	0.38
C	3.94	5.08		K	2.92	3.43
D	0.36	0.56		L	15.24 BSC	
E	0.89 BSC			M	0°	15°
F	0.81	1.17		N	0.51	1.02
G	1.778 BSC					

Figure 12-6 56-pin SDIP mechanical dimensions

12